UG0812

User Guide

T-Format Interface

February 2018

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

Revision 1.0 was published in February 2018. It was the first publication of this document.

2 Introduction

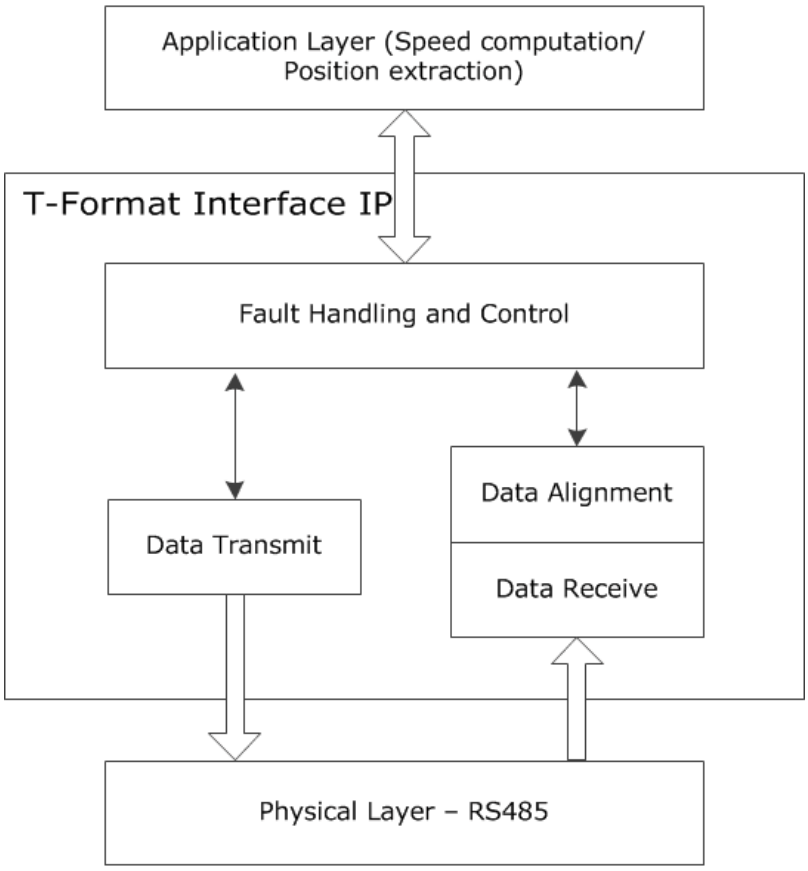
The T-Format interface IP has been designed to provide an interface for the FPGAs to communicate with various compliant Tamagawa products such as rotary encoders.

2.1 Key Features

The following list has the key features of the T-Format interface IP:

- Transmits and Receives serial data from the physical layer (RS-485 interface).
- Aligns data as per T-Format and provides this data as registers that can be read by subsequent blocks.
- Checks for errors, such as Parity, cyclic redundancy check **(**CRC) mismatch, Transmit errors and so on reported by the external device.
- Provides an alarm function that is triggered if the number of fault occurrences exceeds a configured threshold.
- Provides ports for an external CRC generator block, so that the user can modify the CRC polynomial if necessary.

Figure 1 • Top Level Block Diagram of T-Format Interface IP



For complete details on T-Format, see Tamagawa datasheets. Table 1 (see page 3) shows the various commands that can be used to request data from the external device and their functions, and the number of data fields returned for each command.

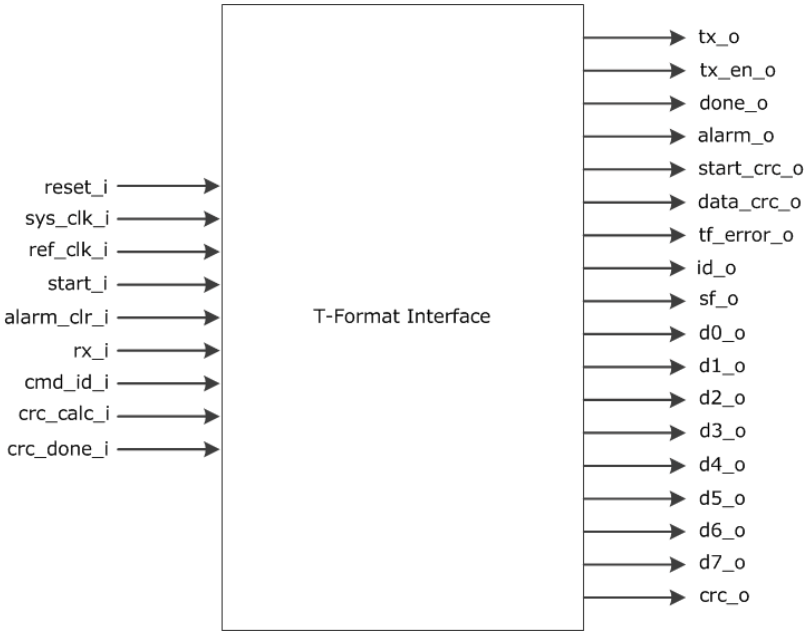
Table 1 • Commands for Control Field

Command ID	Function	Number of Data Fields in Received Frame
0	Rotor Angle (Data Read)	3
1	Multiturn data (Data Read)	3
2	Encoder ID (Data Read)	1
3	Rotor Angle and Multiturn data(Data Read)	8
7	Reset	3
8	Reset	3
C	Reset	3

3 Hardware Implementation

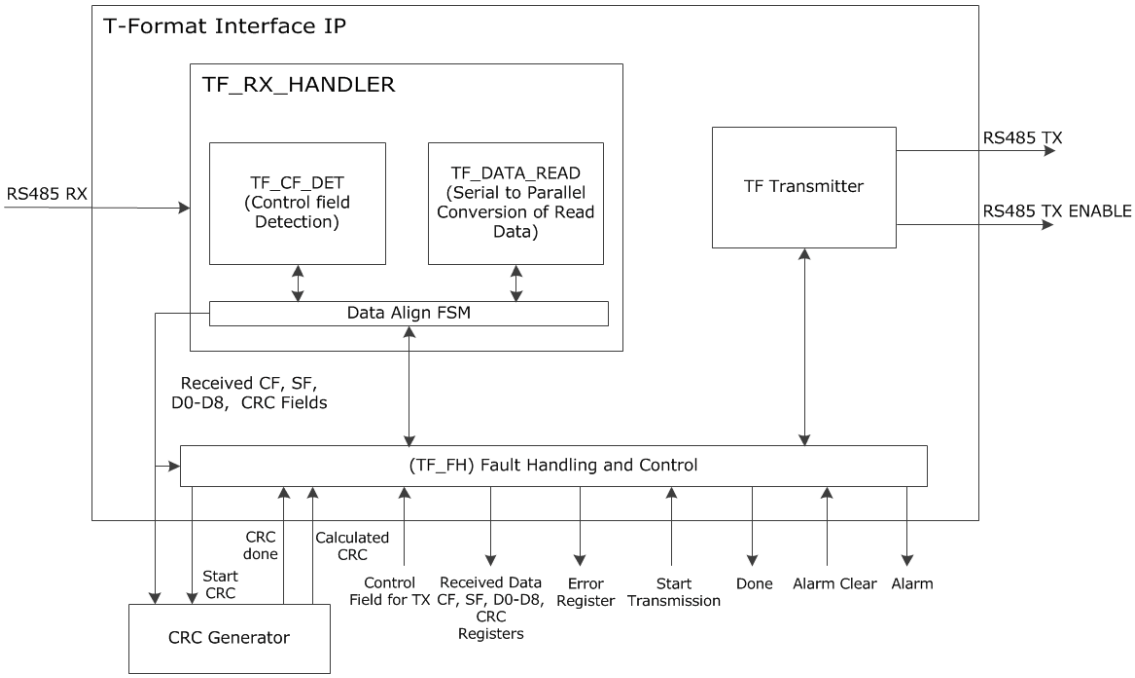
The following figure shows the block diagram of T-Format interface.

Figure 2 • Block Diagram of T-Format Interface



The following figure shows the functional block diagram of T-Format interface.

Figure 3 • Functional Block Diagram of T-Format Interface IP



Each communication transaction in T-Format starts with a transmission of Control Frame (CF) from the requestor, followed by a frame received from the external device. The TF Transmitter block generates serial data to be sent to the external device. It also generates an optional tx_en_o signal required by some RS-485 converters. The encoder receives the data transmitted, and transmits a frame of serial data to the IP, which is received in the rx_i input port of the IP block. The TF_CF_DET block first detects the control field and identifies the ID value. The data length is determined based on the received ID value, and subsequent fields are received and stored in respective registers using the TF_DATA_READ block. After the complete data is stored, the data in all fields except the CRC field is sent to an external CRC generator block, and the calculated CRC generated by this block is compared to the CRC received. Some of the other errors are also checked, and the done_o signal is asserted (‘1’ for one sys_clk_i cycle) after every error free transaction. For more information, see the following section.

3.1 Error Handling

The block identifies the following errors:

- Parity error in the received control field.
- Bad start sequence in received control field.
- Incomplete message where the RX line is stuck at 0 or stuck at 1.
- CRC mismatch between data in received CRC field, and calculated CRC.
- Transmit Errors such as parity error or delimiter error in transmitted CF, as read from bit 6 and bit 7 of the status field (see Tamagawa datasheet).

These errors, when identified by the block, result in a fault counter getting incremented. When the fault counter value exceeds the configured threshold value (configured using g_FAULT_THRESHOLD), the alarm_o output is asserted. The alarm output is deasserted when the alarm_clr_i input is high for one sys_clk_i period. The tf_error_o signal is used to display the type of error that has occurred. This data is reset to 0, when the next transaction begins (start_i is ‘1’).

The following table describes various errors and their corresponding bit position in the tf_error_o register.

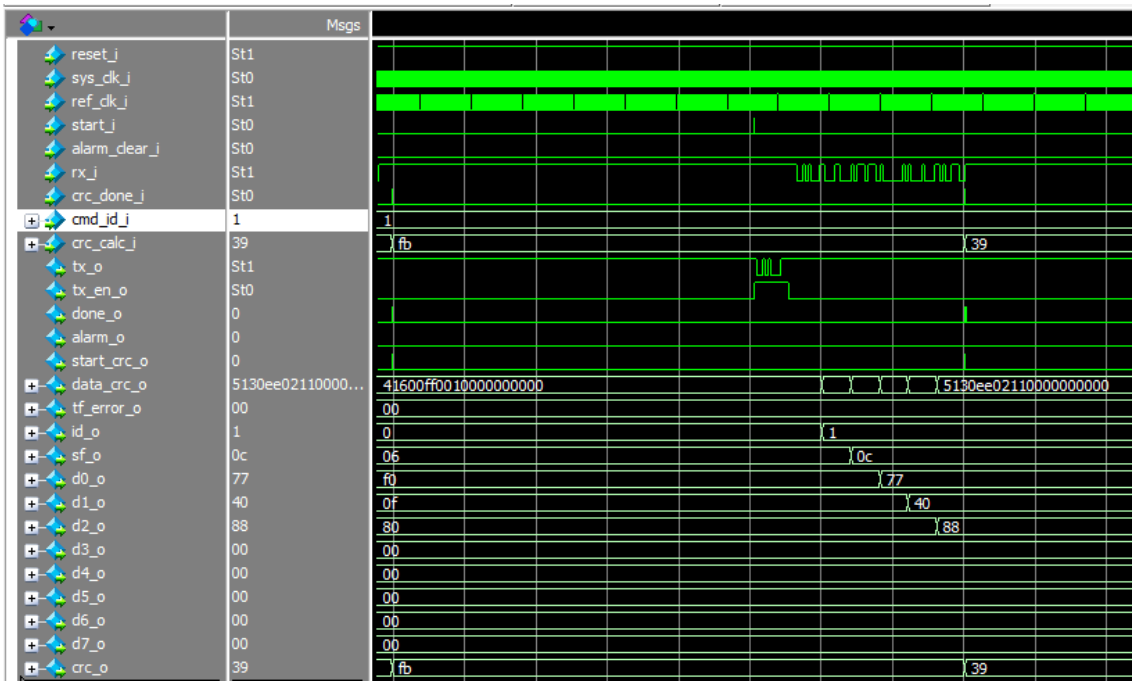
Table 2 • tf_error_o Register Description

Bit	Function
5	TX delimiter error – as indicated in bit 7 of status field
4	TX parity error – as indicated in bit 6 of status field
3	CRC mismatch between CRC field received from slave and calculated CRC data
2	Incomplete message – delimiter error resulting in timeout
1	Bad start sequence in received control field – “0010” not received before timeout
0	Parity Error in received control field

3.2 Timing Diagrams

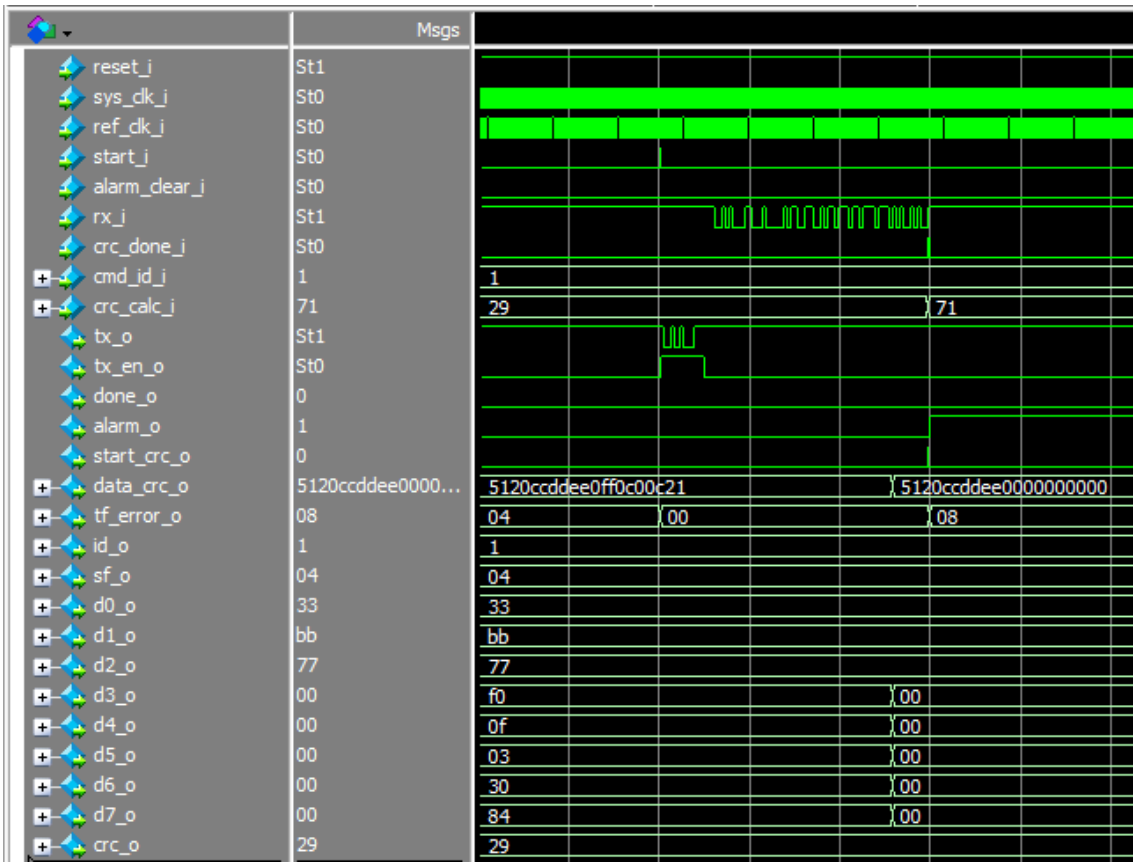
The following figure shows a normal T-Format transaction. The done_o signal is generated at the end of every error free transaction, and the tf_error_o signal remains at 0.

Figure 4 • Timing Diagram – Normal Transaction



The following figure shows a T-Format transaction with CRC error. The done_o signal is not generated, and the tf_error_o signal is 8, indicating that a CRC mismatch has occurred. The done_o signal is generated if the next transaction does not have any error.

Figure 5 • Timing Diagram – CRC Error



3.3 Inputs and Outputs

The following table lists the description of input and output ports of T-Format interface.

Table 3 • Inputs and Outputs of T-Format Interface

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal to design.
sys_clk_i	Input	System Clock.
ref_clk_i	Input	Reference clock, 2.5MHz.*
start_i	Input	Start signal to start T-Format transaction – should be '1' for one sys_clk_i cycle.
alarm_clr_i	Input	Clear alarm signal – should be '1' for one sys_clk_i cycle.
rx_i	Input	Serial data input from encoder.
crc_done_i	Input	Done signal from external CRC block – should be '1' for one sys_clk_i cycle.
cmd_i	Input	Control Field ID to be sent to encoder.
crc_calc_i	Input	Output of CRC Generator block with bits reversed, that is, crc_gen(7) -> crc_calc_i (0), crc_gen(6) -> crc_calc_i(1), .. crc_gen(0) -> crc_calc_i(7).
tx_o	Output	Serial data output to encoder.
tx_en_o	Output	Transmit enable signal – goes high when transmission is in progress.
done_o	Output	Transaction done signal – asserted as a pulse with a width of one sys_clk_i cycle.
alarm_o	Output	Alarm signal – asserted when the number of fault occurrences equals the threshold value configured in g_FAULT_THRESHOLD.
start_crc_o	Output	Start signal for CRC generation block.
data_crc_o	Output	Data for CRC generation block – data is provided as: { CF, SF, D0, D1, D2, .. D7} without delimiters. In case of shorter messages (where only D0-D2 have data), the other fields D3-D7 are taken as 0.
tf_error_o	Output	TF Error register. See Table 1 (see page 3).
id_o	Output	ID value from control field in received frame.*
sf_o	Output	Status field from received frame.*
d0_o	Output	D0 field from received frame.*
d1_o	Output	D1 field from received frame.*
d2_o	Output	D2 field from received frame.*
d3_o	Output	D3 field from received frame.*
d4_o	Output	D4 field from received frame.*
d5_o	Output	D5 field from received frame.*
d6_o	Output	D6 field from received frame.*
d7_o	Output	D7 field from received frame.*
crc_o	Output	CRC field from received frame.*

Note: * For more information, see the Tamagawa datasheet.

3.4 Configuration Parameters

The following table lists the description of the generic configuration parameters used in the hardware implementation of T-Format interface, which can vary based on the application requirements.

Table 4 • Configuration Parameters

Name	Description
g_TIMEOUT_TIME	Defines the timeout time between successive fields in a frame in multiples of sys_clk_i period.
g_FAULT_THRESHOLD	Defines the fault threshold value – alarm_o is asserted when the fault counter exceeds this value (see Error Handling (see page 5)).

3.5 Resource Utilization

The following table lists the resources utilized by the T-Format interface IP, implemented in the SmartFusion®2, IGLOO®2 and RTG4™ devices.

Table 5 • Resource Utilization Report

Resource	Usage
Sequential	260
Combinational Logic	260
MACC	0
RAM1kx18	0
RAM64x18	0

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