Designing a Type-1/2 IEEE 802.3at/af Powered Device

Using PD70101/PD70201 PD Front-End With Integrated PWM Controller ICs

Introduction

The following document provides guidelines for designing a PoE system Powered Device (PD) compliant with IEEE 802.3af (IEEE802.3at Type 1) or 802.3at (Type 2) standards by using Microsemi's PD70101 or PD70201 PD Front End and PWM Controller ICs. The PD70101 and PD70201 ICs are integrated POE Powered Device (PD) Front end and PWM controller for IEEE 802.3af and IEEE 802.3at applications, respectively. The Front End section of the PD70101 IC provides all necessary detection, classification, and operating current levels compliant with the IEEE 802.3af PoE standard. The Front end section of the PD70201 IC provides the necessary detection, classification, 2-event mark for "AT" flag, and operating current levels compliant with the IEEE 802.3at Type 2 standard. The PWM controller section of both PD70101 and PD70201 ICs integrate all functions necessary to provide a complete DC/DC solution for both isolated and non-isolated application requirements.

This document includes a brief overview of PoE functionality with respect to the applicable standards; however it is not to be considered a substitute for the IEEE standards. The applicable standard should always be consulted when making decisions affecting the design of the circuit.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- Microsemi Application Note AN193, Designing a type1/2 IEEE 802.3af/at Powered Device Using PD70100/PD70200 Front End ICs, catalogue number 06-0129-080
- PD70101/PD70201 datasheet, catalogue number 06-0132-058

POE Overview

In its simplest form, PoE consists of a power source, referred to as Power Source Equipment (PSE), an Ethernet cable (typically contained in an infrastructure) with maximum length of 100 meters, and a Powered Device (PD) which accepts both data and power from the Power Interface (PI) of the Ethernet cable. The PI is typically an eight pin RJ45 type connector. Per IEEE 802.3at specification, power may be transmitted on one set of 2-pair combinations, designated "Alternate A" or Alternate B". A diagram of this arrangement is shown in Figure 1.

IEEE 802.3af or IEEE 802.3at type 1 PSEs are designed to operate with Ethernet cabling which may include CAT3 (per TIA/EIA 568). As such they may contain 26AWG wire. A cable of this type may impose a 20Ω maximum power loop resistance to a PSE operating into the maximum specified 100 meter cable length. IEEE 802.3at type 2 PSEs are designed to operate at higher output power levels with CAT 5 or higher (per TIA/EIA 568) Ethernet cabling. These cables contain 24AWG wire (or better) and may impose a maximum 12.5Ω power loop resistance to a PSE operating into the maximum specified 100 meter cable length. The voltage drop and internal temperature rise created in a 100 meter Ethernet cable affect the voltage and current available to the PD. A brief comparison between the AF and AT standards for the PSE and the PD are presented in Tables 1 and 2, respectively.

In addition to IEEE 802.3af/at specifications, a compatible PSE may transmit power over all 4 pairs for additional power available to the PD application.

For further information regarding POE please consult Microsemi Application Note AN193, Designing a type1/2 IEEE 802.3af/at Powered Device Using PD70100/PD70200 Front End ICs, catalogue number 06-0129-080.

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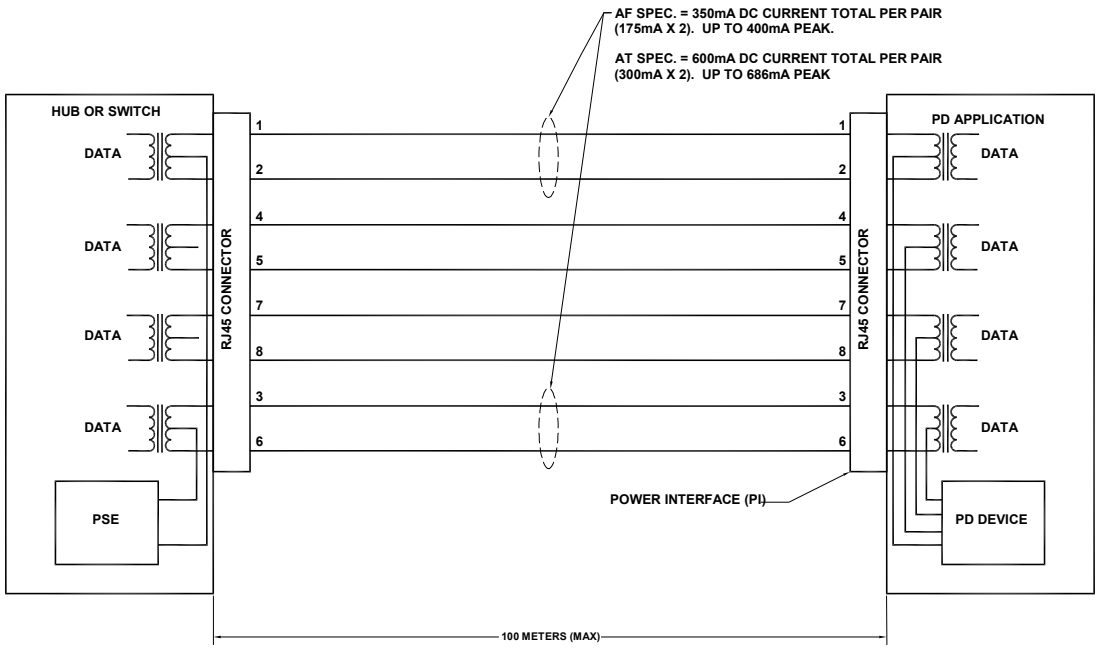
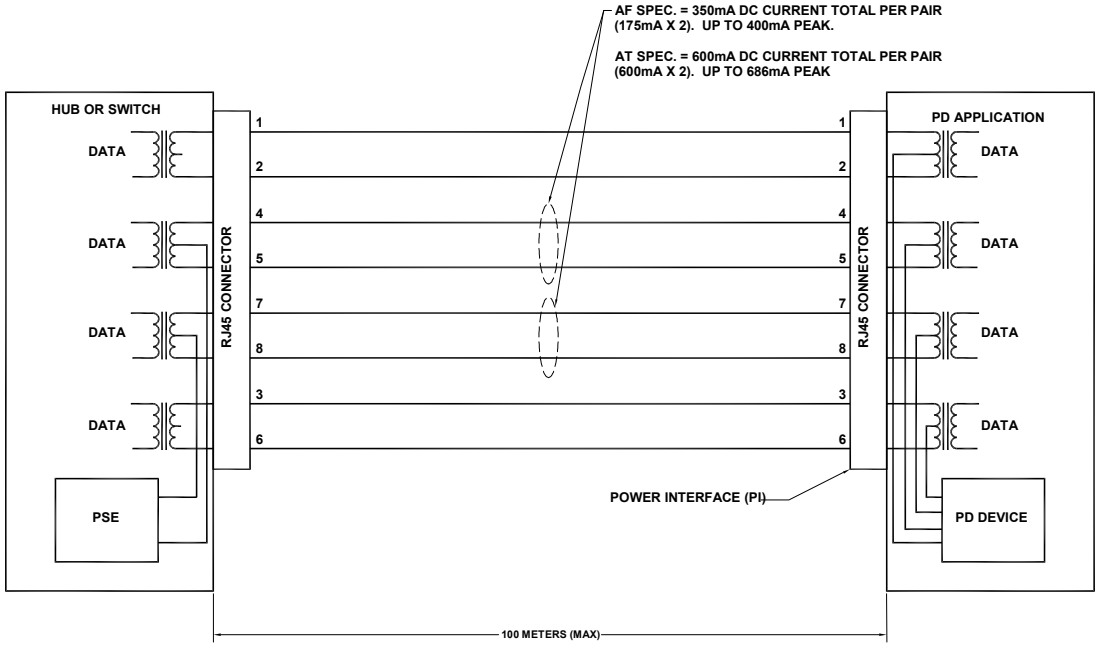
Analog Mixed Signal Group
2381 Morse Avenue, Irvine, CA 92614, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308



Alternative A



Alternative B

Figure 1: Basic PoE Configuration for IEEE 802.3at Standard

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Comparison of IEEE 802.3af and IEEE 802.3at Standards for PSE		
PSE Requirements	**IEEE 802.3af or IEEE 802.3at type 1**	**IEEE 802.3at type 2**
Guaranteed Power at PSE Output	15.4W	30W
PSE Output Voltage	44V to 57V	50V to 57V
Guaranteed Current at PSE Output	350mA DC with up to 400mA peaks	600mA DC with up to 686mA peaks
Maximum Cable Resistance	20Ω	12.5Ω
Physical Layer Classification	Optional	Mandatory
Supported Physical Layer Classification Classes	Class 0 to Class 3	Class 4 - mandatory
Data Link Classification	Optional	Mandatory
2-Events Classification	Not required	Mandatory
4 pairs power feeding	Not allowed	Allowed with 2 collocated PSEs
Communication Supported	10/100 BASE-T (Midspans) 10/100/1000 BASE-T (switches)	10/100/1000 BASE-T Including Midspans (Both type1 and type2)

Table 1: IEEE 802.3af and 802.3at Standards for PSE

Comparison of IEEE 802.3af and IEEE 802.3at Standards for PD		
PD Requirements	**IEEE 802.3af or IEEE 802.3at type 1**	**IEEE 802.3at type 2**
Guaranteed Power at PD Input	12.95W	25.50W
PD Input Voltage	37V to 57V	42.5V to 57V
Guaranteed Current at PD Input	350mA DC with up to 400mA peaks	600mA DC with up to 686mA peaks
Maximum Cable Resistance	20Ω	12.5Ω
Physical Layer Classification	Mandatory (no class = Class 0)	Mandatory
Supported Physical Layer Classification Classes	Class0 to Class3	Class 4 - mandatory
Data Link Classification	Optional	Mandatory
2-Events Classification	Not required	Mandatory
4 pairs power receiving	Allowed	Allowed
Communication Supported	10/100 BASE-T (Midspans) 10/100/1000 BASE-T (switches)	10/100/1000 BASE-T Including Midspans (both type1 and type2)

Table 2: IEEE 802.3af and 802.3at Standards for PD

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PD70101/PD70201 Features

- IEEE 802.3af (IEEE802.3at Type 1) Compliant (PD70101)
- IEEE802.3at Type 2 Compliant (PD70201)
- Support up to 47.7W 4 pair systems with a single PD70201
- Provides PD Detection Signature
- Programmable PD Classification Signature
- Supports 2 Event Classification Flag (PD70201)
- Active Low, Open Drain Power Good Signal
- Integrated Isolation Switch
- 24.9KΩ signature resistor disconnection when power is on
- Inrush Current Limit (Soft Start)
- Integrated 10.5V Start-up Supply for integrated DC/DC controller
- Internal Discharge Circuitry for up to 220µF DC/DC Bulk Capacitor
- Wide Temperature Operating Range -40°C to +85°C
- On-Chip Thermal Protection
- 100 kHz to 500 kHz adjustable DC-DC switching frequency
- DC/DC frequency can be synchronized to external clock
- Supports low power mode operation for higher efficiency
- Soft-start circuit to control the output voltage rise time
- Support efficient synchronous rectification
- PoE Port Input UVLO with programmable threshold and hysteresis
- Internal differential amplifier simplifying non-isolated step down converter
- Over load and short circuit protection

Using PD70101/PD70201: Front End Section

The PD70101's Front End section provides the necessary Detection, Classification, and Isolation Switch control functions for a PoE-powered device conforming to IEEE 802.3af or 802.3at type 1 standards. The PD70201's Front End section provides the same functions as the PD70101, with an additional higher Isolation Switch current capability, additional 2-Events- Classification detection and AT Flag generation conforming to IEEE 802.3at type 2 standards. Both chips are designed for minimal external components.

PD70101/PD70201 IC may be configured as an alternate two or four pair system (see Figure 2) in which one PD70101/PD70201 IC is driven from both diode bridges (output terminals connected in parallel), or may be configured as a four pair system (see Figure 3) in which a single PD70101/PD70201 IC and a single PD70100/PD70200 IC are driven individually by one of the two diode bridges. In four pair, two IC systems the isolation switch output terminals of the PD70101/PD70201 IC and the PD70100/PD70200 IC are connected together in parallel, and the two chips VPP inputs are isolated from one another by using two suitable diodes, each in series with VPP. For each IC, required capacitors of 50nF to 120nF (68nF typically used) are connected across the positive and negative output terminals of the each diode bridge. This configuration, as opposed to the two pair system, allows available output power to affectively double.

In an alternate two pair/four pair single IC system, the two input diode bridge's outputs are wired in parallel, and the common output supplies input power (VPP (+), VPN_IN (-)) to the PD70101/PD70201 IC, which by means of the integrated PWM controller, drives an isolated or non-isolated DC/DC converter (depends on application requirements). The paralleled output terminals from the two diode bridges are connected to the PD70101/PD70201 IC at VPP (positive connection, pin 32), and VPN_IN (negative connection, pin 5). This connection requires a single capacitor of 50nF to 120nF (68nF typically used) connected across the positive and negative output terminals of the paralleled diode bridges. This 68nF capacitor meets the IEEE 802.3af/at standard requirement for hardware detection.

The output connections from the PD70101/PD70201 Front End section are made at VPP (positive connection, pin 32), and VPN_OUT (negative connection, pin 8). VPN_OUT is the primary ground connection from the integrated isolation switch of the PD70101/PD70201 IC to the DC/DC converter. The IC's exposed center pad should be connected electrically to VPN_IN (pin 5)

In addition to the PD70101/PD70201 Front End section's basic input/output connections, the following components are required for a typical application:

- **Detection Resistor:** Connect a 24.9kΩ ±1% resistor between VPP and RDET (Pin 1). This resistor is used to satisfy the Detection signature. A low wattage type may be used as there is less than a 7mW stress on this resistor while Detection phase is active, and the resistor is disconnected after power is on.
- **Reference Resistor:** Connect a 243kΩ ±1% resistor between RREF (pin 3) and VPN_IN (pin 5). This resistor should be located as close as

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practical to the PD70101/PD70201 IC. A low wattage type may be used (there is less than 1mW stress on this resistor).

- **Classification Current Resistor:** The value of this resistor determines the PD current draw during Classification Phase. Values corresponding to IEEE compliant classification levels are shown in Table 4. Connect this resistor between RCLASS (pin 4) and VPN_IN (pin 5).
- **Power Good Pull-up:** Power Good signal is available at PGOOD (pin 2). A PGOOD flag is generated low voltage to optionally inform the application that the power rails for the integrated DC/DC controller are ready, and the DC/DC has begun soft-start. This signal can be used to disable any external input to the PD70101/PD70201's ENABLE pin (pin 10) when operating in a 4-pairs dual IC configuration. PGOOD is an open drain pin which requires a resistor pull-up to be functional. Pull-up voltage on this pin cannot exceed 74V and is recommended to be pulled up to a voltage no higher than VPP. This pin active low and rated at 0.4V and 0.75mA.
- **AT Flag Pull-up (PD70201 only):** AT Flag signal is available at AT_FLAG (pin 7). An AT_FLAG is generated low voltage to inform the application that the PSE providing PD power is IEEE 802.3at compliant. This is an open drain pin which requires a resistor pull-up to be functional. Pull-up voltage on this pin cannot exceed 74V and is recommended to be pulled up to a voltage no higher than VPP. This pin is active low and rated at 0.4V and 0.75mA.
- **Start-up Supply Output Capacitor:** The PD70101/PD70201 contains an internal low power (2mA continuous) regulated DC output available for use as a start-up supply for the integrated DC/DC converter controller. This supply output is available on the VCC pin (pin 31), and is intended to be used in conjunction with an external bootstrapped supply, also connected to the VCC pin. The PD70101/PD70201's VCC pin provides power input to the internal supply rails for the integrated DC/ DC controller. The bootstrapped supply input to VCC is typically provided by means of an auxiliary output from the DC/DC converter, but may be provided by means of any voltage source with a maximum output voltage of 15V (15V provides a safe operating range for the gate drive outputs). The internal start-up supply regulator requires a ceramic capacitor of minimum 4.7µF, to be connected directly between VCC (pin 31) and VPN_OUT (pin 8).

Programmed Classification Signature RCLASS Resistance Values				
Class	RCLASS Resistor Value	PD70101/PD70201 Current Draw During Classification		
		Min.	Average	Max.
0	Open	0		3mA
1	113Ω ±1%	9.5mA	10.5mA	11.5mA
2	64.9Ω ±1%	17.5mA	18.5mA	19.5mA
3	42.2Ω ±1%	26.5mA	28mA	29.5mA
4	30.9Ω ±1%	38mA	40mA	42mA

Table 4: RCLASS Resistance Values

A single PD70101/PD70201 IC may be operated with 4 pairs for extended power capability. Up to 47.7W (PD70201 operating at IEEE 802.3at input voltage levels) is supported. The component requirements for a single PD70101/PD70201 operating with 4 pairs are the same as single IC applications operating with 2 pairs.

A typical 2 pairs/4pairs single IC configuration is outlined in Figure 3.

Some applications may require an indication if power is provided on 4 pairs, or 2 pairs only. An additional circuit may be optionally added to sense if input POE power is provided on 2 pairs or 4 pairs. This circuit is shown in the application example of Figure 2.

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Referencing the optional circuit of Figure 2, the PD70101/PD70201 detection resistor, RDET, is not used, and is replaced by two detection resistors, R3 and R5, which provide the required resistor detection signature for each individual 2 pairs input. R3 and R5 also provide pull up current so that the presence of the individual 2 pairs input may be sensed and combined into a logical OR function via diodes D1 thru D6. The output of this circuit is then used to drive the switch circuit R4, R6, and Q1. The signal present at the Collector of Q1 will be low if only 2 pairs are present and high if all 4 pairs are providing power. Be aware that the output of this 4 pairs detection circuit is at POE voltage levels, and should not directly interface to low-level logic. If required, the Collector of Q1 can interface directly to an optoisolator as shown in the example.

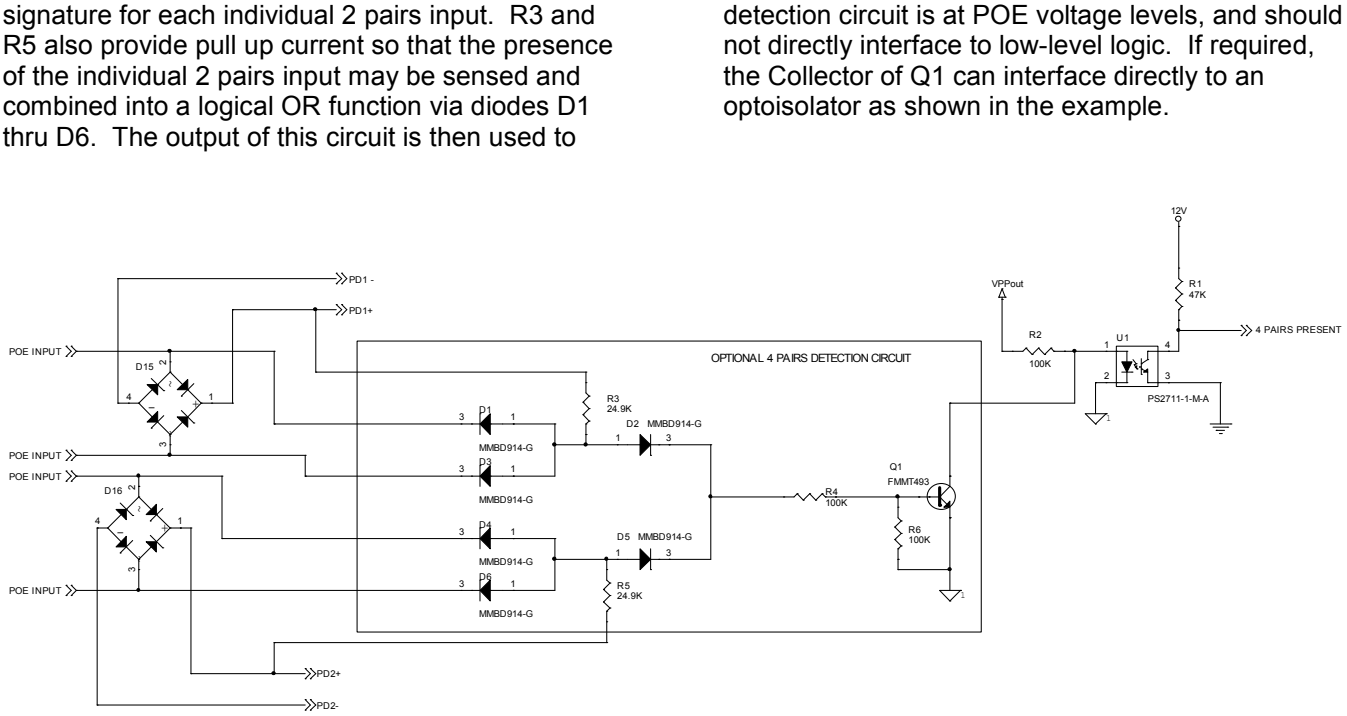


Figure 2. Optional 4 Pairs PSE Detection

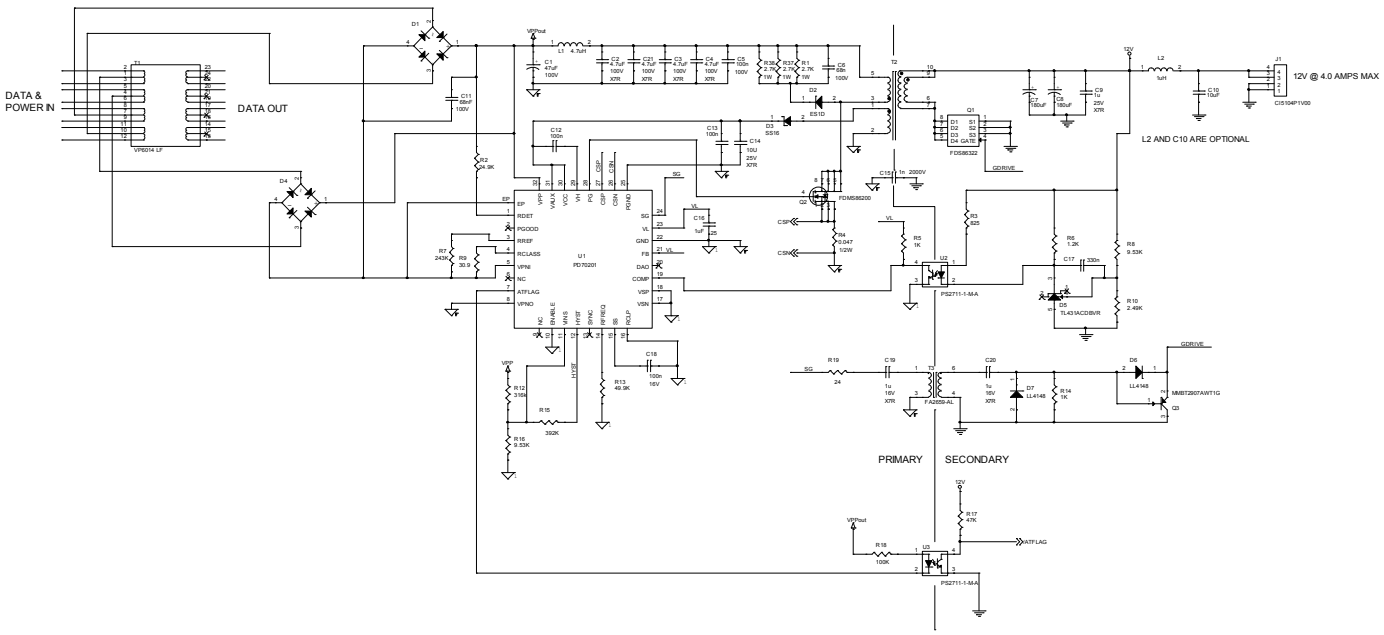


Figure 3. Typical 2 or 4 Pair Configuration with a Single PD70201 IC.

In a 4 pairs dual IC system, a single PD70101/PD70201 IC and a single PD70100/PD70200 are placed in a PD design, each driven by a separate diode bridge. The Isolation Switch output at VPN_OUT is connected in parallel for each IC, while the VPP inputs to PD70101 and PD70100 or PD70201 and PD70200 ICs are connected by means of series blocking diodes. The combined output terminals drive the input filter/bulk capacitor for the DC/DC converter. This affectively doubles the total input power capability to the DC/DC converter.

Under certain conditions, power available at the PI may be on two pairs only. Dual IC configurations where power is applied to only one of the two chips require certain considerations for the AT_FLAG and PGOOD signals.

The AT_FLAG should be connected in a wired-OR configuration. Since the AT_FLAG output is open drain configured, this signal may be easily wired-OR between the PD70101/PD70201 and PD70100/PD70200 ICs for a common AT_FLAG output connection by simply connecting the two AT_FLAG pins together with a common pull-up resistor.

In a dual IC configuration, the PGOOD signal from the PD70100/PD70200 is used to enable the PD70101/PD70201's integrated DC/DC controller during conditions when the PD70101/PD70201's Front End section is not powered, and as such requires special consideration. The PD70101/PD70201's ENABLE pin (pin 10) is active high; it should be tied to ground when it is not used. An example of a dual chip use of DC/DC enable control is shown in Figure 4.

Providing individual PGOOD and AT_FLAG controls between two ICs is necessary for covering all possible power input configurations.

The V_{AUX} regulator output from the single PD70100/PD70200 IC must be connected to the VCC pin of the PD70101/PD70201 IC using a suitable blocking diode. In addition, a blocking diode must be added between the PD70101/PD70201 IC's VAUX pin (pin 31) and VCC pin (pin 30). Small, low current 30V diodes may be used for this requirement.

A typical 4 pairs, 2 IC configuration is outlined in Figure 4.

Operation with an External (non POE) DC Source

PD applications utilizing the PD70101/PD70201 IC may be operated with an external power source (DC wall adaptor). There are three methods of providing power with an external source:

1) External source connected directly to the PD70101/PD70201 Input (VPP to VPN_IN). Requires external source output voltage to be 40V minimum under all load conditions. The adaptor must provide a diode in series with VPP to block reverse current from a fully charged bulk capacitor.

2) External source connected directly to the PD70101/PD70201 output connection to the application. The external source output voltage will be dependent on the application input requirements. Both the external source and the PD70101/PD70201 IC's VPP must have series diodes to block reverse current. If the application's DC/DC converter contains a bootstrapped output connection to VCC, a suitable start-up circuit must be supplied for the external source, as the PD70101/PD70201's internal start-up supply will not function while powering the application with an external source in this configuration. In addition to the start-up supply requirement, an external enable signal is required, as the PD70101/PD70201's internal enable will not function while powering the application with an external source in this configuration. If required, the additional start-up circuit and enable circuit will depend on the application requirements. Note: When not operating with an external adaptor, the PD70101/PD70201 IC's external enable pin should be tied to the GND pin (pin 23).

3) External source connected directly to the application's low voltage supply rails (output side of an isolated or non-isolated power supply). It is recommended the external source contain a series reverse current blocking diode and may optionally be isolated from the application power supply's output by means of a switched connection.

Three examples of PD70101/PD70201 configured with an external wall adaptor are diagrammed in Figure 5.

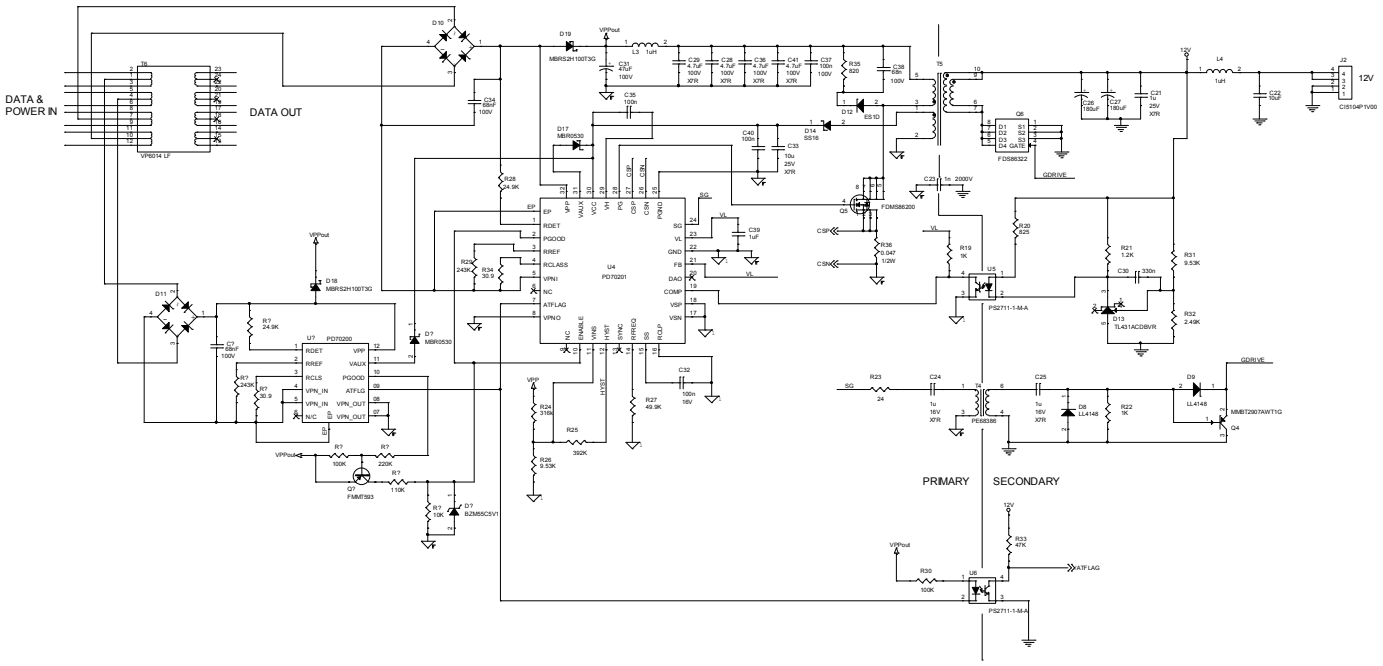
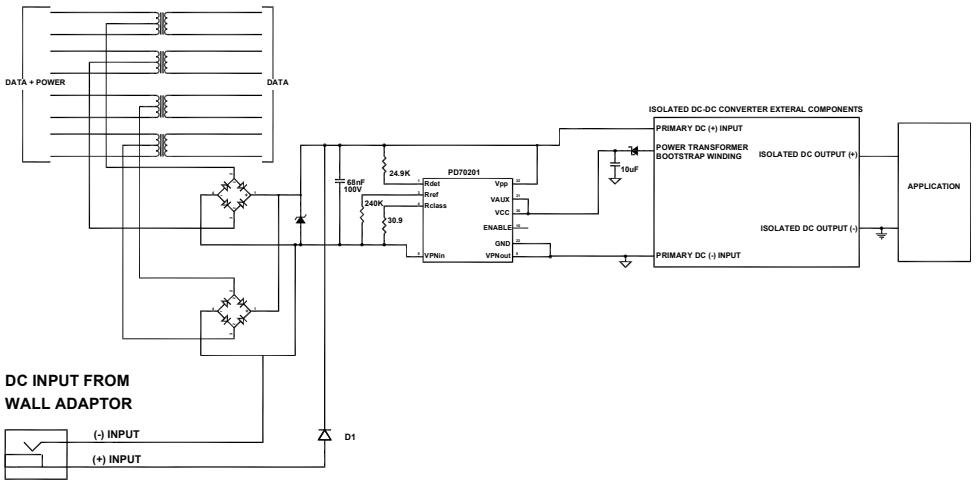
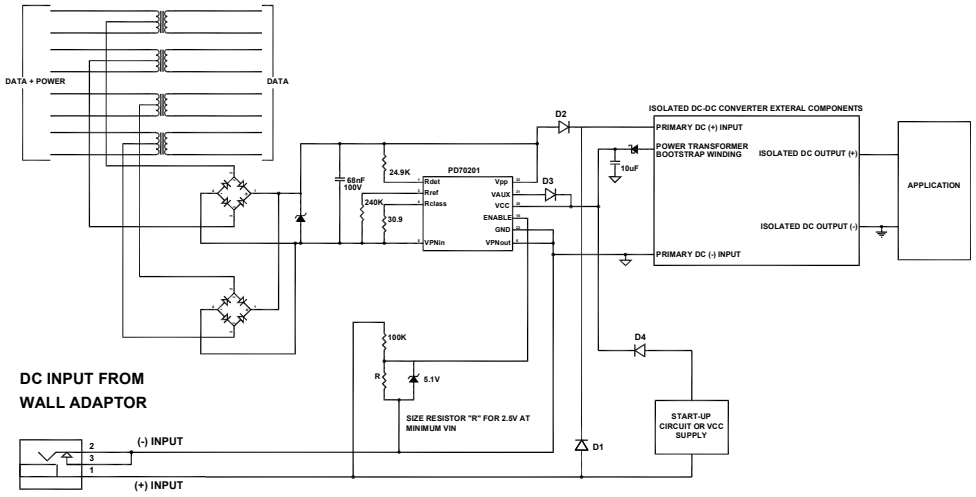


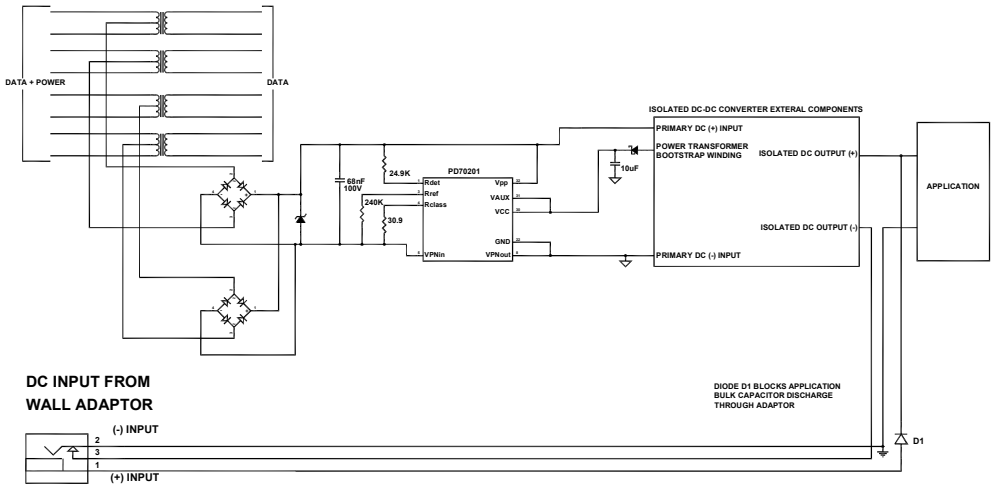
Figure 4: Typical 4 pairs configuration with a PD70200 and PD70201; shows use of ENABLE pin



CONFIGURATION #1: SOURCE CONNECTED TO PD70201 INPUT



CONFIGURATION #2: SOURCE CONNECTED TO PD70201 DC-DC CONVERTER



CONFIGURATION #3: SOURCE CONNECTED TO APPLICATION'S SUPPLY RAILS

Figure 5. External Power Input Configurations

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Soft Start Current Limit

The PD70101/PD70201 IC provides Soft Start current limiting. A rising voltage of 36V to 42V between VPP and VPN_IN will enable the isolation switch in Soft Start Current Limit mode. During this time, the current through the isolation switch is limited to 240mA (typical). The PD70101/PD70201 IC continuously monitors the voltage drop across the isolation switch (VPN_OUT to VPN_IN) during Soft Start mode. When difference between voltages VPN_OUT and VPN_IN drops below 0.7V, the PD70101/PD70201 IC will switch to normal operating mode, in which the isolation switch is fully on, with over-current protection circuitry active.

Soft Start current limit is necessary to limit the inrush current created by the initial charge up of input capacitors upon system start-up. Large inrush currents can create large voltage sags at the PI, which in turn can cause system functions tied to event thresholds (such as AT_FLAG) to reset to their initial states. Soft Start current limit will significantly reduce the voltage sag upon start-up.

The PD70101/PD70201 IC Soft Start function limits current to a maximum of 320mA (240mA typical). Start-up into a fully discharged bulk capacitor will result in large power dissipation in the isolation switch for a period of time dependent on the size of the bulk capacitance. This occurs due to the initial voltage drop across the isolation switch. The maximum initial voltage drop across the isolation switch can be of 42V. In other words, the initial power dissipation of the isolation switch can be no higher than 13.4W (42V x 320mA). The maximum power dissipated by the isolation switch will decrease as the bulk capacitor charges, eventually decreasing to a maximum normal operating power dissipation of 74mW (PD70101) or 311mW (PD70201). The period of time required to switch from Soft Start mode to normal operation mode can be calculated using the following formula:

$$T = \frac{(\Delta V - 0.7) \times C}{I}$$

Whereas:

I = PD70101/PD70201 IC's current during soft start

C = Total input bulk capacitance

ΔV = Initial VPN_OUT – VPN_IN voltage at start of soft start (ΔVmax = VPP)

The PD70101/PD70201 IC can safely operate with a total bulk capacitance of 220µF.

Bulk Capacitor Discharge

The PD70101/PD70201 IC provides discharge of the application bulk capacitor when VPP – VPN_IN falling voltage drops below the isolation switch turn-off threshold (31V to 34V). This feature insures that the application bulk capacitance does not discharge through the detection resistor, which can cause the detection signature to fail and prevent the PSE from starting the PD. While enabled, the discharge function provides a minimum controlled discharge current of 23.8mA, which flows through the VPP pin, internally through the isolation MOSFET's body diode, and out through the VPN_OUT pin. The discharge circuitry monitors the voltage difference between VPP – VPN_OUT, and remains active while the difference voltage is 1.5V ≤ (VPP – VPN_OUT) ≤ 32V. The maximum time to discharge can be calculated by:

$$T = \frac{(\Delta V - 1.5V) \times C}{0.0228}$$

Whereas:

C = Total Input Bulk Capacitance

ΔV = Initial VPP – VPN_OUT Voltage at Isolation Switch Turn-off

Example: Assuming an initial capacitor voltage of 32V, it will take 294ms for a 220µF capacitor to discharge to a 1.5V level.

The PD70101/PD70201 discharge circuitry can be safely operated with a bulk capacitance of up to 220µF.

V_{AUX} regulated output is enabled only when the isolation switch is in normal operation mode. This insures DC/DC controller does not start prematurely.

PGOOD Output

PD70101 and PD70201 IC provide an open drain output indicating POE power good status. This output is in a high impedance state until VPP – VPN_IN voltage exceeds the isolation switch turn-on threshold, and isolation switch moves from Soft Start current limit mode to normal operation mode. Upon assertion, the PGOOD output switches to ground. When VPP – VPN_IN voltage falls below the isolation switch turn-off threshold, the PGOOD output reasserts back to high impedance state.

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AT_FLAG Output (PD70201 only)

The PD70201 IC provides an open drain output indicating a 2 Events Classification was detected. This output is in a high impedance state until the VPP – VPN_IN voltage exceeds the isolation switch turn-on threshold and the isolation switch moves from Soft Start Current Limit mode to normal operation mode. It will then assert to low, but only if a 2 Events Classification Signature was recognized during Classification phase described earlier. Upon assertion, the AT_FLAG output switches to ground. The AT_FLAG output re-asserts back to the high impedance state when the VPP – VPN_IN voltage falls below the isolation switch turn-off threshold.

The AT_FLAG signal is synchronized with the PGOOD signal. For example, PGOOD can be asserted without asserting AT_FLAG, but AT_FLAG cannot be asserted without asserting PGOOD.

The AT_FLAG signal is typically used for indicating the PD application that PSE is capable of supplying AT power levels. Often the PD application is electrically isolated. The AT_FLAG is referenced to the primary ground. As such, it requires an optoisolator to provide an isolation barrier between primary ground and application ground for electrically isolated applications.

Thermal Protection

The PD70101/PD70201 IC provides thermal protection. Integrated thermal sensors monitor the internal temperatures of the isolation switch and classification current source. If the overtemperature threshold of either sensor is exceeded, that sensor's respective circuit will disable.

To insure trouble free operation, it is important that PD70101/PD70201 IC's exposed pad is mounted to a copper area on the PCB that provides an adequate heatsink.

Using PD70101/PD70201: PWM Controller Section

The PD70101/PD70201's PWM Controller section provides all functions necessary to control both isolated and non-isolated DC/DC topologies, including isolated Flyback and Forward converter topologies, as well as non-isolated Buck and Boost topologies.

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The following considerations should be made when using the PD70101/PD70201 PWM controller:

- **Frequency Setting Resistor (RFREQ):** The value of this resistor determines the switching frequency, as well as sets the pin current for both SS and RCLP pins. The value of RFREQ is based on the following equation:

$$Freq = 10x10^9/R_{FREQ}$$

Resistor Range = 100kΩ to 20kΩ

- **Soft Start Charge Current:** The DC/DC soft start time is determined by the value of the

capacitor connected to the SS pin, and the SS pin's charging current. The charging current is calculated:

$$I_{SS\_CHG} = 1.2V/R_{FREQ}$$

The time required for soft start to complete is determined by the time required for the SS pin voltage to transition from 0 to 1.1V (min). This can be calculated with the following equation:

$$T_{SS} = (R_{FREQ} \times C_{SS} \times 1.1)/1.2$$

- **Low Power Mode Clamp Threshold:** The Low Power Mode Clamp Threshold is set by the resistor connected between RCLP pin (pin 17) and GND. The value is determined by the following equation:

$$V_{CLAMP} = 0.3 \times (R_{CLP}/R_{FREQ})$$

The clamp voltage determines the threshold below which the DC/DC converter enters low power skip mode (LPM). This threshold is typically set as a percentage of the peak inductor current at maximum output load and minimum input voltage. V_{CLAMP} voltage equates to a percentage of peak current by the following:

$$I_{LPM} = [(0.9 \times V_{CLAMP})/1.2] \times I_{PK\ (MAX)};$$

$I_{PK\ (MAX)}$ = maximum peak inductor current set by the current sense resistor (assumes $V_{RCS} = 0.12V$ at maximum peak current).

During start up, it starts with LPM mode until Vcomp voltage goes higher than 0.2V and/or $V_{CLAMP} \le 1.11x(V_{COMP}-0.25V)$, ($V_{COMP} \ge 0.25V$). Connecting the RCLP pin to ground disables LPM mode during normal operation.

- **VPP UVLO:** The PD70101/PD70201 ICs offer a VPP monitoring UVLO function. The UVLO function is dependent on the voltage present at the VINS pin (pin 11), and will switch states based on a 1.2V threshold. Hysteresis may be programmed in by means of a resistor connected between HYST pin (pin 12) and VINS pin. Components are determined as follows:

V_{HYST} = HYST Pin Output High (5V typ.)

V_h = Desired Hysteresis

V_{RISING} = Upper Voltage Threshold

Set R3 such that $(V_{HYST} - 1.2)/R3 \le 10uA$

$$R1 = R3 \times (V_h/V_{HYST})$$

$$R2 = 1/[(V_{RISING}/(1.2 \times R1)) - (1/R1) - (1/R3)]$$

Design Example

The following is a design example for a 48W DC/DC Flyback converter using the PD70201 IC. A schematic and parts list of the 48W example can be found in Figures 7.

- **Design Requirements:**

Vmin := 32	Minimum Input Voltage
Vmax := 57	Maximum Input Voltage
Vout := 12	Output Voltage
Pout := 48	Maximum Output Power
Eff := .90	Estimated Efficiency
Fsw := 200k	Switching Frequency
Vaux := 12	Auxillary Output Voltage
Tamb := 70	Ambient Operating Temperature

Flyback operation in DCM is best for output power less than 30W; therefore the design will be a CCM design.

- **Estimated Secondary Diode Drop:**

Synchronous Rectification is used in place of a blocking diode; choose FDMS86322 N-FET.

Sync Transistor: FDMS86322; RDSon = 0.008 at 25°C

$$Iout := \frac{Pout}{Vout} \qquad Iout = 4$$

Kt := 1.58 Multiplier for 100°C

rdson := 0.008·Kt

ddrop := Iout·rdson ddrop = 0.051

- **Transformer Turns Ratio:**

Transformer Turns Ratio is driven by Vmin, Vout, the secondary diode drop, and the controller's maximum duty cycle. Per the datasheet, maximum duty cycle for the PD70201 = 46%.

Dmax := 0.46

$$Tratio := \frac{Vout + ddrop}{Dmax \cdot Vmin} - \frac{Vout + ddrop}{Vmin}$$

Tratio = 0.442 Secondary to Primary (Ns/Np) Turns Ratio

For our design, we will increase the Turns Ratio to 0.444. 0.444 gives a Np/Ns Turns Ratio of 2.25:1, a more practical value.

- **Required Primary Inductance:**

Minimum required primary inductance is based on the desired ripple factor (Krf), which is defined as the percentage of peak to peak inductor ripple current versus inductor average current. This number sets the point in which the primary inductance changes from CCM to DCM operation. A good rule of thumb is to set this number between 0.5 to 1.4. For our design, we will set it to 0.7.

$Krf := 0.7$ Krf is the ratio of inductor ripple to inductor average current

$$Lpri := \frac{Eff \cdot Vmin^2 \cdot \left(\frac{Vout + ddrop}{Tratio}\right)^2}{Krf \cdot Fsw \cdot Pout \cdot \left[Vmin + \left(\frac{Vout + ddrop}{Tratio}\right)\right] \cdot \left[\left(\frac{Vout + ddrop}{Tratio}\right) + Eff \cdot Vmin\right]}$$

$Lpri = 3.054 \times 10^{-5}$

Nominal Primary Inductance (allows for +/- 15%):

$Lnom := Lpri \cdot 1.15$ $Lnom = 3.512 \times 10^{-5}$

- **Transformer Primary/Secondary Currents:**

Average Input Current:

$$Iinavg := \frac{Pout}{Eff \cdot Vmin} \qquad Iinavg = 1.667$$

Average Primary Current:

$$Ipriavg := \frac{Iinavg}{Dmax} \qquad Ipriavg = 3.623$$

Primary Ripple:

$Ipriripple := Ipriavg \cdot Krf$ $Ipriripple = 2.536$

Peak Primary Current:

$$Ipripk := \frac{Ipriripple}{2} + Ipriavg \qquad Ipripk = 4.891$$

Primary Circuit RMS Current:

$$Iprirms := \sqrt{Dmax \cdot \left[Ipripk^2 - (Ipripk \cdot Ipriripple) + \frac{Ipriripple^2}{3}\right]}$$

$Iprirms = 2.507$

Secondary Circuit RMS Current:

$$Isecpk := \frac{Ipripk}{Tratio} \qquad Isecpk = 11.016$$

$$Isecrms := \sqrt{(1 - Dmax) \cdot \left[Isecpk^2 - \left(Isecpk \cdot \frac{Ipriripple}{Tratio}\right) + \frac{Ipriripple^2}{Tratio^2 \cdot 3}\right]}$$

$Isecrms = 6.118$

- **Transformer Specifications:**

Based on the calculations above, the following can be given to a transformer manufacturer for transformer fabrication:

Primary Voltage Range:

$Vmin = 32$

$Vmax = 57$

Secondary Voltage & Power:

$Vout = 12$ $Pout = 48$

Auxilliary Voltage & Power:

$Vaux = 12$ Paux = 1.2

$Fsw = 2 \times 10^5$ Switching Frequency

$$Dmin := \frac{Vout + ddrop}{Vout + ddrop + Tratio \cdot Vmax} \qquad Dmin = 0.323$$

Maximum Primary Operating Volt-Seconds:

$$Vsecmax := \frac{Dmin \cdot Vmax}{Fsw} \qquad Vsecmax = 9.193 \times 10^{-5}$$

Open Circuit Primary Inductance (+/- 15%):

$Lnom = 3.512 \times 10^{-5}$

Turns Ratio:

$$Naux := \frac{Vaux}{Vout}$$ Turns Ratio Calculation for Aux Winding

Nsec/Npri: $Tratio = 0.444$ Npri/Nsec: $\frac{1}{Tratio} = 2.252$

Naux/Nsec: $Naux = 1$

Winding Currents:

$Iprirms = 2.507$ $Ipriavg = 3.623$

$Ipripk = 4.891$ $Isecrms = 6.118$

- **Primary Clamp Equations:**

The maximum transformer primary voltage seen across the V_{DS} of the primary transistor during the off period will be greater than the maximum input voltage by a factor of the secondary voltage reflected by the transformer's turns ratio *plus* the voltage generated by the leakage inductance of the primary. Because of this, a suitable clamp is required to insure the primary voltage does not exceed the transistor's maximum V_{DS}. There are many types of clamps available to the designer; each has it's merits and drawbacks. For this design the more common RCD clamp will be used. An example of an RCD clamp is outlined in

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figure 7. The first step is to select a maximum V_{DS} transistor rating. The reflected voltage is found:

Reflected Mosfet Drain Voltage:

$$Vd := \left(\frac{Vout + ddrop}{Tratio}\right) + Vmax \qquad Vd = 84.141$$

Vd=the reflected voltage across the transistor

Based on the above equation, the transistor selection will need to have a V_{DS} rating considerably larger than 85V. 100V does not leave margin for voltage overshoot, and would require significant power loss to achieve, so a 150V transistor will be used.

Next, the maximum clamp voltage and a clamping coefficient is calculated using the chosen V_{DS} rating de-rated by 15%. The clamping coefficient is simply the ratio

Clamp Voltage Limit (with BVdss derated):

$$Vclamp := BVdss \cdot 0.85 - Vd \qquad Vclamp = 43.359$$

Clamp Coeffient based on selected Turns Ratio:

$$Kccalc := \frac{Tratio \cdot Vclamp}{(Vout + ddrop)} \qquad Kccalc = 1.598$$

Maximum Transistor Stress Voltage:

$$Vstress := Vd + Vclamp \qquad Vstress = 127.5$$

$$BVdss \cdot 0.85 = 127.5$$

Using Leakage inductance estimated at 1% of the primary inductance, and the values calculated above, the final RC values are calculated:

Estimated Leakage Inductance:

$Lleak := Lnom \cdot 0.01$ Leakage is set at 1% of total primary inductance

Clamp Voltage Limit:

$Vclamp = 43.359$

Desired Clamp Capacitor Ripple Voltage:

$$Vcripple := Vclamp \cdot 0.1$$

Clamp Coefficient:

$$Kccalc = 1.598$$

Resistor Calculation:

$$Rclmp := \frac{(Kccalc - 1) \cdot \left[2 \cdot Kccalc \cdot (Vout + ddrop)^2\right]}{Tratio^2 \cdot Fsw \cdot Lleak \cdot Ipripk^2}$$

$$Rclmp = 837.011$$

Resistor Power Dissipation:

$$Prclmp := 0.5 \cdot Fsw \cdot Lleak \cdot Ipripk^2 \cdot \frac{Kccalc}{Kccalc - 1}$$

$$Prclmp = 2.246$$

Capacitor Calculation:

$$Cclmp := \frac{Kccalc \cdot (Vout + ddrop)}{Tratio \cdot Rclmp \cdot Fsw \cdot Vcripple}$$

$$Cclmp = 5.974 \times 10^{-8}$$

Clamp Current Calculation:

$$Trst := \frac{Tratio \cdot Lleak \cdot Ipripk}{Tratio \cdot Vclamp - (Vout + ddrop)}$$

Leak L Reset Time: $Trst = 1.059 \times 10^{-7}$

$$Iclmprms := Ipripk \cdot \sqrt{\frac{Trst \cdot Fsw}{3}}$$

$$Iclmprms = 0.411$$

Based on the above equations, the clamp resistor will need to be 3 X 2.7K Ohm, 1W 5% resistors in parallel. The capacitor will need to be a .068µF, 100V capacitor.

Using the clamp current and maximum stress voltage the diode is selected. A fast diode is desired.

$$Vstress = 127.5$$

$$Iclmprms = 0.411$$

A 200V, 1A ES1D Diode is selected.

Note that the above component selections will require final tweaking at the prototype stage.

- **Primary FET Requirements:**

  The primary FET will be chosen based on maximum primary RMS current, and maximum V_{DS} stress. Note that the maximum stress has already been accounted for; we will chose a 150V FET based on the primary RMS Current and RDSon.

  $Iprirms = 2.507$

  A FDMS86200 FET by Fairchild has a V_{DS} rating of 150V, maximum continuous I_{DS} rating of 9.6A, and a specified RDSon of 18mΩ at 25°C.

- **Primary FET Power Dissipation:**

Selected Transistor: FDMS86200

Chosen RDSon (at 100°C): $RDSon := .03$

Chosen θja: $\theta ja := 50$

Chosen Ambient T: $Tamb = 70$

Chosen Max. Junction T: $Tj := 100$

Transistor BVdss: $BVdss = 150$

Transistor Power Limit:

$$Plimit := \frac{Tj - Tamb}{\theta ja} \qquad Plimit = 0.6$$

Transistor Qgs2: $Qgs := 2.9n$

Transistor Qgd: $Qgd := 7.7n$

Transistor gate resistance: $Rg := 1.2$

Transistor gate voltage at start of miller effect: $Vgsmiller := 3.9$

Transistor gate threshold voltage: $Vth := 2.5$

Transistor gate drive max voltage: $Vcc := 12$

Gate drive on resistance: $Rhi := 10$

Gate drive off resistance: $Rlo := 5$

Rising Gate Current and Turn-on Time:

$$Ig1 := \frac{Vcc - [0.5\cdot(Vgsmiller + Vth)]}{Rhi + Rg} \qquad Ig1 = 0.78571$$

$$Ig2 := \frac{Vcc - Vgsmiller}{Rhi + Rg} \qquad Ig2 = 0.72321$$

$$\Delta ton := \frac{Qgs}{Ig1} + \frac{Qgd}{Ig2} \qquad \Delta ton = 1.43378\times 10^{-8}$$

Falling Gate Current and Turn-off Time:

$$Igf1 := \frac{Vcc - [0.5\cdot(Vgsmiller + Vth)]}{Rlo + Rg} \qquad Igf1 = 1.41935$$

$$Igf2 := \frac{Vcc - Vgsmiller}{Rlo + Rg} \qquad Igf2 = 1.30645$$

$$\Delta toff := \frac{Qgs}{Igf1} + \frac{Qgd}{Igf2} \qquad \Delta toff = 7.93701\times 10^{-9}$$

Valley Current:

$$Ivalley := Ipriavg - \frac{Ipriripple}{2} \qquad Ivalley = 2.30496$$

Operational Primary RMS Current:

$Iprirms = 2.48022$

Conduction Loss:

$$Pcond := Iprirms^2\cdot RDSon \qquad Pcond = 0.18454$$

Turn On Switch Loss:

$$Pswon := \frac{Ivalley\cdot\left(Vmin + \frac{Vout + ddrop}{Tratio}\right)\Delta ton}{6}\cdot Fsw$$

$Pswon = 0.06515$

Turn Off Switch Loss: $Vclamp = 43.3591$

$$Pswoff := \frac{Ipripk\cdot(Vmin + Vclamp)\cdot\Delta toff}{2}\cdot Fsw \qquad Pswoff = 0.28634$$

Total Power Loss:

$$Plosstot := Pcond + Pswon + Pswoff \qquad Plosstot = 0.53603$$

In the above calculations, R_{DS}on is derated at 100°C. Values for Vth, Qgd and Rg are available in most MOSFET datasheets. Qgs2 is the switching gate charge; if not specified, it may be estimated using the Vgs vs Gate charge graph (found in all MOSFET datasheets) by determining the equivalent charge between Vth and Vgsmiller.

- **Synchronous FET Requirements:**

  The output synchronous FET is chosen by calculating the maximum DS voltage created during the primary on time (sync FET is off), and the maximum secondary RMS current. To de-rate the FET, DS voltage is increased by 30% and DS current is increased by 50% for proper FET selection.

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Maximum Primary Reflected Voltage across FET:

$Vsecref := Vmax \cdot Tratio + Vout$ $Vsecref = 37.308$

$Vsecref \cdot 1.3 = 48.5$

Maximum FET Current (de-rated):

$Irect := Isecrms \cdot 1.5$ $Irect = 9.177$

A FET is chosen with a V_{DS} of 60V or higher, and a current capability of 9 Amps or greater. Chosen is the FDMS86322. This FET has an R_{DS}on (25°C) of 0.007 at 13A, and a maximum V_{DS} of 80V.

- **Synchronous FET Power Dissipation:**

$ddropcalc := Isecrms \cdot rdson$

$ddropcalc = 0.077$ Voltage drop across the transistor

$rdson = 0.013$ Rdson at 100°C

Rectifier Power Loss:

$Prect := Isecrms \cdot ddropcalc$ $Prect = 0.473$

Rectifier Junction Temp:

$Tamb = 70$

$Thetajarect := 50$ Package theta ja

$Jtrect := Thetajarect \cdot Prect + Tamb$ $Jtrect = 93.654$

- **Sense Resistor Calculation:**

The sense resistor is chosen based on the maximum peak current expected, and the voltage threshold where the controller starts to limit current. For the PD70201, the current limit threshold voltage is 1.2V with a gain of 5 current sense amplifier, so the resistor is sized such that the operating peak primary current develops at approximately 90% of this value. 1.1V is approximately 90% of 1.2V.

$Vthreshold := 1.1$

Sense Resistor Value (accounts for X5 gain):

$$Rsns := \frac{Vthreshold}{Ipripk \cdot 5}$$ $Rsns = 0.04596$

$Prsns := Iprirms^2 \cdot Rsns$ $Prsns = 0.2827$

The above takes into account Av = 5 for the current sense amplifier.

A 47mΩ 1/2W resistor will meet the requirment.

- **Output Capacitor Calculation:**

The output filter capacitor is chosen based on the desired output voltage ripple, output voltage undershoot (droop) during load step, and the RMS ripple current the capacitor must endure.

Desired Output Ripple: $Vripple := 0.1$

Desired Closed-Loop Bandwidth: $Fc := 4k$

Desired Output Droop Load Step: $Vdroop := 0.6$

Load Step: $Istep := Iout \cdot 0.9$

$Isecpk = 11.016$

$$Ioutavg := \frac{Iinavg}{Tratio}$$ $Ioutavg = 3.754$

$Isecrms = 6.118$

$Icoutrms := \sqrt{Isecrms^2 - Ioutavg^2}$ $Icoutrms = 4.831$

$$Cesr := \frac{Vripple}{Isecpk}$$ $Cesr = 9.077 \times 10^{-3}$

$$Cout := \frac{Istep}{2 \cdot \pi \cdot Vdroop \cdot Fc}$$ $Cout = 2.387 \times 10^{-4}$

Chosen Output Capacitor:

$Coutact := 360u$

$Cesract := 0.008$

For the output capacitor, we will choose 2x Sanyo OSCON 25SVPF180M capacitors in parallel. These are 180µF, 25V capacitors with an ESR of 16m Ohm and a maximum ripple capability of $4.65A_{RMS}$.

- **Input Filter Calculation:**

The input filter is used to reduce the voltage fluctuations seen at the DC/DC converter input due to the large peak currents involved. There are several approaches to providing an input filter; the input filter can consist of a simple input capacitor (usually several capacitors in parallel due to the large ripple currents), or can be a more complex LC filter. For this design, we will choose an LC filter as our input filter. The input to the LC filter will be a common aluminum electrolytic; the output of the LC filter will consist of smaller ceramic capacitors to absorb the ripple current.

Our design requires the ripple voltage on VPP to be 50mV or less. We will first choose a suitable ripple voltage at the primary, and then size the input capacitor to achieve that ripple voltage. The input capacitor will need to absorb most of the primary ripple current, so it's ripple handling capability is critical. Ceramic capacitors have very good ripple current capability and are a good choice for the input capacitor for this design.

First we will determine the maximum ripple current seen by the capacitor, and use this use this current to select a suitable input capacitor based on our selected primary ripple of 320mV:

$$Cinputrms := \sqrt{Iprirms^2 - Iinhigh^2}$$

$$Cinputrms = 1.873$$

$$Vinripple := 0.32$$

$$Cmin := \frac{Cinputrms \cdot Dmax}{Fsw \cdot Vinripple} \qquad Cmin = 1.34888 \times 10^{-5}$$

For this design, we will choose 4x 4.7µF 100V ceramic capacitors in parallel. 4 capacitors are chosen to account for capacitor tolerance variation. The ceramic capacitors chosen (1812 case size) have a ripple capability at 100 kHz of greater than 2A for a 20°C case temperature rise.

The capacitors chosen will meet more than this requirement.

Next, we will determine the voltage developed across our chosen input capacitors:

$$Cminact := 15u$$ Actual capacitance - 20% tolerance

$$Cinesr := 1.2m$$

$$deltavin := \frac{Cinputrms \cdot Dmax}{Fsw \cdot Cminact} + Ipriavg \cdot Cinesr$$

$$deltavin = 0.29202$$

Next we will chose an inductor based on the desired attenuation. For this design, we will attenuate the input current by 40dB:

Filter Attenuation Desired:

$$A := 0.01$$

Filter Cutoff Frequency for Required Attenuation:

$$Fo := \sqrt{A} \cdot Fsw \qquad Fo = 2 \times 10^4$$

Required Lin vs Cin:

$$Lin1 := \frac{1}{4\pi^2 \cdot Fo^2 \cdot Cminact} \qquad Lin1 = 4.22172 \times 10^{-6}$$

$$InputfilterIrms := A \cdot Cinputrms \qquad InputfilterIrms = 0.01837$$

For this design we will use a 4.7µH inductor. This inductor needs to handle the maximum Primary RMS current at low line, and should be sized with a minimum DCR to increase efficiency.

Finally, we will need to check our filter for stability. In order for the filter to be stable, the filter output impedance must be less than the input impedance of the DC-DC converter. The input impedance is calculated at DC for a first order check. The filter output impedance is compared at two frequency points: DC (which is simply the DCR of the inductor), and at the resonant point where peaking occurs due to the filter Q:

$$Zinsmpsdc := \frac{Vmin^2 \cdot Eff}{Pout}$$

$$Zinsmpsdc = 19.2$$ Converter Input Impedance at DC

$$Zoutfilterdc := DCR$$

$$Zoutfilterdc = 0.045$$ Filter Output Impedance at DC

Filter Output Impedance at resonant point:

$$Zoutfiltermax := \sqrt{\frac{(Cinact \cdot ESR^2 + Linact) \cdot (Cinact \cdot DCR^2 + Linact)}{Cinact^2 \cdot (ESR + DCR)^2}}$$

$$Zoutfiltermax = 6.804$$

The calculated output impedance of our filter at DC is 45mΩ; at the resonant point it is 6.8Ω. Both of these values are less than the Converter DC input impedance of 19.2Ω; our filter values will not cause stability issues.

- **Control Loop Calculations:**

  Control loop calculations are made by determining the modulator and filter gain and phase at the desired crossover frequency, and then selecting feedback components to increase

(or decrease) the gain for unity gain at the crossover point. First, the modulator and filter must be evaluated to determine the frequency location of the Right Hand Plane Zero (inherent in CCM Flyback designs), and assure that the chosen crossover frequency is less than 20% of that frequency:

Calculation of Right Hand Plane Zero:

$$Rload := \frac{Vout}{Iout}$$

$$Fzrhp := \frac{(1 - Dmax)^2 \cdot Rload}{2\pi \cdot Dmax \cdot Lnom \cdot Tratio^2} \qquad Fzrhp = 4.372 \times 10^4$$

$$Fzrhp \cdot 0.2 = 8.744 \times 10^3$$ This number must be greater than the proposed crossover frequency.

Our proposed crossover frequency is 4kHz; we have plenty of margin.

The modulator and filter gain-phase of our regulator utilizes the following transfer function:

$$Kcc := \frac{Ipripk}{1.2}$$ Current Control Factor

$$\omega z1 := \frac{1}{Cesract \cdot Coutact}$$ Capacitor ESR zero

$$\omega z2 := \frac{(1 - Dmax)^2 \cdot Rload}{Dmax \cdot Lnom \cdot Tratio^2}$$ RHP zero

$$\omega p := \frac{(1 + Dmax)}{Rload \cdot Coutact}$$ Load pole

$$Vro := \frac{Dmax}{1 - Dmax} \cdot Vmin$$ Reflected output voltage

$$H(s) := \frac{Kcc \cdot Rload \cdot Vmin \cdot Tratio^{-1}}{2 \cdot Vro + Vmin} \cdot \frac{\left(1 + \frac{s}{\omega z1}\right) \cdot \left(1 - \frac{s}{\omega z2}\right)}{1 + \frac{s}{\omega p}}$$

Solving for H at the crossover frequency:

$$Gxo := 20 \cdot \log\left(\left|H(2 \cdot \pi \cdot i \cdot Fc)\right|\right)$$

$$Gxo = -5.179$$ Gain at crossover point (dB)

$$Pxo := \arg(H(2 \cdot \pi \cdot i \cdot Fc)) \cdot \frac{180}{\pi}$$

$$Pxo = -88.008$$ Phase shift at crossover point (Degrees)

Once the gain and phase are known, the loop must be closed such that the gain at the crossover frequency is equal to 1 (0dB), and the phase margin is greater than 45°.

In most isolated designs, the feedback loop is closed by means of an optocoupler which bridges the primary/secondary isolation barrier. The optocoupler is chosen to account for the isolation requirements and the input/output current gain (noted as a percentage, "CTR", which translates to the percentage of input LED current transferred to the output). For our design, the optocoupler will drive the PD70201's COMP pin directly. The optocoupler components are selected as follows:

Optocoupler Calculations:

$Vf := 1$ Optocoupler: NEC PS2711-1-M-A

$Vdd := 5.0$ Vdd = PD70201's VL typical output voltage

$Rpullup := 1k$ Rpullup added to increase Optocoupler pole frequency

$Vcesat := 0.3$

$Tf := 5u$ These values are fall time test conditions found in the datasheet; used for estimating the pole capacitance; Tf = fall time, Rl = test load.

$Rl := 100$

$CTRmax := 2.00$

$CTRmin := 1.00$

$$Ioptomin := \frac{Vdd - 1.2}{Rpullup} \qquad Ioptomin = 3.8 \times 10^{-3}$$

$$Ioptomax := \left(\frac{Vdd - Vcesat}{Rpullup}\right) + 500u \qquad Ioptomax = 5.2 \times 10^{-3}$$

Ioptomin assumes 1.2 max regulation input for PD70201; Ioptomax adds maximum Error Amp Comp pin current capability.

Optoisolator Characteristic Pole Capacitor:

$$Cpole := \frac{Tf}{2.2 \cdot Rl} \qquad Cpole = 2.273 \times 10^{-8}$$

$$\omega popto := \frac{1}{Rpullup \cdot Cpole} \qquad fpopto := \frac{\omega popto}{2 \cdot \pi} = 7.003 \times 10^3$$

$$Iledmin := \frac{Ioptomin}{CTRmax} \qquad Iledmin = 1.9 \times 10^{-3}$$

On the secondary side, the optocoupler must be driven with an error amplifier that regulates the output voltage. Most designs utilize a common TL431 shunt regulator, due to it's ability to regulate without requiring additional input power for operation. The compensation components, as well as the DC setting resistors will be placed around the TL431. First, the DC setting resistors are calculated:

TL431 Calculations:

Reference Resistors:

$Vref := 2.5$

$Iref := 4u$

$Iresistordivider := 1m$

$Rlowercalc := \frac{Vref}{Iresistordivider}$ $Rlowercalc = 2.5 \times 10^{3}$

$Rlower := 2.49k$ Actual resistor used

$Ruppercalc := \frac{(Vout - Vref)}{Iresistordivider + Iref}$ $Ruppercalc = 9.462 \times 10^{3}$

$Rupper := 9.53k$ Actual resistor used

$Voutcalc := \left(\frac{Vref}{Rlower} + Iref\right) \cdot Rupper + Vref$ $Voutcalc = 12.106$

Next, the compensation components are selected:

431 Compensation (Type Two):

$Gxo = -5.179$ Modulator and Filter gain at Fc (dB)

$Gc := 10^{\left(\frac{Gxo}{20}\right)}$

$Gc = 0.551$ Modulator and Filter gain at FC (mag)

$G431 := \frac{1}{Gc} = 1.815$ Required feedback gain

$fz431 := 54$ Compensation Zero; set to 1/4 Load Pole

$fp431 := 14k$ Compensation Pole; set to 1/4 ESR zero

$Ibias := 2m$ 431 bias for regulation

$CTRtyp := 1.5$ Optoisolator CTR typical

$Rledcalc := \frac{CTRtyp \cdot Rpullup}{G431}$

$Rledcalc = 826.267$ LED Resistor

$Czcalc := \frac{1}{2 \cdot \pi \cdot Rupper \cdot fz431}$

$Czcalc = 3.093 \times 10^{-7}$ Calculated Zero Capacitor

$Cpcalc := \frac{1}{2 \cdot \pi \cdot Rpullup \cdot fp431}$

$Cpcalc = 1.137 \times 10^{-8}$ Calculated Pole Capacitor

$Cpole = 2.273 \times 10^{-8}$ Optoisolator Pole Capacitor

Actual Compensation Values Used:

$Rled := 825$

$Cz := 330n$ If Cpole less than 5x Cpcalc, use Cpole in the Transfer Function

$Cp := 22.7n$

Finally, the chosen values are used in the TL431/optocoupler Transfer Function:

TL431/Optoisolator Transfer Function:

$$G(s) := -\left(\frac{s \cdot Rupper \cdot Cz + 1}{s \cdot Rupper \cdot Cz}\right) \cdot \left(\frac{1}{1 + s \cdot Rpullup \cdot Cp}\right) \cdot \frac{Rpullup}{Rled} \cdot CTRtyp$$

Bias Resistor:

$$Rbias := \frac{Rled \cdot Iledmin + Vf}{Ibias}$$

$Rbias = 1.284 \times 10^{3}$

The two functions are multiplied together to achieve the overall loop gain:

$Gtot431(s) := H(s) \cdot G(s)$

A Bode Plot of the overall loop gain is shown in Figure 6.

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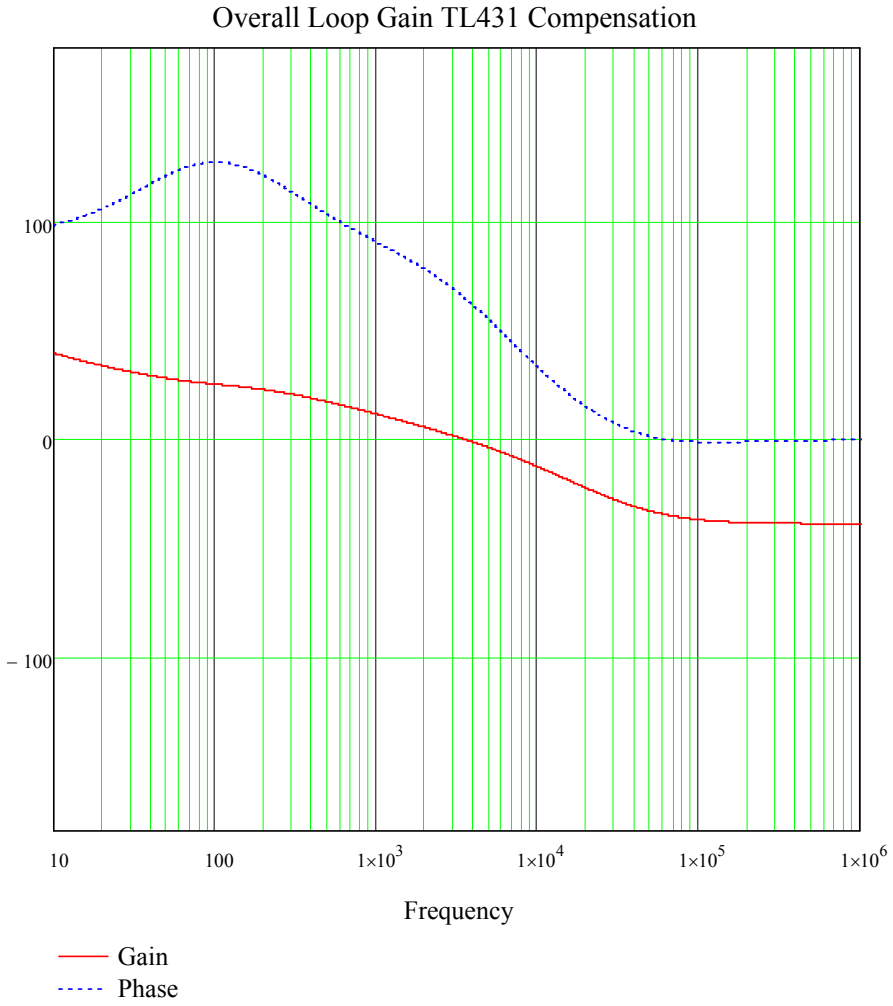

Figure 6. Loop Bode Plot

Synchronous Gate Drive:

The PD70201 provides a dedicated output driver for a Synchronous FET. This output is available on the SG pin (pin 25). To adhere to the isolation requirements, the SG output is transformer coupled to the Synchronous FET. A coupling capacitor is required in series with the primary to reset the magnetizing inductance. The transformer will saturate without it. The LC tank circuit formed by the coupling capacitor and the transformer magnetizing inductance can generate oscillations during sudden changes in duty cycle. A damping resistor in series with the coupling capacitor should be used to damp oscillations. On the secondary side, a DC restoration and fast gate turn-off circuits are provided to keep the gate drive voltage constant over varying duty cycle, and to insure fast transistor turn off.

Referencing Figure 9, DC restoration is provided via Capacitor C20, and Diode D7. The fast turn-off circuit consists of R14, Q3 and D6. Resistor R11 limits the synchronous MOSFET's turn-on rate of rise, and is optional (can be used to limit EMI).

When selecting the components for the synchronous FET gate drive, first the transformer should be selected based on the maximum volt-microseconds of the SG pin drive output. Maximum volt-microseconds is calculated:

$$VCCmax := 15$$

$$Dmin = 0.323 \quad \text{Duty Cycle at High Line}$$

$$Vgdusecmax := \frac{(1 - Dmin) \cdot VCCmax}{Fsw} \qquad Vgdusecmax = 5.081 \times 10^{-5}$$

Because of the capacitor in series with the primary, the drive voltage is bipolar. The calculated maximum volt-microsecond value may divided by 2 for transformer selection due to the bipolar drive.

The magnetizing inductance will affect the transient response of the isolated drive signal. Generally a lower inductance will produce a faster response time. Our selected transformer has a magnetizing inductance of 296uH.

Once the transformer is selected, the two coupling capacitor values are calculated. The coupling capacitor values will determine the amount of ripple voltage seen at the gate of the synchronous FET; total gate ripple will be the sum of the individual capacitor ripple voltages.

To size the coupling capacitors, first determine the maximum ripple we will allow each capacitor to contribute to the overall gate ripple voltage. (~1% of the maximum gate drive voltage is chosen for our design). Next, factor in the values for synchronous FET gate charge, and the current flowing in the pull down resistor, R14:

$Qg := 31n$ FDMS86322 Gate Charge

$Vdrv := 12$ Nominal Gate Drive Voltage

$\Delta Vc1 := 0.1$ Desired Ripple Across Primary Cap

$\Delta Vc2 := 0.1$ Desired Ripple Across Secondary Cap

$Rgs := 1k$ Gate Resistor

$D := 0.95$ Off Time Duty Cycle (increased to account for transients)

$Lm := 296u$ Magnetizing Inductance

$Fsw = 2 \times 10^{5}$ Switching Frequency

$$Cc2 := \frac{Qg}{\Delta Vc2} + \frac{(Vdrv - 0.7)\cdot D}{\Delta Vc2 \cdot Rgs \cdot Fsw}$$

$Cc2 = 8.467 \times 10^{-7}$ Secondary Side Capacitor

Our design will use a 1µF capacitor on the secondary side. On the primary side:

$$Cc1 := \frac{Qg}{\Delta Vc1} + \frac{(Vdrv - 0.7)\cdot D}{\Delta Vc1 \cdot Rgs \cdot Fsw} + \frac{Vdrv \cdot \left(D^2 - D^3\right)}{\Delta Vc1 \cdot 4 \cdot Lm \cdot Fsw^2}$$

$Cc1 = 9.611 \times 10^{-7}$ Primary Side Capacitor

We will use a 1uF capacitor on the primary side.

Once the primary side capacitor is determined, the series damping resistor is found:

$Cc1act := 1.0u$ Primary Side Capacitor

$$\sqrt{\frac{Lm}{Cc1act}} \cdot 2 = 34.409$$

A total series resistance of 34Ω is required. This resistance includes the PD70201's drive resistance of 10Ω, meaning an additional resistance of 24Ω must be added. Resistor power is calculated assuming the transformer magnetizing current is dominant:

$$drcurrentpk := \frac{Vdrv}{Lm} \cdot \left[\frac{(1 - Dmin)}{Fsw}\right] \qquad drcurrentpk = 0.137$$

$$drcurrentrms := drcurrentpk \sqrt{\frac{(1 - Dmin)}{3}} \qquad drcurrentrms = 0.065$$

$drvpwr := drcurrentrms^2 \cdot 24$

$drvpwr = 0.102$ Calculated Resistor Power

Our chosen resistor is 24Ω, 1W. This is a standard value.

The following pages contain a schematic and bill of material for the above example.

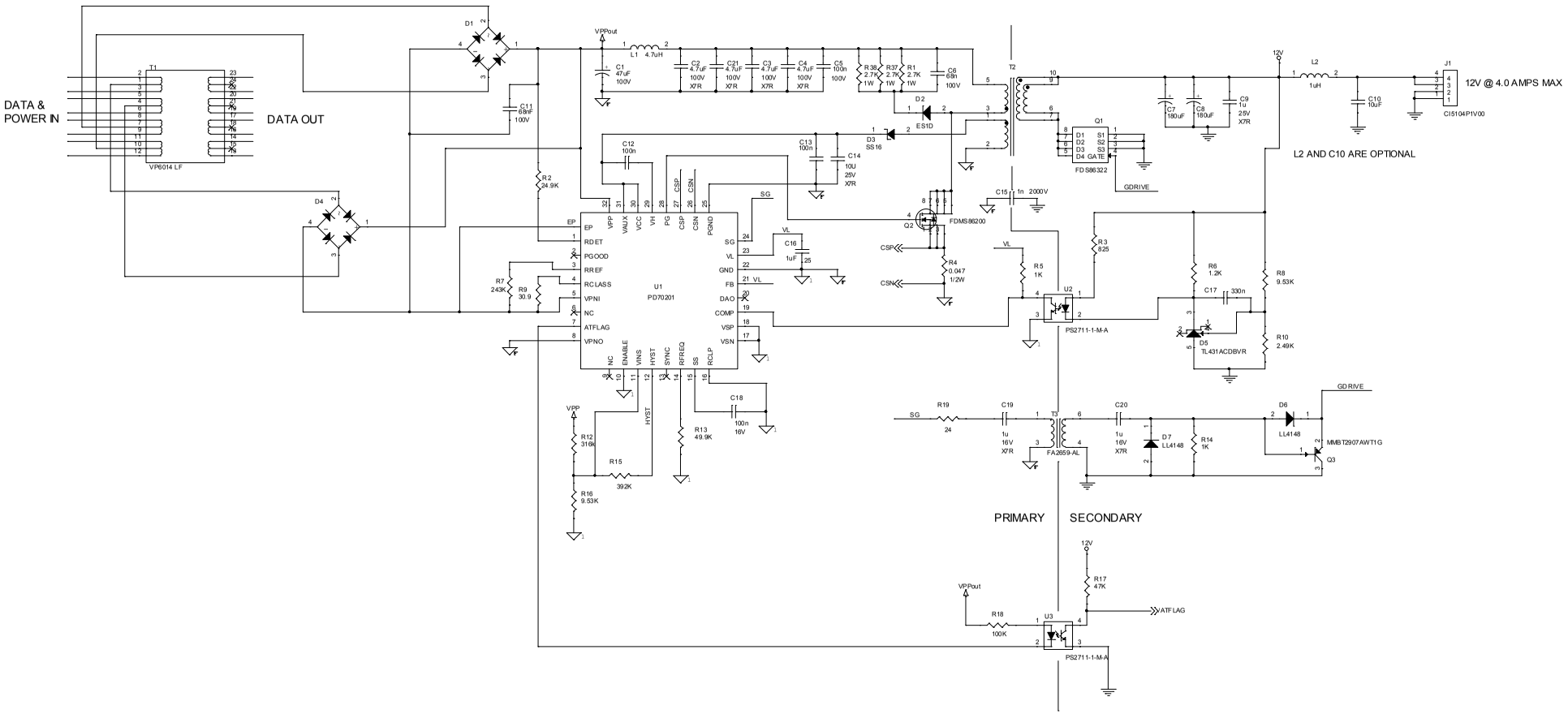

Figure 7. PD70201 48W Example Design

Bill of Materials - PD70201 Example Design

Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
1	1	C1	CAP ALU 47µF 100V 20%	Panasonic	EEU-FC2A470
2	4	C2,C3,C4, C21	CAP CER 4.7µF 100V 20% X7R ^1210 SMT	CAPAX	1210X475J101SNT
3	1	C5	CAP CRM 100nF 100V 10%^^X7R 1206 SMT	EPCOS	B37872K1104K62
4	2	C7,C8	Capacitor, 180µF, 16m Ohm ESR, 4.65A ripple current	Sanyo	25SVPF180M
5	1	C9	CAP CRM 1µF 25V 10% X7R, 1206	TAIYOYUDEN	TMK316B7105ML-T
6	1	C10	CAP X7R 10µF 16V 10% 1206	TDK	C3216X7R1C106K
7	2	C6,C11	CAP CRM 68nF 100V 10%^^X7R 1206 SMT	AVX	12061C683KAT2A
8	2	C12,C13	CAP CRM 100nF 25V 10%^^X7R 0805 SMT	Murata	GRM216R71E104KA01
9	1	C14	Capacitor, X7R, 10µF, 25V, 20% 1206	TAIYOYUDEN	TMK316AB7106KL-T
10	1	C15	CAP CRM 1nF/2000V 10%++X7R 1206 SMT	AVX	1206GC102KAT1A
11	1	C16	Capacitor,X7R, 1µF, 25V, 10% 0603	Murata	GRM188R71E105KA12D
12	1	C17	Capacitor, X7R, 330nF, 16V, 10% 0603	TAIYOYUDEN	EMK107B7334KA-T
13	1	C18	Capacitor, X7R, 100nF, 16V, 10% 0603	TAIYOYUDEN	EMK107B7104KA-T
14	1	C19	CAP CRM 1µF 16V 10%^^X7R 0603 SMT^^	Vishay	VJ0603Y105KXJT
15	1	C20	CAP CRM 1µF 16V 10%^^X7R 0603 SMT^^	Vishay	VJ0603Y105KXJT
16	2	D1,D4	DIO bridge 100V 2.0A, SDB-1 case	Fairchild	DF01S
17	1	D2	DIO FAST SWI 200V 1A	Fairchild	ES1D
18	1	D3	Diode Schottky 1A 60V SMA	Fairchild	SS16
19	1	D5	IC Adj Prec Shunt Reg 2.5V ^^1% SOT-23-5 SMT	Texas Instruments	TL431ACDBVR
20	1	D6	DIO FAST SWI 75V 300mA^^4nS SOD80C MiniMELF	Vishay	LL4148
21	1	D7	DIO FAST SWI 75V 300mA^^4nS SOD80C MiniMELF	Vishay	LL4148
22	1	J1	PIN HEADER 4 PIN 0.156"^^TIN, WITH LOCKING WALL	CviLux	CI5104P1V00
23	1	L1	INDUCTOR PWR 4.7µH 20%, 45mΩ, 2.2A	Wurth	7440700047
24	1	L2	Power Inductor 1µH SMT	Wurth	7440690010
25	1	Q1	FET, N-Channel, 80V, 13A	Fairchild	FDS86322

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

Bill of Materials - PD70201 Example Design

Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
26	1	Q2	FET, N-Channel, 150V, 9A	Fairchild	FDMS86200
27	1	Q3	TRN PNP 60V 600mA SOT323 SMT 250mW MMBT2907AW^	ON Semiconductor	MMBT2907AWT1G
28	3	R1,R37,R38	RES 2.7K Ohms, 1W 5%, 2512 SMT	Panasonic	ERJ-1TYJ272U
29	1	R2	RES TK FLM 24.9K 100mW1% 0805	Panasonic	ERJ6EKF2492V
30	1	R3	RES 825, 62.5mW 1%^^0603 SMT MTL FLM	Panasonic	ERJ3EKF8250V
31	1	R4	RES .047 OHM 1/2W 1% 2010 SMD	Panasonic	ERJL1DKF47MU
32	1	R5	RES 1.00K 62.5mW 1%^^0603 SMT MTL FLM	Panasonic	ERJ3EKF1001V
33	1	R6	RES TCK FLM 1.2K 62.5mW 1%^^0603 SMT	Samsung	RC1608F1201CS
34	1	R7	RES 243K 62.5mW 1%0603 SMT MTL FLM	Panasonic	ERJ3EKF2433V
35	1	R8	RES 9.53K 0.1W 1%^^0603 SMT MTL FLM	Panasonic	ERJ3EKF9531V
36	1	R9	RES 30.9 62.5mW 1%0603 SMT MTL FLM	Panasonic	ERJ3EKF30R9V
37	1	R10	RES 2.49K 62.5mW 1%^^0603 SMT MTL FLM	Vishay	CRCW06032K49FKEA
38	1	R11	Resistor, 4.7 Ohm, 5% 1/16W 0603	Panasonic	ERJ3GEYJ4R7V
39	1	R12	RES 316K 62.5mW 1%0603 SMT MTL FLM	Panasonic	ERJ3EKF3163V
40	1	R13	RES 49.9K 62.5mW 1% 0603^^SMT	Panasonic	ERJ3EKF4992V
41	1	R14	RES TCK FLM 10K 125mW 1%^^0805 SMT	Panasonic	ERJ3GEYJ104V
42	1	R15	RES 392K 125mW 1%^^0805 SMT MTL FLM	Rohm	MCR10EZHFX3923
43	1	R16	RES TK FLM 12.4K 125mW^^1% 0805	Rohm	MCR10EZPF 1242
44	1	R17	Resistor, 47K, 5%, 1/16W 0603	Panasonic	ERJ3GEYJ473V
45	1	R18	Resistor, SMT 100K, 5%, 1/16W 0805	Panasonic	ERJ6GEYJ104V
46	1	R19	Resistor, SMT, 24Ω, 5%, 1/4W, 1206	Panasonic	ERJ8GEYJ240U
47	1	T1	1000 BASE –T SINGLE PORT VOICE OVER IP MAGNETICS MODULE SMT	BOTHHAND	VP6014 LF
48	1	T2	48W transformer		Custom build
49	1	T3	Transformer, Gate Drive, 1:1 turns ratio, 269µH	Coilcraft	FA2659-AL
50	1	U1	IC, POE PD Front End and PWM Controller	Microsemi	PD70201
51	2	U2,U3	Optoisolator, CTR = 100 to 200	NEC	PS2711-1-M-A

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Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

Revision History

Revision Level / Date	Para. Affected	Description
0.2/ May, 2011		Originate

For support contact: sales_AMSG@microsemi.com

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