

65 kW Transient Voltage Suppressor

- High Reliability controlled devices
- Thru hole mounting
- Unidirectional (A) and Bidirectional (CA) construction
- Selections for 48 V to 75 V standoff voltages (V_{WM})

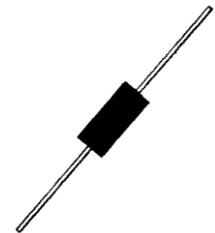
DEVICES

MRT65KP48A thru MRT65KP75CA, e3

LEVELS
 M, MA, MX, MXL

FEATURES

- High reliability controlled devices with wafer fabrication and assembly lot traceability
- 100 % surge tested devices
- Suppresses transients up to 65 kW @ 6.4/69 μ s
- Fast response with less than 5ns turn-on time
- Preferred 65kW TVS for aircraft power bus protection
- Optional upscreaming available by replacing the M prefix with MA, MX or MXL. These prefixes specify various screening and conformance inspection options based on MIL-PRF-19500. Refer to [MicroNote 129](#) for more details on the screening options.
- Moisture classification is Level 1 with no dry pack required per IPC/JEDEC J-STD-020B
- RoHS Compliant devices available by adding "e3" suffix
- 3σ lot norm screening performed on Standby Current I_D



CASE 5A

APPLICATIONS / BENEFITS

- Pin injection protection per RTCA/DO-160F up to Level 5 for Waveform 4 (6.4/69 μ s) and up to Level 3 for Waveform 5A (40/120 μ s) at 70 °C
- Compatible with "abnormal surge voltage (dc)" in 16.6.2.4 (Category A, B, and Z) of RTCA/DO-160F
- The MRT65KP48A is designed for Category A in protecting 80 V components**
- The MRT65KP54A or 60A is designed for Category B in protecting 90 V or 100 V components**
- The MRT65KP75A is designed for Category Z in protecting 125 V components**

** including switching transistors, MOSFETS & IGBTs in offline switching power supplies

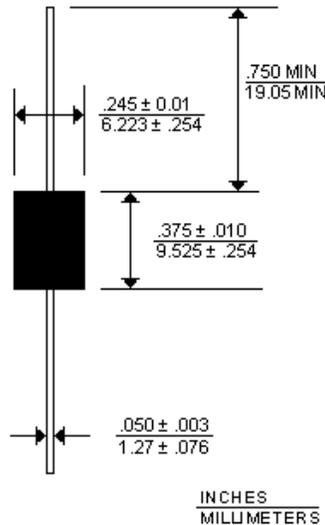
MAXIMUM RATINGS

- Peak Pulse Power dissipation at 25 °C: 65 kW at @ 6.4/69 μ s per waveform in Figure 8 (derate per Figure 2) with impulse repetition rate (duty factor) of 0.01 % max
- Operating and Storage temperature: -55 °C to +150 °C
- Steady-state power dissipation: 7 W @ TL = 25 °C
- Temperature coefficient of voltage: +0.100 %/°C max
- Solder temperatures: 260 °C for 10 s (maximum)

MECHANICAL AND PACKAGING

- Void-free transfer molded thermosetting epoxy body meeting UL94V-0 requirements
- Tin-Lead (90 % Sn, 10 % Pb) or RoHS (100% Sn) Compliant annealed matte-Tin plating readily solderable per MIL-STD-750, method 2026
- Body marked with part number
- Cathode indicated by band. No cathode band on bi-directional devices
- Available in bulk or custom tape-and-reel packaging
- TAPE-AND-REEL standard per EIA-296 (add "TR" suffix to part number)
- Weight: 1.6 grams (approximate)

PACKAGE DIMENSIONS



NOTE: Cathode indicated by band
 All dimensions in inches
 millimeters

Case 5A

SYMBOLS & DEFINITIONS

| Symbol | Definition | Symbol | Definition |
|----------|---------------------------------|----------|--------------------------------|
| V_{WM} | Working Peak (Standoff) Voltage | I_{PP} | Peak Pulse Current |
| P_{PP} | Peak Pulse Power | V_C | Clamping Voltage |
| V_{BR} | Breakdown Voltage | I_{BR} | Breakdown Current for V_{BR} |
| I_D | Standby Current | | |

ELECTRICAL CHARACTERISTICS @ 25°C

| MICROSEMI PART NUMBER (replace A suffix with CA for bidirectional) | Working Standoff Voltage V_{WM} | Maximum Standby Current $I_D @ V_{WM}$ | Minimum Breakdown Voltage $V_{BR} @ I_{BR}$ | Breakdown Current I_{BR} | Maximum Clamping Voltage $V_C @ I_{PP}$ (Note 1) | Peak Pulse Current $I_{PP} @ 6.4/69 \mu s$ (Note 2) |
|---|--------------------------------------|---|--|-------------------------------|---|---|
| | V max | μA | V | mA | V | A |
| MRT65KP48A | 48 | 5 | 53.3 | 5 | 77.7 | 836 |
| MRT65KP54A | 54 | 5 | 60.0 | 5 | 87.5 | 742 |
| MRT65KP60A | 60 | 5 | 66.7 | 5 | 97.3 | 668 |
| MRT65KP75A | 75 | 5 | 83.3 | 5 | 122 | 533 |

GRAPHS

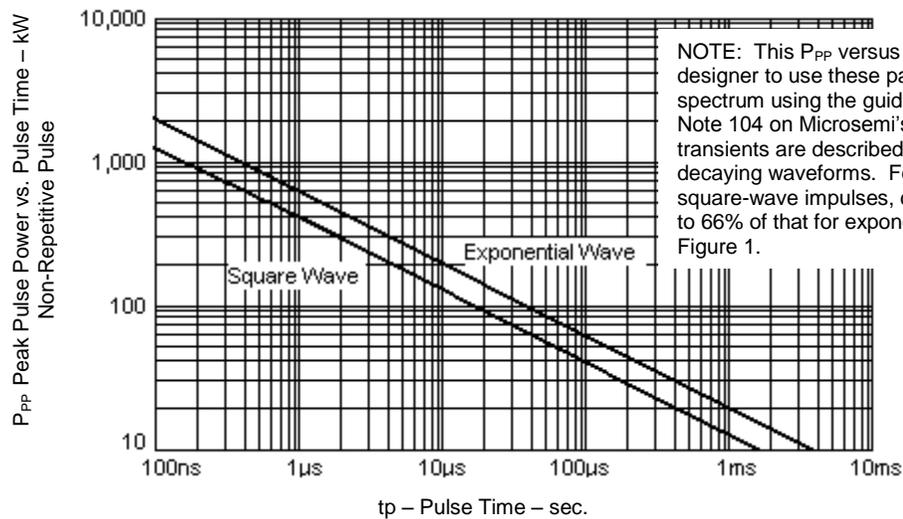


FIGURE 1
Peak Pulse Power vs. Pulse Time
To 50% of Exponentially Decaying Pulse

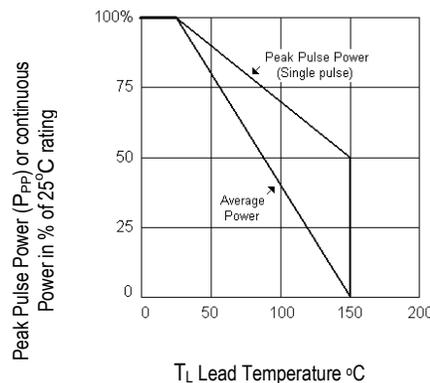
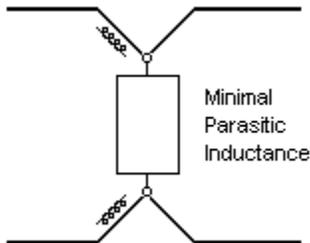
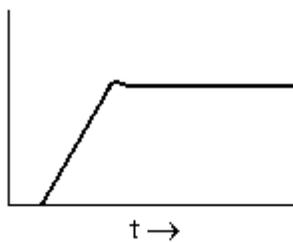


FIGURE 2
POWER DERATING

GRAPHS Contd.

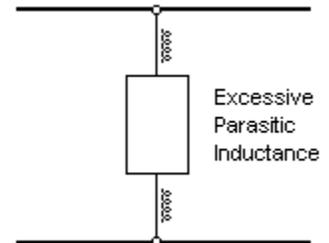
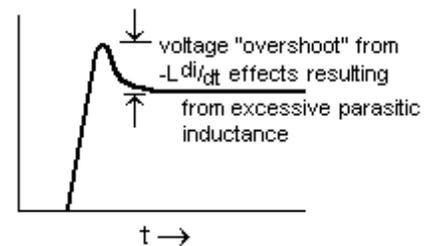
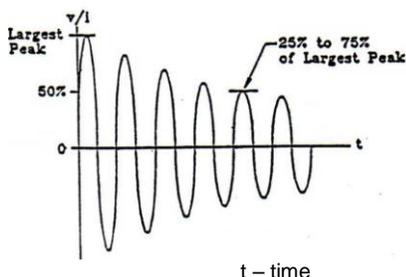
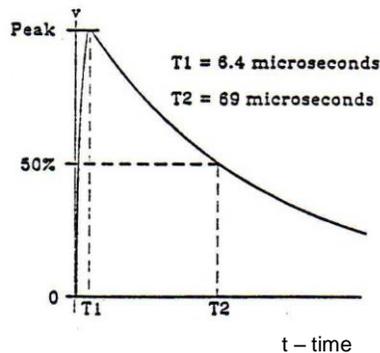
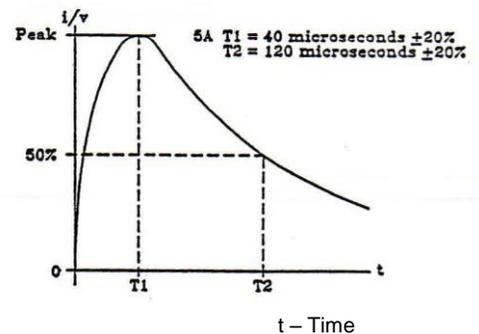
Correct


FIGURE 3

FIGURE 4

INSTALLATION

TVS devices used across power lines are subject to relatively high magnitude surge currents and are more prone to adverse parasitic inductance effects in the mounting leads. Minimizing the shunt path of the lead inductance and their $V = -L di/dt$ effects will optimize the TVS effectiveness. Examples of optimum installation and poor installation are illustrated in figures 3 through figure 6. Figure 3 illustrates minimal parasitic inductance with attachment at end of device. Inductive voltage drop is across input leads. Virtually no "overshoot" voltage results as illustrated with figure 4. The loss of effectiveness in protection caused by excessive parasitic inductance is illustrated in figures 5 and 6. Also see MicroNote 111 for further information on "Parasitic Lead Inductance in TVS".

Wrong


FIGURE 5

FIGURE 6

FIGURE 7 – Waveform 3

FIGURE 8 – Waveform 4

FIGURE 9 – Waveform 5A

NOTE: The 1MHz damped oscillatory waveform (3) has an effective pulse width of 4 μ s. Equivalent peak pulse power at each of the pulse widths represented in RTCA/DO-160E for waveforms 3, 4 and 5A (above) have been determined referencing Figure 1 herein as well as Application Notes 104 and 120 (found on Microsemi's website) and are listed below.

GRAPHS Contd.

| WAVEFORM NUMBER | PULSE WIDTH (μs) | PEAK PULSE POWER (kW) |
|-----------------|-------------------------------|------------------------|
| 3 | 4 | 290 |
| 4 | 6.4/69 | 65 |
| 5A | 40/120 | 49 |

Note: High current fast rise-time transients of 250 ns or less can more than triple the V_C from parasitic inductance effects ($V = -L di/dt$) compared to the clamping voltage shown in the Electrical Characteristics as also described in Figures 5 and 6 herein.