

## 130 kW Transient Voltage Suppressor

- High Reliability controlled devices
- Thru hole mounting
- Bidirectional (CA) construction
- Selections for 275 V and 295 V standoff voltages ( $V_{WM}$ )

### DEVICES

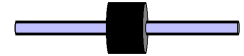
**MRT130KP275CV and MRT130KP275CA, e3**  
**MRT130KP295CV and MRT130KP295CA, e3**

### LEVELS

M, MA, MX, MXL

### FEATURES

- High reliability controlled devices with wafer fabrication and assembly lot traceability
- 100 % surge tested devices
- Suppresses transients up to 130 kW @ 6.4/69  $\mu$ s
- Fast response with less than 5ns turn-on time
- Available as either low clamp with "CV" suffix or normal clamping features with "CA" suffix
- Optional upscreening available by replacing the M prefix with MA, MX or MXL. These prefixes specify various screening and conformance inspection options based on MIL-PRF-19500. Refer to [MicroNote 129](#) for more details on the screening options.
- Moisture classification is Level 1 with no dry pack required per IPC/JEDEC J-STD-020B
- RoHS Compliant devices available by adding "e3" suffix
- 3 $\sigma$  lot norm screening performed on Standby Current  $I_D$



Case-5a

### APPLICATIONS / BENEFITS

- Pin injection protection per RTCA/DO-160F Table 22-2 up to Level 5 for Waveform 4 (6.4/69  $\mu$ s) and Level 3 for Waveform 5A (40/120  $\mu$ s) at 70 °C
- Secondary lightning protection per IEC61000-4-5 with 12 Ohms source impedance for Class 1,2, 3 and 4
- Secondary lightning protection per IEC61000-4-5 with 2 Ohms source impedance for Class 2 and 3
- Compatible with "abnormal surge voltage" as described in 16.5.2.3.1b of RTCA/DO-160F
- The very low clamping with "CV" suffix is designed for low clamping protection of 400V transistors, IGBTs and MOSFETs in off-line switching power supplies.
- The normal clamp device with "CA" suffix is for use in less-sensitive applications including RFI/EMI filters and general across-the-line protection

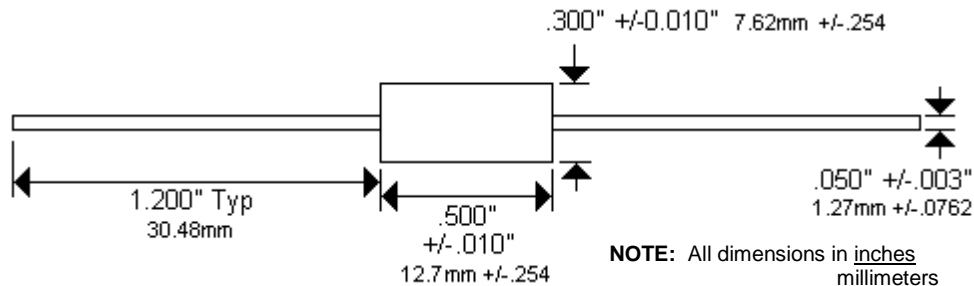
### MAXIMUM RATINGS

- Peak Pulse Power dissipation at 25 °C: 130 kW at @ 6.4/69  $\mu$ s per waveform in Figure 8 (derate as per Figure 2) with Impulse repetition rate (duty factor) of 0.001 % max for  $T_A = 25$  °C
- Steady-state power dissipation: 7 Watts @  $T_L = 25$  °C or 1.61 Watts at  $T_A = 25$  °C when mounted on FR4 PC board with recommended footprint
- Operating and Storage temperatures: -55 °C to +150 °C
- Temperature coefficient of voltage: 0.1 %/°C max
- Solder temperatures: 260 °C for 10 s (maximum)

## MECHANICAL AND PACKAGING

- Void-free transfer molded thermosetting epoxy body meeting UL94V-0 requirements
- Tin-Lead (90 % Sn, 10 % Pb) or RoHS (100% Sn) compliant annealed matte-tin plating readily solderable per MIL-STD-750, method 2026
- Body marked with part number
- No cathode band on bi-directional devices
- Weight: 2.3 grams (approximate)
- Available in bulk or custom tape-and-reel packaging
- TAPE-AND-REEL standard per EIA-296 (add "TR" suffix to part number)

## PACKAGE DIMENSIONS



Case-5a

## SYMBOLS & DEFINITIONS

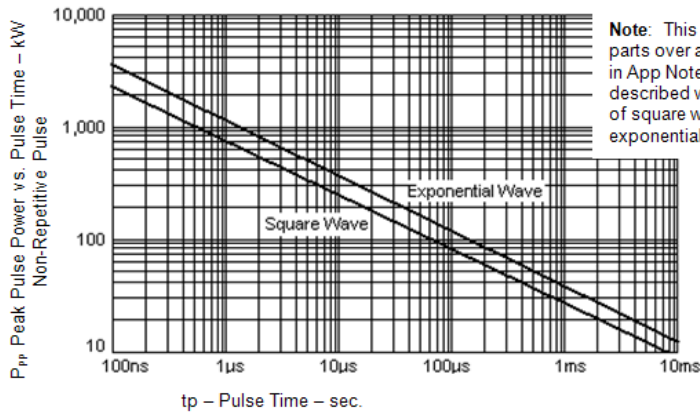
Symbol	Definition	Symbol	Definition
$V_{WM}$	Working Peak (Standoff) Voltage	$I_{PP}$	Peak Pulse Current
$P_{PP}$	Peak Pulse Power	$V_C$	Clamping Voltage
$V_{BR}$	Breakdown Voltage	$I_{BR}$	Breakdown Current for $V_{BR}$
$I_D$	Standby Current		

## ELECTRICAL CHARACTERISTICS @ 25°C

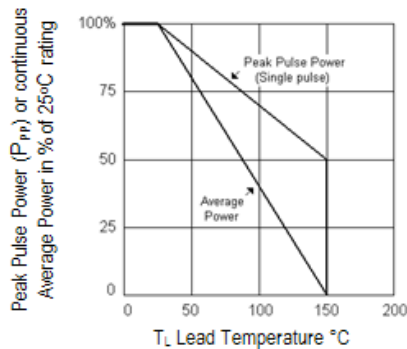
MICROSEMI PART NUMBER	Working Standoff Voltage $V_{WM}$	Maximum Standby Current $I_D @ V_{WM}$	Minimum Breakdown Voltage $V_{BR} @ I_{BR}$	Breakdown Current $I_{BR}$	Maximum Clamping Voltage $V_C @ I_{PP}$ (Note 1)	Peak Pulse Current $I_{PP} @ 6.4/69 \mu s$ (Note 2)
	V max	$\mu A$	Volts	mA	Volts	Amps
MRT130KP275CV	275	5	300	5	400	292
MRT130KP275CA	275	5	300	5	445	292
MRT130KP295CV	295	5	300	5	410	282
MRT130KP295CA	295	5	300	5	460	282

**Note 1:** See MicroNote 108 for lower Clamping Voltage performance at reduced  $I_P$  values relative to  $I_{PP}$  and  $P_{PP}$  ratings and Figure 1.  
**Note 2:** Also equivalent to 90 and 87 Amps (40 kW) respectively at a longer impulse of 10/1000  $\mu s$  (see Figure 1) with clamping voltages shown. Also see other equivalent peak pulse power performance levels for aircraft waveforms on page 3 for this device.

## GRAPHS



**FIGURE 1**  
 Peak Pulse Power vs. Pulse Time  
 To 50% of Exponentially Decaying Pulse



**FIGURE 2**  
 POWER DERATING

## GRAPHS Contd.

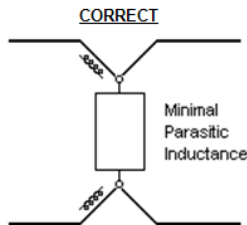


Figure 3



Figure 4

### INSTALLATION

TVS devices used across power lines are subject to relatively high magnitude surge currents and are more prone to adverse parasitic inductance effects in the mounting leads. Minimizing the shunt path of the lead inductance and their  $V = -L \frac{di}{dt}$  effects will optimize the TVS effectiveness. Examples of optimum installation and poor installation are illustrated in figures 3 through figure 6. Figure 3 illustrates minimal parasitic inductance with attachment at end of device. Inductive voltage drop is across input leads. Virtually no "overshoot" voltage results as illustrated with figure 4. The loss of effectiveness in protection caused by excessive parasitic inductance is illustrated in figures 5 and 6. Also see MicroNote 111 for further information on "Parasitic Lead Inductance in TVS".

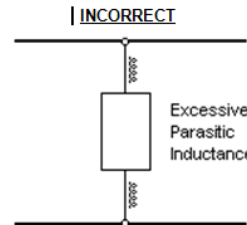


Figure 5

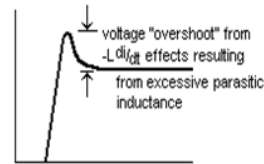


Figure 6

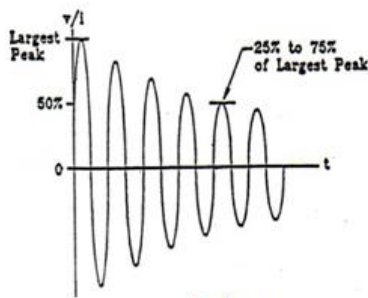


Figure 7 – Waveform 3

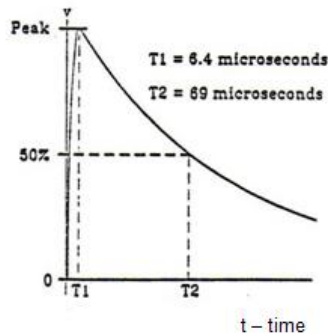


Figure 8 – Waveform 4

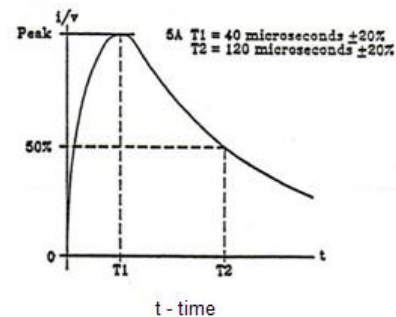


Figure 9 – Waveform 5A

**Note:** The 1MHz damped oscillatory waveform (3) has an effective pulse width of 4  $\mu$ s. Equivalent peak pulse power for the RT130KP275CA and RT130KP295CA at each of the pulse widths represented in RTCA/DO-160E for wave forms 3, 4 and 5A (above) have been determined referencing Figure 1 herein as well as Application Notes 104 and 120 (found on Microsemi's website) and are listed below.

WAVEFORM NUMBER	PULSE WIDTH $\mu$ S	PEAK PULSE POWER kW
3	4	580
4	6.4/69	130
5A	40/120	98

**Note:** High current fast rise-time transients of 250 ns or less can more than triple the  $V_C$  from parasitic inductance effects ( $V = -L \frac{di}{dt}$ ) compared to the clamping voltage shown in the initial Electrical Characteristics on page 1 as also described in Figures 5 and 6 herein.