RELIABILITY REPORT

FOR

MAX3622CUE+

PLASTIC ENCAPSULATED DEVICES

November 23, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX3622CUE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
.....Attachments
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation

I. Device Description

A. General

The MAX3622 is a low-jitter precision clock generator optimized for networking applications. The device integrates a crystal oscillator and a phase-locked loop (PLL) clock multiplier to generate high-frequency clock outputs for Ethernet and other networking applications. Maxim's proprietary PLL design features ultra-low jitter (0.36psRMS) and excellent power-supply noise rejection, minimizing design risk for network equipment. The MAX3622 has one LVPECL output and one LVCMOS output. It is available in a 16-pin TSSOP package and operates over the 0°C to +70°C temperature range.

II. Manufacturing Information

A. Description/Function:	Low-Jitter, Precision Clock Generator with Two Outputs
B. Process:	MB3
C. Number of Device Transistors:	
D. Fabrication Location:	California
E. Assembly Location:	Thailand
F. Date of Initial Production:	December 18, 2007

III. Packaging Information

A. Package Type:	16L TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2568 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	106°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	90°C/W
M. Multi Layer Theta Jc:	27°C/W

IV. Die Information

A. Dimensions:	82 X 82 mils
B. Passivation:	BCB
C. Interconnect:	Al with top layer 100% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.4 \times 10^{-9}$

$\lambda = 23.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SCFZD3006D D/C 0830)

The HD86 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX3622CUE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0	SCFZDZ004B, D/C 0725

Note 1: Life Test Data may represent plastic DIP qualification lots.