RELIABILITY REPORT

FOR

MAX3610BU/D

PLASTIC ENCAPSULATED DEVICES

September 22, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX3610BU/D successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3610 is a low-jitter, high-performance, dual-rate clock generator optimized for 1Gbps/2Gbps/4Gbps Fibre-Channel applications. When connected with an external AT-cut crystal, the device generates a precision clock output by integrating a crystal oscillator with Maxim's low-noise phase-locked loop (PLL) providing a low-cost solution. By coupling Maxim's low-noise PLL design featuring a low-jitter generation VCO with an inexpensive fundamental mode crystal, the MAX3610 provides the optimum combination of low cost, flexibility, and high performance. The MAX3610 output frequency is selectable. When using a 26.5625MHz crystal, the output clock rate can be set to either 106.25MHz or 212.5MHz. When operating at 106.25MHz, the typical phase jitter is 0.7psRMS from 12kHz to 20MHz. The MAX3610A has low-voltage positive-emitter-coupled logic (LVPECL) clock output drivers. The MAX3610B has low-voltage differential-signal (LVDS) clock output drivers. The MAX3610 output drivers can also be disabled. The MAX3610 operates from a single +3.3V supply. The PECL version typically consumes 165mW, while the LVDS version typically consumes 174mW. Both devices are available in die form and have a 0°C to +85°C operating temperature range.

II. Manufacturing Information

A. Description/Function:	Low-Jitter 106.25MHz/212.5MHz Fibre-Channel Clock Generator
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	NA
F. Date of Initial Production:	4/7/2004

III. Packaging Information

A. Package Type:	-pin DICE SALES
B. Lead Frame:	
C. Lead Finish:	
D. Die Attach:	None
E. Bondwire:	NA (NA mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0000-0004
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1

IV. Die Information

A. Dimensions:	74 X 64 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.99 \times 10^{-9}$

$\lambda = 4.99$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HT49 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX3610BU/D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	96	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data