June 2007

ERRATA SHEET
DS3100

Revision A2 Errata

The errata listed below describe situations where DS3100 revision A2 components perform differently than expected or differently than described in the data sheet. Microsemi Corporation intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3100 revision A2 components. Revision A2 components are branded on the topside of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively.

1) LOCAL LOOPBACK ISSUE IN BITS TRANSCEIVERS

Description:
When local loopback (BLCR4:LLB = 1) in the BITS transceivers is enabled, the BITS receiver squelches its output clock if the BITS receiver LIU is declaring analog loss of signal (BLIR1:LOS = 1).

Workaround:
Enable analog loopback (BLCR4:ALB = 1) simultaneously with local loopback.

Analog loopback internally connects the BITS transmitter TTIP/TRING pins to the BITS receiver RTIP/RRING pins. This provides a valid signal to the BITS receiver LIU, eliminating the analog loss of signal condition and thereby causing the BITS receiver to ***not*** squelch its output clock. The BITS transmitter must be configured for the same mode of operation as the receiver (DS1, E1, or 2048kHz) and have BLCR4:TPD = 0 for this workaround to be effective.

2) 6312kHz RECEIVE SENSITIVITY AND LOS THRESHOLD

Description:
In 6312kHz mode (BMCR:RMODE = 11b) the BITS LIU receivers have a loss-of-signal threshold of approximately -24dBm, but the LIU receivers do not reliably recover the incoming signal at signal levels below -15dBm.

Workaround:
System software can periodically read the signal level from the BLIR2:RL[3:0] register field. If software finds the level to be less than -15dBm, then the input clock connected to that BITS receiver (as specified in the BCCR2:RCLKD field) can be manually invalidated by clearing the associated bit in the VALCR1 or VALCR2 registers.