Component Selection and Performance Test for the MAX945x High-Precision CLK Generators

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Abstract: The MAX9450/MAX9451/MAX9452 are high-precision clock generators with an integrated VCXO, the same PLL core, and three different outputs: LVPECL, HSTL, LVDS. The MAX945x clock generators have four main features: integrated VCXO, wide operating-frequency range, wide PLL frequency divider with very fine granularity, and a function-rich input reference monitor. In this application note, we explain how to select the external crystal and choose the external loop-filter components. The performance measurements for tuning range, jitter, and phase noise with various crystals are discussed.

Introduction

The MAX9450/MAX9451/MAX9452 clock generators[1] provide high-precision clocks for timing in SONET/SDH systems, Gigabit Ethernet systems, and the ADC/DAC of 3G base stations. The devices can also be used as a jitter attenuator, and they have the same core with three different outputs: LVPECL, HSTL and LVDS. The block diagram of the chip is shown in **Figure 1**.

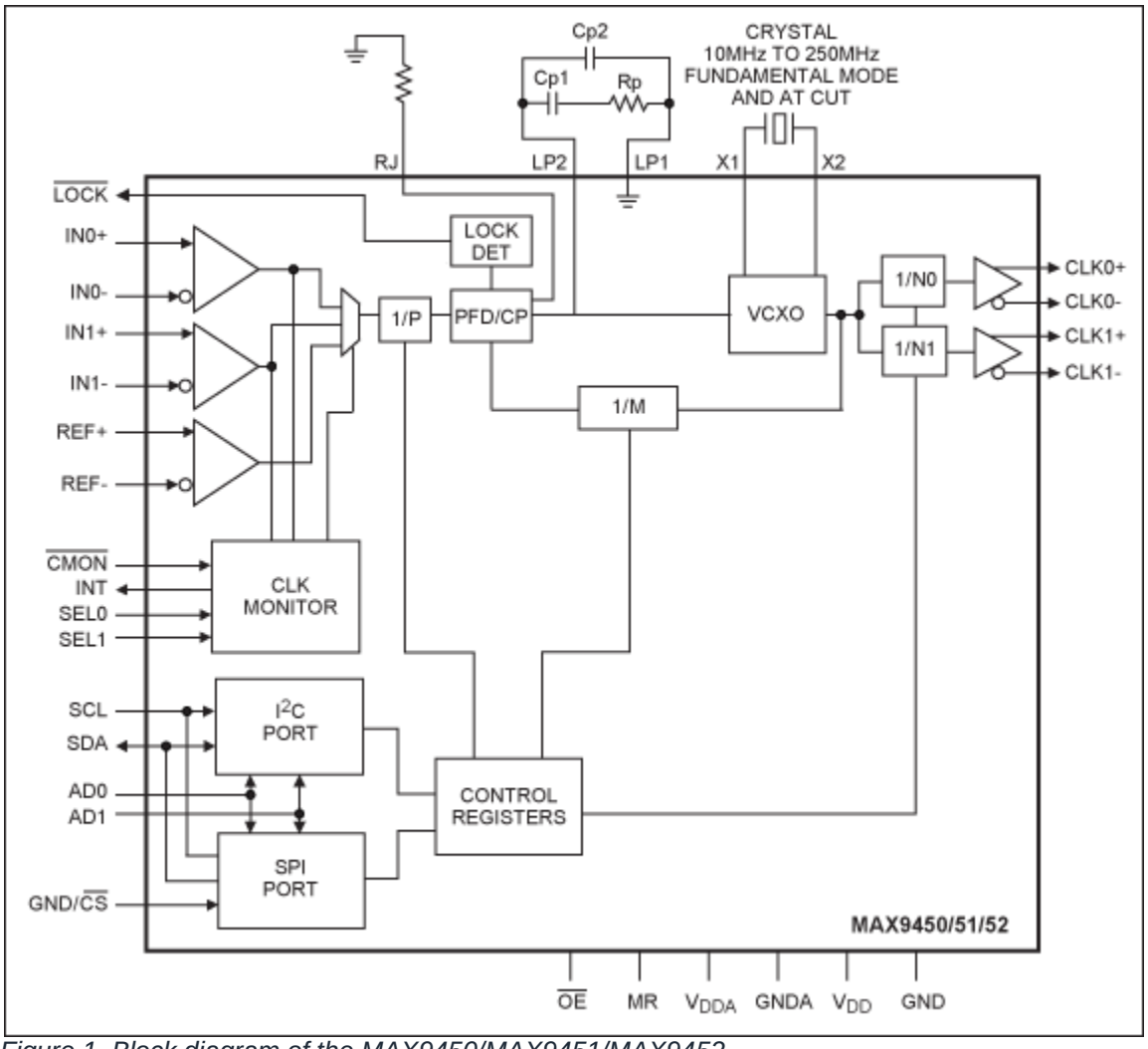

Figure 1. Block diagram of the MAX9450/MAX9451/MAX9452.

The VCXO integrated in the MAX945x devices eliminates the use of an external VCXO and provides a cost-effective solution for generating high-precision clocks. The VCXO frequency and tuning range are determined by the same parameters as the external crystal. The VCXO is designed so that it can operate with a wide range of crystal frequencies from 15MHz to 160MHz. Compared to finding a VCXO of the *right* frequency, a crystal of the *same* frequency is much easy to obtain, which provides the flexibility for different applications. Each device's frequency divider has a very broad range from 1 to 32,768, which allows the clock generator's 160MHz output to be synchronized to an 8kHz reference input. Furthermore, the devices have a reference monitor function which oversees the quality of the input reference clocks.

To use these chips properly, the designer must choose the right crystals and loop-filter components. This application noteguides the selection of these external parts. The performance results measured on various crystals are provided.

Crystal Selection

As shown in Figure 1, the VCXO's active circuitry is integrated into the chip and only the crystal and loop-filter RC components are external. As noted above, the crystal frequency must be the same as the desired output frequency. But we also need to consider the crystal's oscillation mode, cut type, loading capacitance (CL), frequency tolerance range, shunt capacitance (C0), and motional capacitance (C1).

The crystals for MAX945x must be AT-cut and oscillate in the fundamental mode, which means that the crystals need a wide tuning range and small temperature variation. Figure 2 shows the equivalent circuit of a crystal.

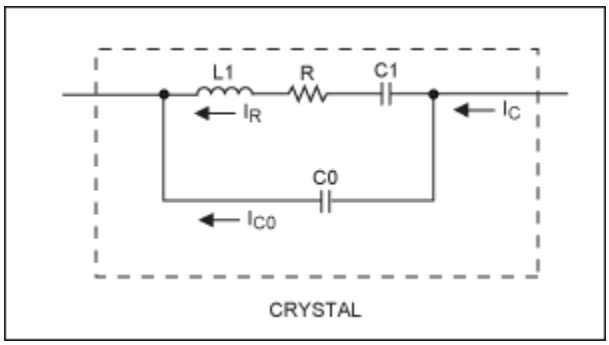

Figure 2. The crystal equivalent circuit.

The VCXO's oscillation frequency is determined by:

$$f_P = \frac{1}{2\pi f_0} \times \sqrt{1 + \frac{C_1}{C_0 + C_L}} \qquad \text{(Eq. 1)}$$

From this equation, we take the variation analysis of f_P with respect to C_L and obtain:

$$\Delta f_P = \frac{-1}{4\pi f_0} \times \frac{C_1}{(C_0 + C_L)^2} \times \Delta C_L \qquad \text{(Eq. 2)}$$

From Equation 2 we see that tuning sensitivity increases with a large C_1 value and small values of C_0 and C_L. Therefore, to make the MAX945x clock generators have a wide tuning range, we need to select crystals with the same relative values for C_1, C_0, and C_L. Experiments showed that to get a good tuning range we need C_1 > 6fF, C_L = 8pF and C_0 < 2.5pF. (This will be illustrated with data later.) Note, however, that if the value of C_L is smaller than 8pF, it will cause the positive side loss in the tuning range. We tested the DSX321S crystal from KDS[2] and XHFF45 crystal from Fortiming[3], and the measured results are presented later. For both the tested crystals, the values of the shunt capacitors used on the PCB board are given in **Table 1**.

Filter-Loop Component Selection

The MAX9450 has an external loop filter, which provides the flexibility for setting the components of the PLL loop filter. There is a general rule for selecting the loop filter bandwidth: to suppress the jitter coming from the reference input, select a narrow PLL bandwidth; to suppress the jitter created by the VCXO, use a wider PLL bandwidth. It is, therefore, commonly assumed that if the VCXO is known to have much less jitter than the input jitter bandwidth, then the right PLL filter bandwidth can be determined. In this example the PLL filter bandwidth would thus be narrower than the input jitter bandwidth. In practice, however, we commonly do not know the input jitter bandwidth and the VCXO jitter level. Thus, the best loop-filter components are often found experimentally by knowing how the components affect the PLL bandwidth.

It can be shown that the open-loop unit-gain bandwidth, ω_o, is the same as the 3dB bandwidth, ω_{3db}, of the PLL. This means that ω_o can be determined by the PLL's jitter attenuation requirement. The following equations guide the component selection with a given ω_o. The ω_o can be expressed as:

$$\omega_O = \frac{I_P \times R_P \times K_{VCO}}{N} \text{ (Rad/s)} \qquad \text{(Eq. 3)}$$

where I_P is the charge pump current, RP is the loop filter resistor, N is the frequency divider ratio, and KVCO is the VCXO's sensitivity. This equation is valid when the time constant of $R_P C_{P1}$ meets:

$$R_P \times C_{P1} < \frac{5}{\omega_O} \qquad \text{(Eq. 4)}$$

In addition, this relationship ensures a good phase margin for loop stability. The function of C_{P2} is to filter voltage ripples as the current charge pump switches. The general rule for choosing C_{P2} is:

$$C_{P2} = \frac{C_{P1}}{10} \qquad \text{(Eq. 5)}$$

It will be helpful to proceed through an example to obtain the values of the components. It is given that the ω_{3db} is expected as 5000rad/S, N = 4, and I_P = 80µA. The measured average K_{VCO} is 15KHz/V. From Equation 3, we have:

$$R_P = \frac{N \times \omega_O}{I_P \times K_{VCO}} = \frac{4 \times 5000}{80 \times (1e-6) \times 15000} = 16.6k\Omega \qquad \text{(Eq. 6)}$$

We choose R_P = 16kΩ. Then the value of CP1 can be determined by:

$$C_{P1} = \frac{5}{R_P \times \omega_O} = \frac{5}{16000 \times 5000} = 62.5nF \qquad \text{(Eq. 7)}$$

We choose C_{P1} = 66nF and C_{P2} = 6.6nF, according to Equation 5. To obtain the specified 80µA charge-pump current and using the formula on Page 10 of the MAX9450 data sheet,[1] we obtain the RJ's value as 30kΩ. For a general discussion of determining the loop-filter components, please see the references at the end.[4]

Measurement Results

We tested the crystals from KDS and Fortiming. **Table 1** shows the crystals' tuning range and the MAX9450's jitter performance. The jitter measurements were not done for every crystal; the period jitter is described by the RMS and peak-to-peak values. The phase noise was measured by integration in the 12kHz to 20MHz band.

Table 1. Tuning Range and Jitter Performance of the MAX9450

KDS Crystal DSX321S						
	Tuning Range Upper Limit	**Tuning Range Lower Limit**	**Upper Tuning Range (PPM)**	**Upper Tuning Range (PPM)**	**Jitter (RMS/P-P) (ps)**	**Phase Noise 12kHz-20MHz (ps)**
155.52MHz Crystal C_L = 8pF, no shunt caps						
Crystal 1	155.534	155.5052	90	-96		
Crystal 2	155.5348	155.5044	95	-101		
Crystal 3	155.5332	155.5036	84	-106		
155.52MHz Crystal C_L = 6.5pF, no shunt caps						
Crystal 1	155.5276	155.5	48	-129		
Crystal 2	155.5248	155.496	30	-155		
122.88MHz Crystal C_L = 8pF, no shunt caps						
Crystal 1	122.8936	122.8692	110	-88		
Crystal 2	122.8944	122.87	117	-82	5.1/40	
155.52MHz Crystal C_L = 16pF, with two 10pF shunt caps						
Crystal 1	155.558	155.5276	244	48	2.75/20	0.65
155.52MHz Crystal C_L = 14pF, with two 10pF shunt caps						
Crystal 1	155.528	155.5168	51	-20		
Fortiming Crystal XHFF45						
155.52MHz Crystal C_L = 16pF, with two 10pF shunt caps						
Crystal 1	155.5564	155.5292	234	59	4.0/31	0.544
Crystal 2	155.5568	155.5304	236	67	4.48/35	0.79
Crystal 3	155.5569	155.5294	237	60	4.5/34	0.58
155.52MHz Crystal C_L = 8pF, with two 5pF shunt caps						
Crystal 1	155.5292	155.5096	59	-67	2.8/20	0.414

Figures 3 through **5** show the MAX9450 phase-noise plots with the crystals from KDS and Fortiming.

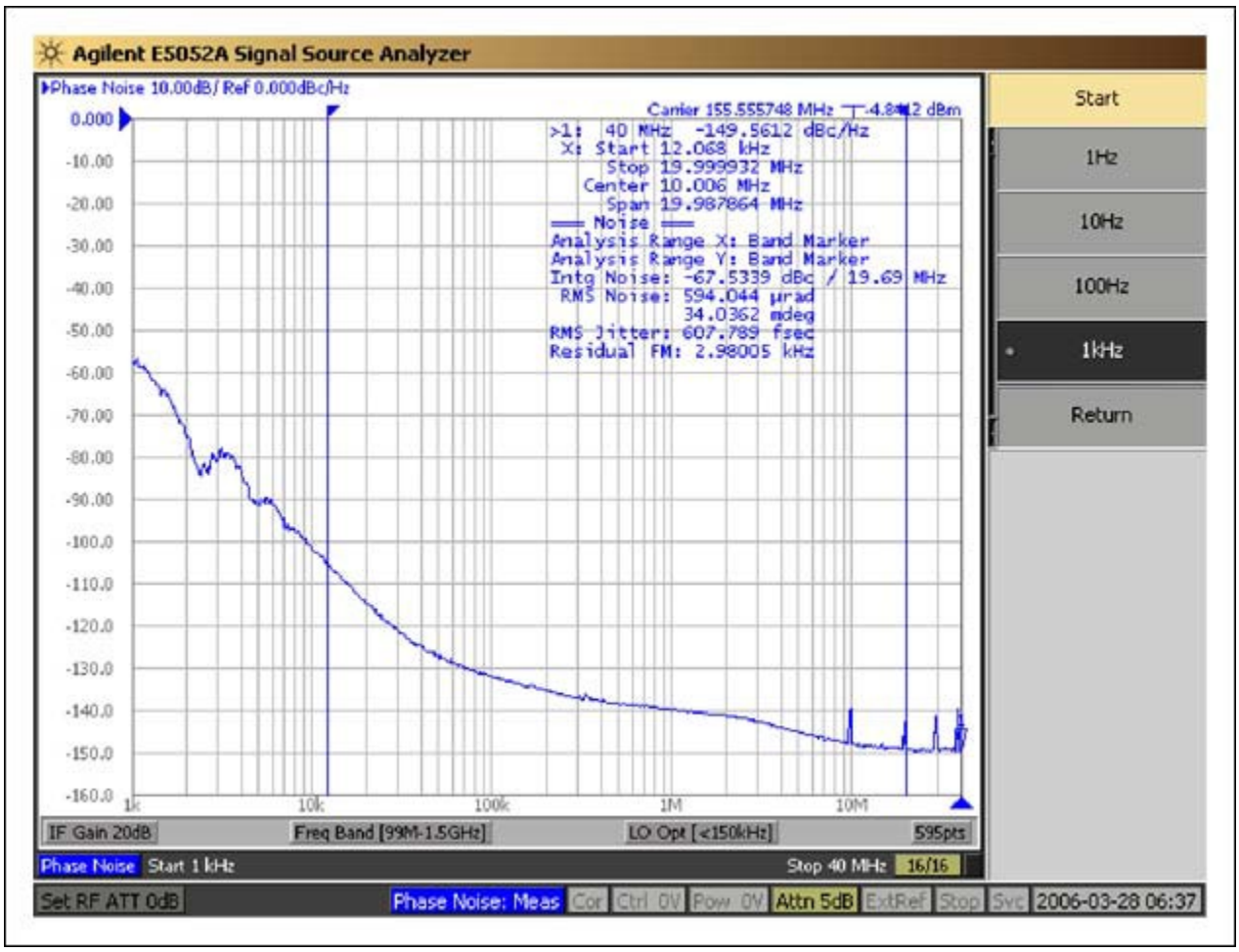

Figure 3. KDS 155.52MHz crystal with 16pF C_L.

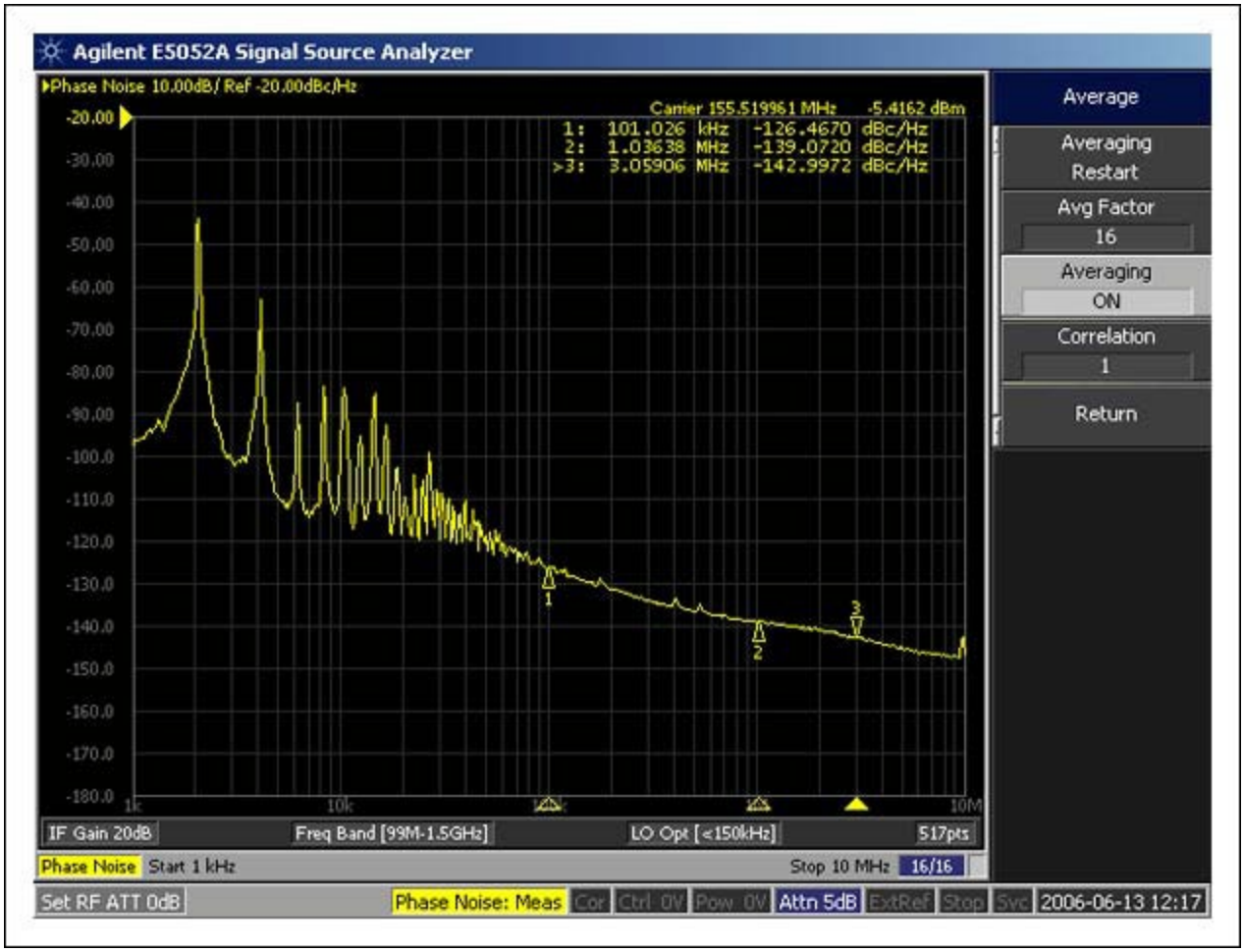

Figure 4. KDS 155.52MHz crystal with 8pF C_L.

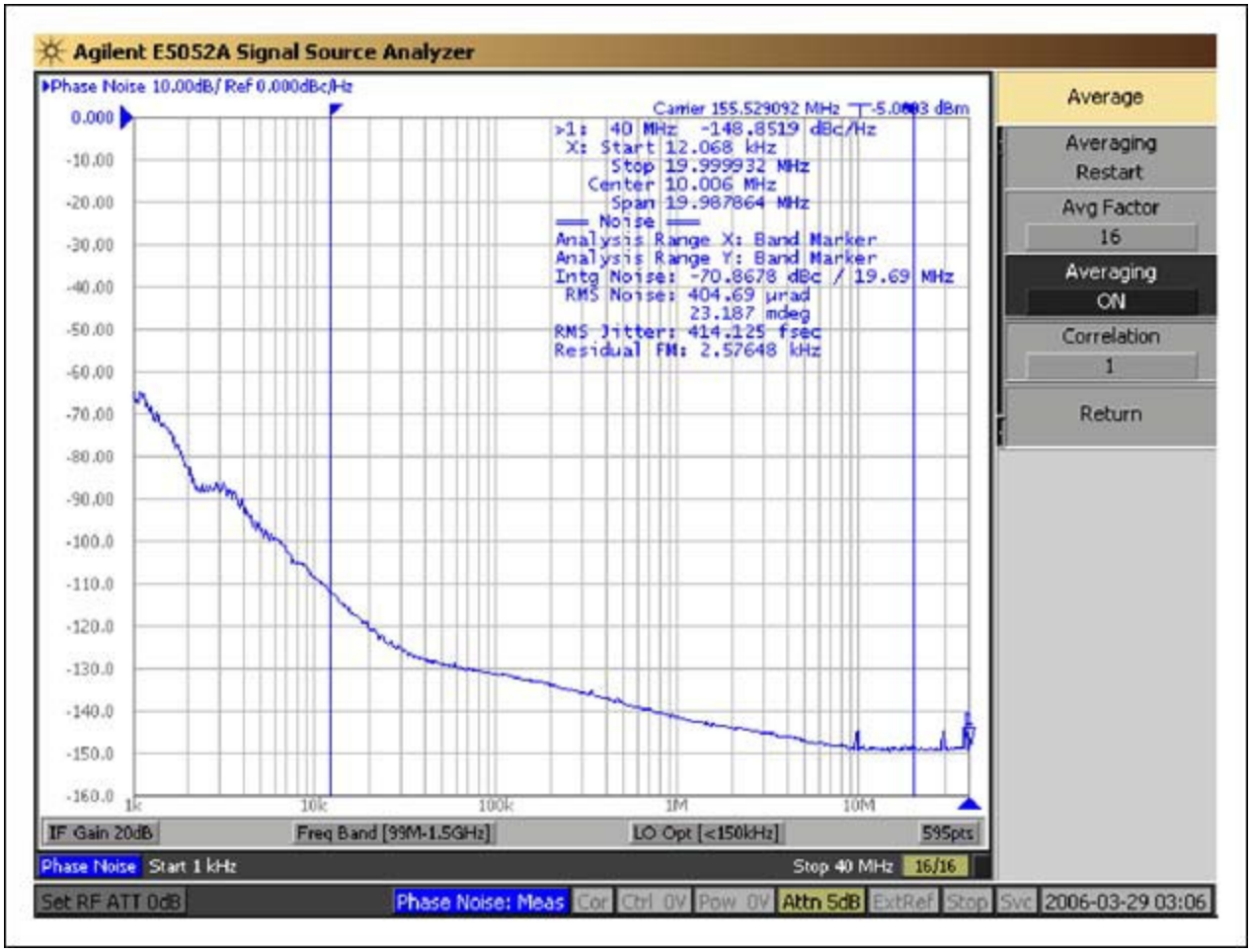

Figure 5. Fortiming 155.52MHz crystal with 8pF C_L.

Summary

The following observations can be made from the measurement results shown above.

1. For a proper and symmetrical tuning range, 8pF is recommended for the crystal load (C_L) capacitance. The maximum tuning is around ±100ppm.
2. The MAX9450's phase noise in the 12kHz to 20MHz band is less than 1ps for both crystals, and is irrelevant to the load capacitance.
3. A crystal with a large loading capacitance has less tuning range.
4. In average, KDS's crystal provided a wider tuning range than Fortiming's crystal.

The evaluation (EV) board for the MAX945x is available. To request an EV board, please contact the factory.

References

1. MAX9450/MAX9451/MAX9452 data sheet
2. KDS DSX321S data sheet at: http://www.kds.info/index_en.htm
3. Fortiming XHFF45 data sheet at: http://www.4timing.com/specification/xhff45p.pdf
4. W. O. Keese, "An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops," at: http://www.sss-mag.com/pdf/pllfil.pdf