**Design Note:**

# HFDN-13.0

Rev.2; 04/08

# Loop-Filter Configuration for the MAX3670 Low-Jitter PLL Reference Clock Generator

# Loop-Filter Configuration for the MAX3670 Low-Jitter PLL Reference Clock Generator

## 1 Introduction

The MAX3670 low-jitter clock generator is a monolithic phase-locked loop (PLL) that uses an external high-Q voltage-controlled oscillator (VCO) to create a very low jitter clock signal phase-locked to a system clock input. It is ideal for SONET OC-48 or OC-192 applications requiring a very low jitter 156MHz or 622MHz clock signal. The contribution of the MAX3670 to total system jitter is typically small compared to that of the external VCO. When used with a low-jitter voltage-controlled SAW oscillator (VCSO) or a voltage-controlled crystal oscillator (VCXO), the total system jitter can be less than $1ps_{rms}$.

Figure 1 is a block diagram of the MAX3670. The system clock input to the PLL is typically 78MHz, 156MHz, or 622MHz, and the VCXO or VCSO typically operates at 156MHz or 622MHz. The PLL bandwidth is adjustable from 10Hz to 10kHz by means of selectable on-chip dividers, phase detector gain selection, and external resistor values. The MAX3670 PLL jitter peaking can be held to less than 0.1dB with an external filter capacitor no larger than 2.2uF. An on-chip op amp provides loop-filter gain, and an optional clock output divider is offered. A lock detect output can be used to indicate the status of the system clock input.

This design note provides analysis and examples that address optimal PLL configuration, including external component values, internal divider settings, and internal phase detector gain for low-jitter applications.

## 2 MAX3670 Reference Clock Generator PLL Model

Figure 2 is a simplified model of the MAX3670 PLL in closed-loop operation. The phase-frequency detector converts phase error into current with a gain of $K_{pd}$ (A/UI). In the MAX3670, one of two settings can be selected for $K_{pd}$ using the GSEL inputs, which also control a portion of the feedback divider ratio. The loop filter, with transfer function F(s), operates on the phase detector output current to generate the control voltage to the VCO. This filter, in conjunction with the feedback divider, establishes the key characteristics of PLL operation, including bandwidth, output jitter, and PLL stability. The VCO then translates the filter output voltage to frequency, and the VCO output is fed back through the dividers to the phase-frequency detector. The external VCO transfer function is $K_{vco}/s$, where $K_{vco}$ (Hz/volt) is the VCO frequency gain, and 1/s represents the integration of frequency to phase.

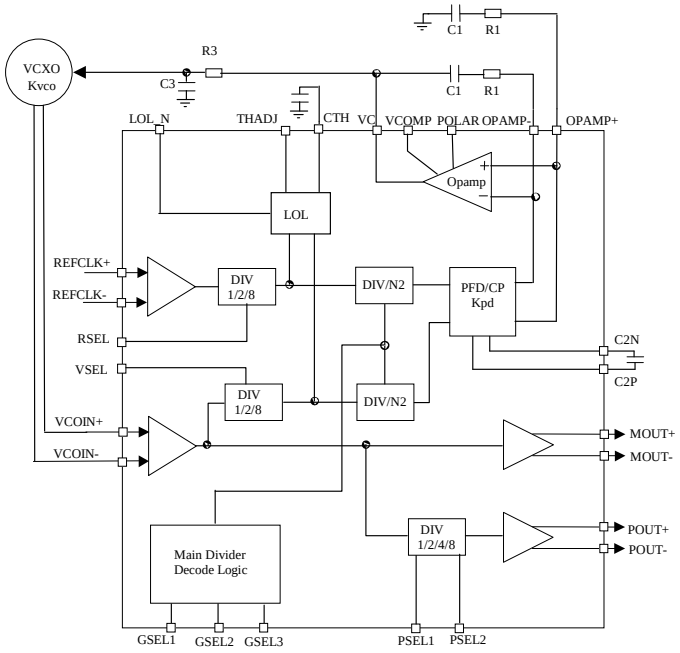


*Figure 1. MAX3670 low-jitter reference clock generator block diagram*

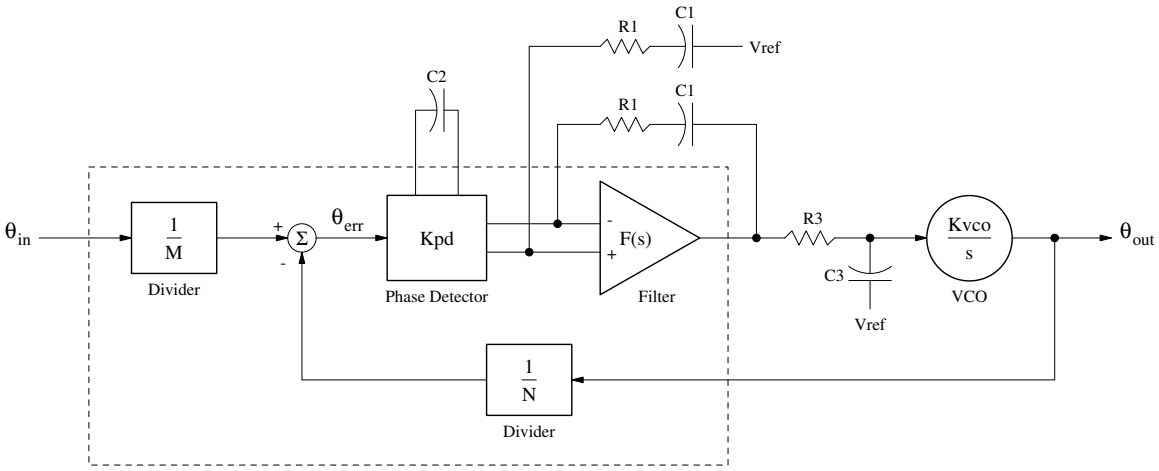


*Figure 2. Idealized PLL phase-domain model*

## 3 Closed-Loop PLL Model

When the PLL is in closed-loop operation, the small signal behavior is well characterized as a second-order linear system. The following is a brief summary of the relationships that govern the operation of the MAX3670 PLL.

The external VCO is the first integrator in the PLL transfer function, $K_{vco}/s$. To control static phase error, the loop filter provides a second integrator, implemented via the internal op amp and capacitor $C_1$. For stability, a zero is added to the loop in the form of resistor $R_1$ in series with $C_1$. The location of this zero can be approximated as

$$f_z = \frac{1}{2\pi R_1 C_1}$$

A high order pole (HOP) is also needed to reduce spurious noise from the phase detector. It can be implemented either by providing a compensation capacitor $C_2$, which produces a pole at

$$f_{hop} = \frac{1}{2\pi(20k\Omega)(C_2)},$$

or by adding a lowpass filter, consisting of $R_3$ and $C_3$, directly on the VCO tuning port, which produces a pole at

$$f_{hop} = \frac{1}{2\pi R_3 C_3}.$$

Using $R_3$ and $C_3$ may be preferable, because it filters more noise in the PLL; but, in that case, it may still be necessary (particularly when using large values for $R_1$ and N) to provide filtering via $C_2$ in order to prevent clipping in the op amp. Finally, the external VCO adds a HOP, due to the modulation bandwidth of the tuning input. In order for the analysis presented here to model true system behavior, the pole associated with the VCO should be well above the other poles.

## 4 Factors Governing Closed-Loop PLL Behavior

The PLL phase transfer function relates the phase at the clock output of the MAX3670, $\theta_{out}$, to the phase at the system clock input, $\theta_{in}$. This transfer function describes how phase noise (jitter) is attenuated from the PLL input to the PLL output, and is shown in the bode plot of Figure 3. An important closed-loop performance specification is the loop bandwidth (in Hz), which is given by

$$K = \frac{K_{pd} R_1 K_{vco}}{2\pi N}.$$

Jitter present on the reference clock input is attenuated for frequencies higher than the loop bandwidth, K. If the total output jitter is dominated by the noise in the clock input, then lowering the loop bandwidth will reduce system jitter.

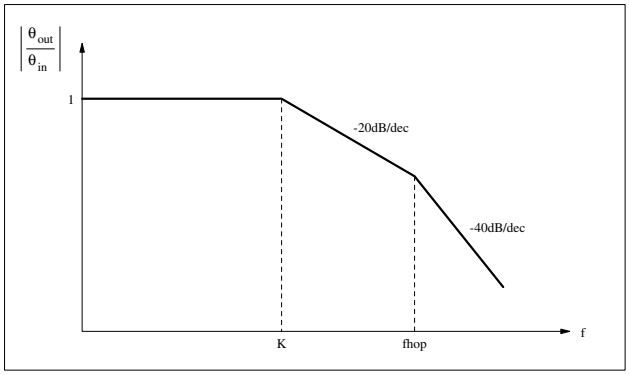


*Figure 3. PLL phase transfer function, $\theta_{out}/\theta_{in}(f)$*

The VCO phase transfer function relates the phase at the output of the PLL, $\theta_{out}$, to the phase of the VCO. This transfer function describes how phase noise in the external PLL oscillator (VCXO or VCSO) is attenuated in the MAX3670 output, and is shown in Figure 4. VCO phase noise is attenuated at frequencies lower than the loop bandwidth (conversely, VCO phase noise at frequencies greater than the loop bandwidth is not attenuated). If the total output jitter is dominated by phase noise in the VCO, then raising the loop bandwidth will reduce system jitter.

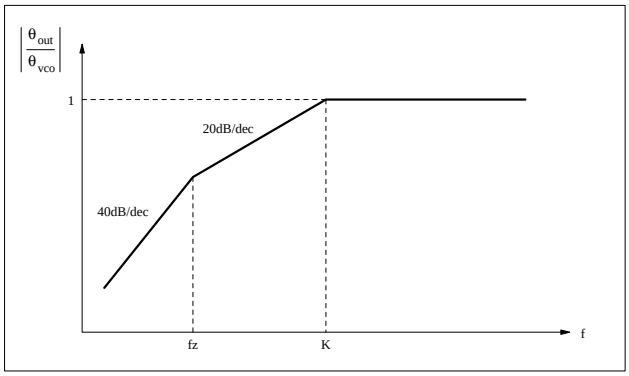


*Figure 4. VCO phase transfer function, $\theta_{out}/\theta_{VCO}(f)$*

Finally, any additional noise present at the VCO tuning input port, in the band between $f_z$ and K, will be transmitted to the output of the PLL with a gain of $N/K_{pd}R_1$ (UI/V).

# 5 PLL Configuration and External Component Selection

This section provides a brief explanation of the design choices that can be made to achieve the desired performance from the MAX3670 PLL. This process begins by choosing the PLL closed-loop bandwidth, VCO frequency, and system clock and feedback divider ratios, depending on the application. The external VCO might be a low-jitter VCXO for 155MHz applications or a low-jitter VCSO for 622MHz applications. Consult the vendor for minimum, maximum, and typical values of VCO gain, $K_{VCO}$. If possible, the system clock divider, RSEL, and the VCO divider, VSEL, should be set so that the compare frequency at the LOL sample point is 78MHz, to provide optimum LOL detection. The next step is to set the values for the discrete resistors and capacitors to implement the desired pole locations.

In some important applications, it may be desirable to limit the jitter peaking in the PLL phase transfer function bandpass region to less than 0.1dB. This can be achieved by setting the zero frequency lower than the loop bandwidth by a factor of approximately 100, which produces a large damping coefficient. In this case, the jitter peaking, in dB, is given by

$$Peaking = 20\log\left(1+\frac{f_z}{K}\right).$$

The next step in the PLL configuration is the selection of the HOP frequency. As noted before, a HOP is useful in cutting down high-frequency spurious noise from the digital phase detector. This is addressed by choosing the HOP frequency to be much less than the phase detector compare frequency. A good choice is 10*fhop < fvco/N, where N is the total feedback division ratio. It should, however, be placed high enough in frequency that it does not decrease the overall loop phase margin and impact jitter peaking. This objective can be accomplished by making certain that $f_{hop} > 4K$. This will ensure that the contribution to jitter peaking from the HOP is less than 0.08dB.

The next section shows how a spreadsheet can be used as a tool to optimize the design.

# 6 Component Selection for Minimum Jitter

For a particular choice of loop bandwidth, VCO gain, and divider ratios, the values of the passive components $C_1$, $C_2$, and $R_1$ can be selected in a manner to minimize the intrinsic and spurious jitter components at the reference clock generator output. Of course, this does not include the unattenuated

jitter due to the VCO or transmitted through the PLL from the system clock input, as described above.

Intrinsic PLL noise is associated with the loop-filter feedback resistor, $R_1$. This noise in the MAX3670 scales with the value of $R_1$, and it rolls off below the zero frequency, $f_z$, and above the loop bandwidth, K, as discussed above. When measured in a 1kHz to 20MHz bandwidth, the intrinsic random jitter, in $UI_{rms}$ with respect to the VCO frequency, can be approximated by

$$\theta_{rms} = \sqrt{\frac{(36\times10^{-9} + 1.29\times10^{-12} R_1)^2 K_{vco} 4}{2\pi}},$$

where the factor of 4 corresponds to $f_{hop} = 4K$.

Spurious noise results from unavoidable offsets in the MAX3670 op amp and elsewhere. In normal operation, the phase detector generates up and down pulses on each rising edge of the phase detector inputs, and these edges occur at the compare frequency $f_{vco}/N$. Any offsets in the loop cause either the up or down pulse to be slightly longer, which produces spurious noise. Subject to some reasonable assumptions, and if $f_{hop} << f_{vco}/N$, then the worst-case spurious output jitter, in $UI_{rms}$ with respect to the VCO frequency, is given by

$$\theta_{rms} = 0.3\frac{\pi f_{hop} K_{pd} K_{vco} R_1 \delta}{4 f_{compare}^{\ 2}},$$

where $\delta = 0.02$ is a factor that characterizes the offsets in the actual part. Table 1 shows how a spreadsheet can be used to facilitate selection of specific component values, given a particular VCO and loop bandwidth selection. In this example, the value of $C_1$ was limited to 2.2uF, in order to restrict the physical configuration to 0805 size. Otherwise, the values of $R_1$, $C_1$, and $C_2$ were chosen manually to minimize calculated intrinsic and spurious jitter contributions. In general, the least-intrinsic noise results from using lower values of $R_1$ and the feedback divider N.

## References

For additional information on the MAX3670 low-jitter reference clock generator, see the product data sheet.

**Table 1. Spurious and Intrinsic Noise Spreadsheet**

**PLL Parameters for Typical 155MHz/622MHz Oscillators Optimized for Output Noise**

| Freq VCO (MHz) | Kvco (ppm/V) | Kvco (kHz/V) | Loop BW (Hz) | DIV N1 | DIV N2 | fcomp (MHz) | Kpd (uA/UI) | R1 (kohms) | fz (Hz) | fhop (Hz) | C1 (uF) | C2 (nF) | Spurious Jitter (ps rms) | Intrinsic Noise (ps rms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **155.52** | **50** | **7.78** | **10000** | 2 | 1 | 77.760 | 20 | 808 | 100.00 | 40000 | 0.002 | 0.199 | 0.000 | 0.488 |
| **155.52** | **50** | **7.78** | **3162** | 2 | 1 | 77.760 | 20 | 255 | 31.62 | 12648 | 0.020 | 0.629 | 0.000 | 0.165 |
| **155.52** | **50** | **7.78** | **1000** | 2 | 1 | 77.760 | 20 | 81 | 10.00 | 4000 | 0.197 | 1.989 | 0.000 | 0.063 |
| **155.52** | **50** | **7.78** | **316** | 2 | 1 | 77.760 | 20 | 26 | 3.16 | 1264 | 1.973 | 6.296 | 0.000 | 0.031 |
| **155.52** | **50** | **7.78** | **100** | 2 | 16 | 4.860 | 20 | 129 | 1.00 | 400 | 1.231 | 19.895 | 0.000 | 0.092 |
| **155.52** | **50** | **7.78** | **31.6** | 2 | 128 | 0.608 | 20 | 327 | 0.32 | 126 | 1.541 | 62.959 | 0.001 | 0.207 |
| **155.52** | **50** | **7.78** | **10** | 2 | 256 | 0.304 | 5 | 827 | 0.10 | 40 | 1.924 | 198.950 | 0.000 | 0.499 |
| **622.08** | **200** | **124.42** | **10000** | 8 | 1 | 77.760 | 20 | 202 | 100.00 | 40000 | 0.008 | 0.199 | 0.000 | 0.134 |
| **622.08** | **200** | **124.42** | **3162** | 8 | 1 | 77.760 | 20 | 64 | 31.62 | 12648 | 0.079 | 0.629 | 0.000 | 0.054 |
| **622.08** | **200** | **124.42** | **1000** | 8 | 1 | 77.760 | 20 | 20 | 10.00 | 4000 | 0.788 | 1.989 | 0.000 | 0.028 |
| **622.08** | **200** | **124.42** | **316** | 8 | 4 | 19.440 | 20 | 26 | 3.16 | 1264 | 1.973 | 6.296 | 0.000 | 0.031 |
| **622.08** | **200** | **124.42** | **100** | 8 | 64 | 1.215 | 20 | 129 | 1.00 | 400 | 1.231 | 19.895 | 0.001 | 0.092 |
| **622.08** | **200** | **124.42** | **31.6** | 8 | 512 | 0.152 | 20 | 327 | 0.32 | 126 | 1.541 | 62.959 | 0.034 | 0.207 |
| **622.08** | **200** | **124.42** | **10** | 8 | 1024 | 0.076 | 5 | 827 | 0.10 | 40 | 1.924 | 198.950 | 0.027 | 0.499 |

Assumptions: 1) Must have C1 < 2.2uF 2) fz = LoopBW/100
3) fhop = LoopBW*4 4) No other significant higher-order poles
5) Jitter after 1kHz (SONET) highpass jitter filter