A Novel 65 nm Radiation Tolerant Flash Configuration Cell Used in RTG4 Field Programmable Gate Array

Jih-Jong Wang, *Member, IEEE,* Nadia Rezzak, *Member, IEEE,* Durwyn Dsilva, *Member, IEEE,* James Jia, *Member, IEEE,* Alex Cai, Frank Hawley, *Member, IEEE,* John McCollum, and Esmat Hamdy, *Senior Member, IEEE*

***Abstract*—Newly introduced radiation-tolerant flash-based FPGA, RT4G, uses a novel configuration cell design composed of a NMOS switch controlled by a totem pole p-channel flash and n-channel Flash construction. Its reliability, especially radiation tolerance, is far superior to that in the present available Flash-based FPGA. This paper describes the new flash-based configuration cell and explains its function and radiation characteristics. A subtle and unique retention issue was found and resolved through studying physical mechanisms and experimenting.**

***Index Terms*—CMOS, N-Flash, P-Flash, SEE, TID**

I. Introduction

FLASH-based field programmable gate array (FPGA) is an important integrated circuit device in aerospace electronics. It has a unique feature of being both programmable and non-volatile. The merit is enabled by the characteristics of the Flash configuration cell. The technology manufacturing Flash configuration cell is inherited from Flash-memories'. The basic knowledge of Flash memory generally applies to Flash configuration cell, and readers can refer to well-written books [1, 2] for details. However, often ignored, there are major differences between Flash memory and Flash configuration cell, owing to their very different applications. The differences will be revealed in the following discourse.

Historically, since the introduction of the first Flash-based FPGA the Flash configuration cell is N-Flash type, and it has lasted for many generations, from 0.25 μm to 65 nm technologies. Only until recently, circa early 2015, the newly introduced RTG4 family, manufactured by 65 nm technology, use a different Flash design called C-Flash, which comprises, similar to the CMOS construction, an N-Flash and a P-Flash.

This paper chronically follows the development of TID hardening of 65 nm radiation-hardened RTG4 product family. The following paragraphs in this section briefly describe the content.

The aerospace-electronics designers' interests prompt the studies of total ionizing dose (TID) effects on N-Flash-based FPGA since the introduction of the first commercially available product [3-6]. Experiment results and device physics reveal that N-Flash configuration cell's sensitivity to TID effects is the root cause for FPGA missing the aerospace-electronics requirement. The best result, comes from the newest 65 nm SmartFusion2 Family, has tolerance below 40 krad(SiO_2).

To offer a truly radiation-hardened Flash-based FPGA, with TID tolerance higher than 100 krad(SiO_2). The Flash configuration cell is redesigned and subsequently replaced by the aforementioned C-Flash. The TID testing on test structures shows C-Flash's tolerance well above 100 krad(SiO_2). However, a retention issue was found in the programmed P-Flash in the C-Flash configuration cell when statically biased for normal FPGA operation. After thorough investigations and many experiments, the physical mechanism was found and the retention issue was resolved by a small modification of the original C-Flash configuration cell. Finally the TID tolerance of new C-Flash cell and FPGA is presented.

For completeness—about the reliability of single event effects on Flash cells—heavy-ion testing data show no observable failures. This topic is beyond the scope of this paper. Interested readers can refer publication [7] for details.

II. Experiment

The devices-under-test (DUT) are Flash cells on test chips, commercial-grade 65 nm Flash-based FPGA, specifically product code named M2S050, and radiation-hardened 65 nm product code-named RT4G150.

No packaged test chip is irradiated at wafer level by ARACOR X-ray irradiator in Vanderbilt University. The electrical characteristics, usually I-V, are measured by the HP 4156 parametric measurement system and interconnected through the Agilent E5250A switching matrix. Test chips packaged in DIP and FPGAs are irradiated under γ-ray at AFRL, DMEA or NASA. For the packaged test chip, the devices' I-V is measured the same way as above. The propagation delay is measured on inverter-chain designs in

J.J. Wang, is with Microsemi-SOC, San Jose, CA95134 (e-mail: jih-jong.wang@microsemi.com).

N. Rezzak, D. Dsilva, J. Jia, A.Cai, F. Hawley, J. McCollum, and E. Hamdy are also with Microsemi-SOC, San Jose, CA95134.

FPGAs by Agilent Infiniium oscilloscope with input provided by Agilent 33220A waveform generator. Fig. 1 depicts a typical example, in which the waveforms illustrate how the delay is measured. Finally the FPGA's standby power supply current ($I_{DDSTDBY}$) is measured by HP 6629A power supply that also biases the DUT during irradiation.

Dose rate is always within the condition A of TM1019.8. Experiments conducted are proven insensitive to dose rate; therefore only the total dose is relevant and no notion of dose rate is reported in this paper. Ambient environment is always the irradiation condition.

III. N-FLASH CELL TID CHARACTERISTICS AND TID TOLERANCE OF FPGA

The technology of N-Flash configuration cell originates from Flash memories'. The transistor-level construction, however, is novel. As shown in Fig. 2, the cell actually comprises two transistors sharing a common gate that, for Flash, includes floating and control gate. Functionally the wider Flash performs the switch function in FPGA, thus it is called switch; the narrower Flash, called sense, is erased and programmed to define the configuration to be on or off. Also note the size of the cell is significantly larger than Flash memories' size.

For operations, write and read are done on sense devices. Write includes erasing the Flash to turn switch on and programming to turn switch off. Read is the "verify" operation, which measure every Flash's V_T to confirm the robustness of write. In normal FPGA operation, the erased switches connect various functional circuits and modules to execute the task, and the programmed switches provide isolation to avoid unwanted connections. Figure 3 depicts a 2 x 2 arrays to help understanding these operations. The architecture of sense alone is the same as that of Flash memory cell. The configuration write into sense will be exactly the same as switch's configuration.

TID effects on Flash-based FPGA start at the Flash configuration cells. Figure 4 shows the TID effects on the N-Flash cell. V_T is measured on the sense device as a function of total dose. Dose is applied in steps, and V_T is measured at each step. DUT drain to source is biased at 1.2 V (V_{DS}), the operation V_{DD}, and gate bias is ramped to monitor channel current I_{DS}. When I_{DS} is at 10 μA, the gate voltage is defined as V_T. The V_T versus total dose is also modeled by a natural decay equation [3]:

$$V_T(\gamma) = V_T(\infty) + [V_T(0) - V_T(\infty)] \cdot Exp(-A\gamma) \quad (1)$$

Where γ is the total dose, $V_T(0)$ initial value, $V_T(\infty)$ the saturation value when γ approaches infinity and A the decay constant. Data displayed quantitatively the degradation of both the erased and programmed cell that includes both switch and sense.

Figure 5 illustrates the physical mechanisms causing the V_T shift. In programmed N-Flash, electron emission, hole injection and hole trapping cause the V_T shift to lower. In erased N-Flash, electron injection and hole emission shift V_T to higher.

Erased-switch degradation is reflected on FPGA as the propagation delay degradation. Figure 6(a) shows the measured data. The design tested is an inverter chain of two thousand stages. The degradation is immediate from the start and continuous to the end of experiment. As shown in Fig. 6(b), the erased switches interconnecting the inverters degrade with total dose will increase the effective interconnecting resistance and consequently increase the delay.

Note that high voltage MOSFET in the configuration circuits also play a secondary role here. The quantitative analysis, e.g. Spice simulation, has not been completed to show consistence with the testing data. Nevertheless, the endeavor is not critical in the scope of this paper.

Programmed-switch degradation reflects on FPGA as the degradation on 1.2 VDC core power supply current (I_{DDSTDY}). Since the result has minor dependence on the FPGA design, the same inverter chain design was used. Figure 7(a) displays I_{DDSTDY} versus total dose: the current increase mildly initially, and followed by a steep jump at the end. Usually testing is stopped when current reach to close half amp when DUT was still functional. The elevating temperature on DUT caused by high current makes data untruthful and further testing unnecessary. As shown in Fig. 7(b), the current increase is mainly owing to programmed switch for isolation turns on and consequently causes driver contention. Also to be noted is the TID tolerance for I_{DDSTDY} is higher than for propagation delay, which is usually defined at 10% of the degradation.

In conclusion, N-Flash cell TID degradations determine the FPGA tolerance. The most critical electrical parameter is propagation delay.

IV. COMPLEMENTARY FLASH CONFIGURATION CELL AND ITS TID CHARACTERISTICS

The test results in previous section basically conclude that, to develop a Flash-based FPGA having TID tolerance higher than 100 krad(SiO_2), the N-Flash configuration cell has to be modified. In this section a cell composed of N-Flash and P-Flash in a structure similar to CMOS, thus called C-Flash, is proposed. The cell itself has been proposed fifteen years ago [8]; but it was just a concept without any product concept and actually developing an FPGA. Furthermore, radiation effects were never mentioned before.

Figure 8 depicts the schematics of C-Flash and its configuration states. C-Flash is actually a very intuitive programmable cell: just like SRAM-based, it composes of a memory-function configuration cell and an NMOSFET switch. However, the configuration elements, the cell without the switch, have complicated operations.

First of all, the traditional nomenclature of erased and programmed is not applicable to C-Flash anymore. Referring to Fig. 8, the C-Flash has to be defined by the switch state; it is on when switch is configured to on and off when switch is off. The reason is that at switch-off state, the N-Flash is erased to on and P-Flash is programmed to off, and the N- and P-Flash states are reversed for switch-on state.

2 x 2 arrays of C-Flash in Fig. 9 help to understand write and read operations. The write includes erasing N- and P-Flash simultaneous in a segment and followed by programming N-Flash word by word and then P-Flash word by word. Since the numbers of both word-line and bit-line are doubled, the table listing the bias of all the lines during configuration is more than quadrupled. Nevertheless the physical mechanisms, except P-Flash is complementary to N-Flash, are the same. The detail to be discoursed will be too extensive for this paper's scope. Another extra overhead is that in each cell p-well area has to be added, and the cell area is consequently increased.

Note that C-Flash cell or C-Flash sometimes means the configuration cell comprising the C-Flash memory and NMOS switch and other times the C-Flash memory only. Usually reader can distinguish the difference by the context.

The C-Flash cell is designed and wafer-fabricated on test chips, and they are tested for TID characteristics. Figure 10(a) plots the on-state switch I_D-V_D at various radiation steps from initial to 300 krad(SiO_2). The V_T of both N- and P-Flash are also measured for each step and plotted in Fig. 10(b). The same data are measured on C-Flash at switch-off state and plotted in Fig. 11(a) for switch I_D-V_D and (b) for N- and P-Flash V_T.

These test results clearly demonstrate the C-Flash's excellent TID tolerance. Based on previous section's conclusion, C-Flash based FPGA should have good TID tolerance. However, retention is also a reliability concern of paramount importance in Flash technology. Before C-Flash cell is proven no retention issue, it will not be implemented in FPGA.

V. RETENTION ISSUE IN COMPLEMENTARY FLASH CELL AND ITS SOLUTION

Retention issue due to band-to-band tunneling induced hot electron (BBHE) injection was found in the P-Flash at switch-off state. The symptom is V_T drifting to more positive, which means the P-Flash is turning on, over time. This issue will degrade the effectiveness of isolation provided by off-state switch and worsening contention issue in FPGA.

This physical mechanism, illustrated in Fig. 12, has been proposed to program P-Flash memory [9, 10]. When high voltage is applied to P-Flash gate with drain ground, deep-depletion in the gate-drain overlap region occurs and induces band-to-band tunneling of electrons into the drain-depletion region [11]. Then the electrons injected into the drain-depletion region are accelerated by the high electric field, which is due to the n-well to drain bias, and gradually gaining kinetic energy as they travel toward channel. These high energy electrons cause impact ionization and generate hot-electrons injecting into the floating gate and consequently cause P-Flash V_T to shift more positive. To evaluate the situation, retention tests on P-Flash are performed. Figure 13 shows the results: using conservative criterion of 0.1 V shift as the critical point, the lifetime of P-Flash with 2.5 V_{DD} and 0 V_{SS} at switch-off state is about 7 days.

It is obvious that reducing the drain voltage alone will alleviate the problem significantly. Consequently, an additional PMOS transistor inserted between the N-Flash drain and P-Flash drain, as shown in Fig. 14, solves it. The voltage drop across source-to-drain of the PMOS reduces the voltage drops of both gate-drain and body-drain more than 1 V, and suppresses both the band-to-band tunneling and hot electron impact-ionization mechanisms. The load by PMOS is a V_T drop under back bias. The PMOS $|V_T|$ is approximately 1.5 V without body bias. Referring data shown by Fig. 13, it means $1/V_{GD}$ larger than 0.66 and pushes the lifetime to significantly longer than the 10 years criterion.

VI. TID CHARACTERISTICS OF NEW C-FLASH CELL AND ITS IMPACT ON TID TOLERANCE OF FPGA

Retention-reliability enhanced C-Flash cell has been tested for TID characteristics. Figure 15 plots the results of switch-on state: (a) N- and P-Flash V_T shift as function of total dose, (b) on-switch I_D-V_D from zero to 200 krad(SiO_2); also the results of switch-off state: (c) N- and P-Flash V_T shift as function of total dose, (b) off-switch I_D-V_D from zero to 200 krad(SiO_2). Similar to the results of the original C-Flash cell in Fig. 10 and 11, the TID tolerance of this new C-Flash cell is also significantly exceeding 100 krad(SiO_2).

Finally, the first FPGA based on enhanced C-Flash cell, RT4G150, is manufactured by 65 nm technology. The propagation delay, using the same design as before, is measured in terms of total irradiated dose. Figure 16 shows the result: there is no observable of speed degradation up to above150 krad(SiO_2). The standby power-supply current (I_{DDSTDY}) is measured simultaneously. Figure 17 shows its slight and gradual increase. These results confirm the aforementioned prediction that Flash cell dictates the TID tolerance of Flash-based FPGA.

VII. CONCLUSION

In 65 nm technology, non-volatile memory N-Flash based FPGA's TID tolerance is dominated by its N-Flash configuration cell. The softness of N-Flash cell causes the TID tolerance significantly below 100 krad(SiO_2).

C-Flash memory controlled NMOSFET switch can be implemented for configuring FPGA. The TID hardness nature of C-Flash cell can significantly enhance the FPGA's TID tolerance to over 100 krad(SiO_2).

The retention of programmed P-Flash is C-Flash cell is an issue that caused by the voltage drop between gate-drain and body (n-well)-drain. A PMOS inserting between the P-Flash drain and N-Flash drain will reduce the voltage drops and resolve the issue.

Based on retention-reliability enhanced C-Flash cell, 65 nm FPGA RT4G150 demonstrates that, comparing to 65 nm FPGA using N-Flash cell, the hardness is significantly improved to over 150 krad(SiO_2).

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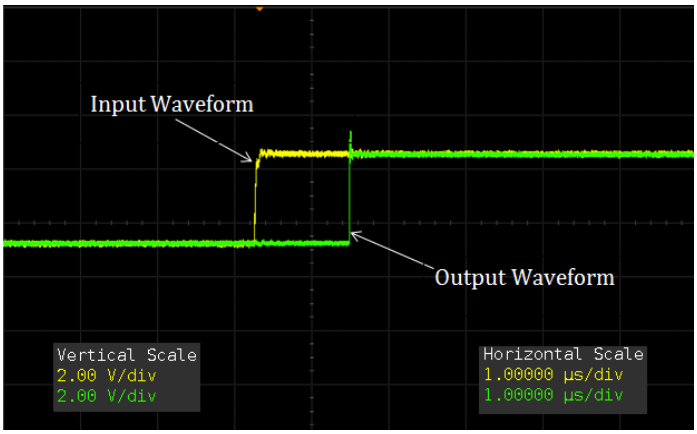
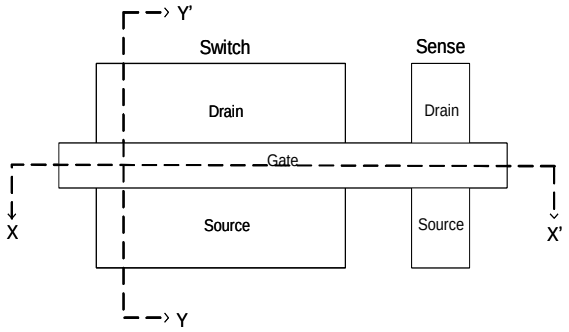
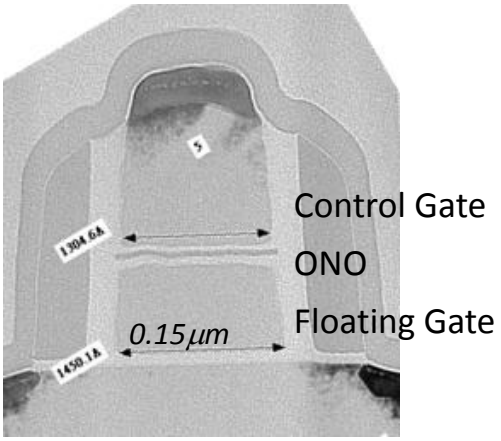


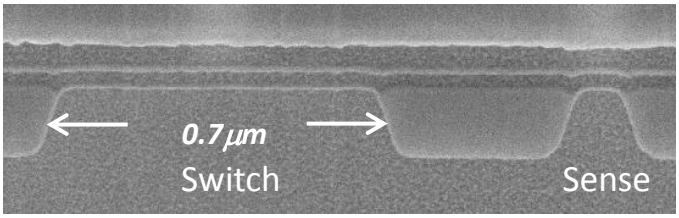
Fig. 1 Oscilloscope captures show the distance between output and input switching edges is the propagation delay of a inverter chain design in FPGA.



(a)



(b)



(c)

Fig. 2 (a) Layout of the Flash cell: each cell contains one switch and one sense FG transistor; the control gate and FG are shared by both the switch and sense transistor. (b) TEM micrograph showing the cross-section of Y-Y' cut. (c) SEM micrograph showing the cross-section of X-X' cut.

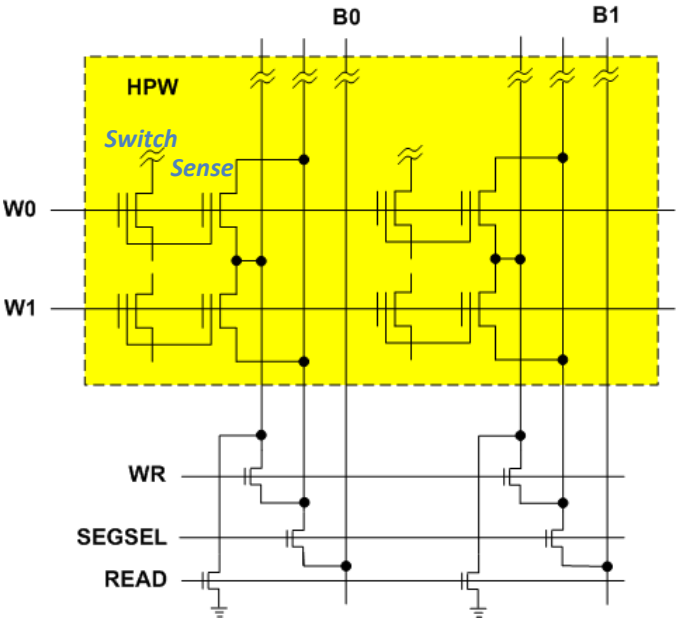


Fig. 3 Schematics illustrate a 2 × 2 N-Flash array showing the basic operation architecture.

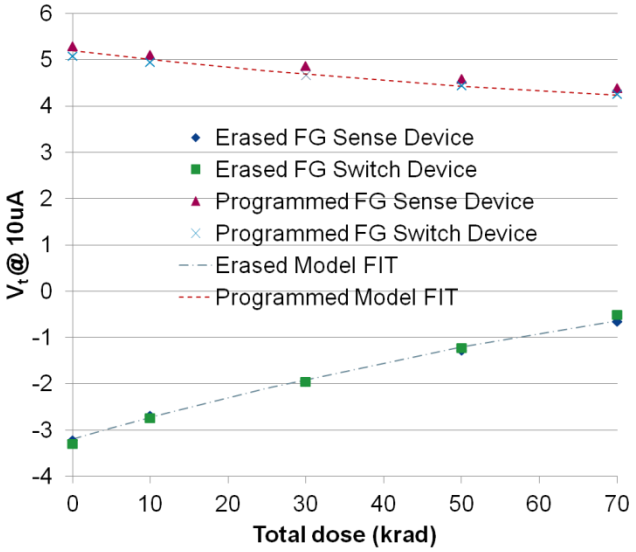


Fig. 4 Plots show TID effects on the V_T shift of N-Flash configuration cell.

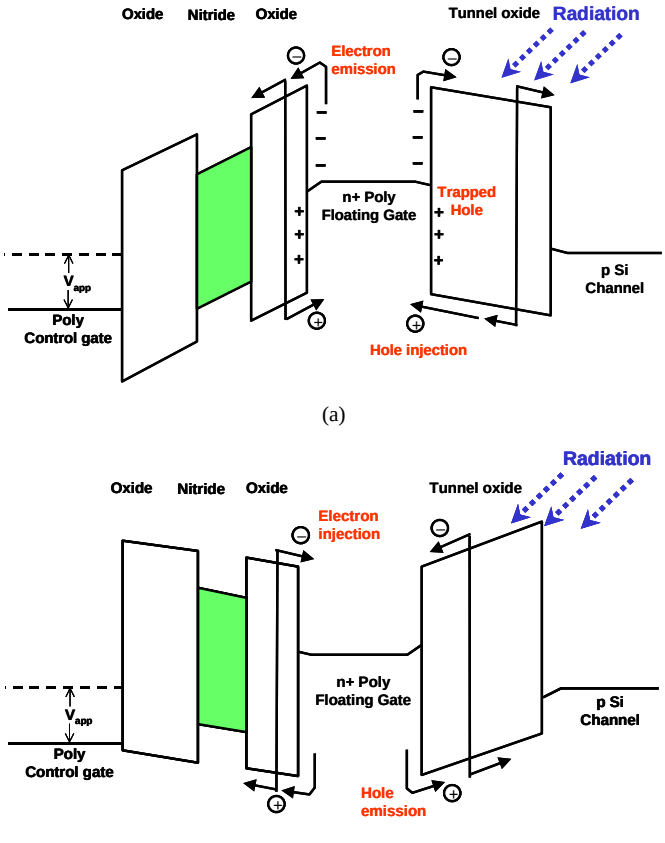
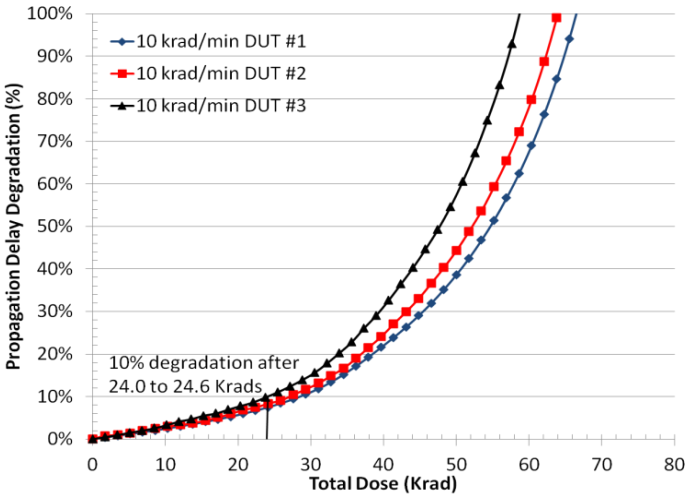


Fig.5 Graphs illustrate physical mechanisms of (a) V_T shifted to lower in programmed N-Flash including electron emission, hole injection and hole trapping and (b) V_T shifted to higher in erased N-Flash including electron injection and hole emission.



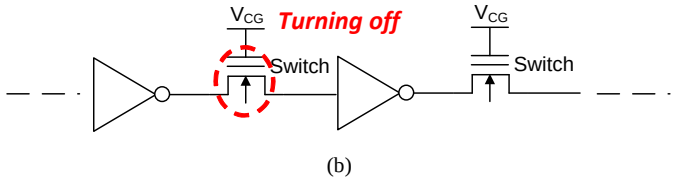


Fig. 6 Plots show TID effects on the degradation of propagation delay of an inverter chain in 65 nm N-Flash based FPGA.

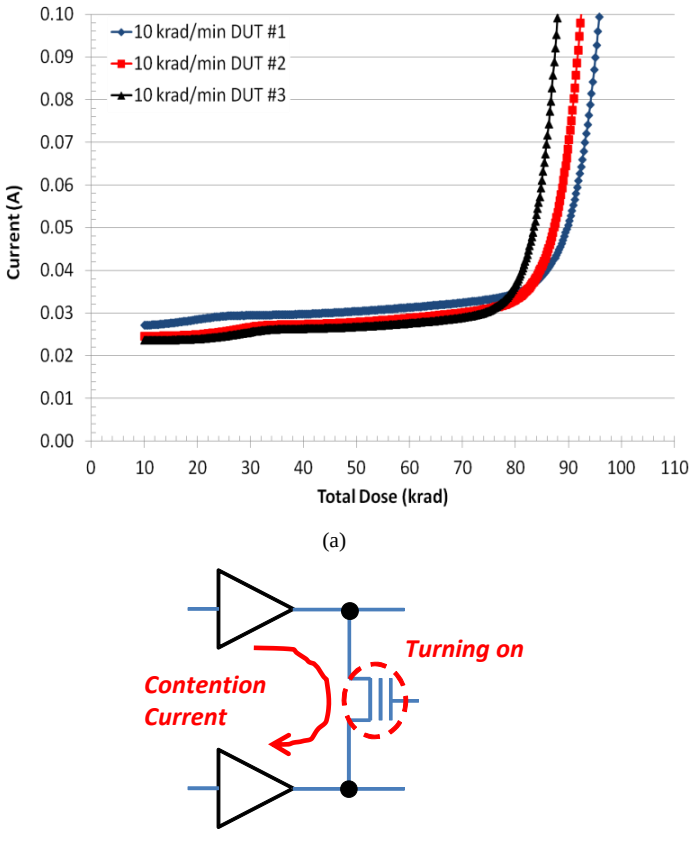


Fig. 7 Plots show TID effects on the degradation of core static power supply current in 65 nm N-Flash based FPGA.

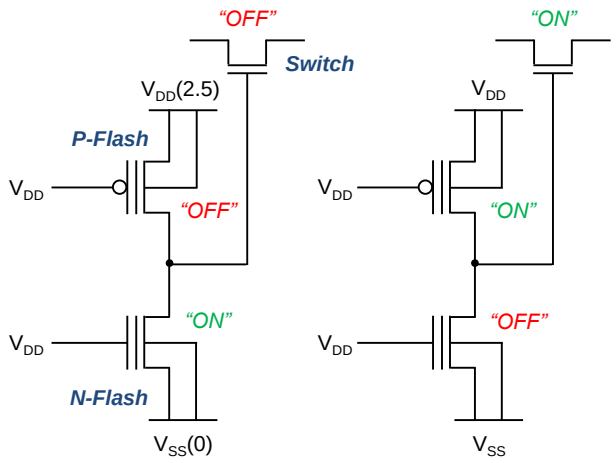


Fig. 8 Schematics illustrate Complementary Flash cell at switch-on and switch-off state.

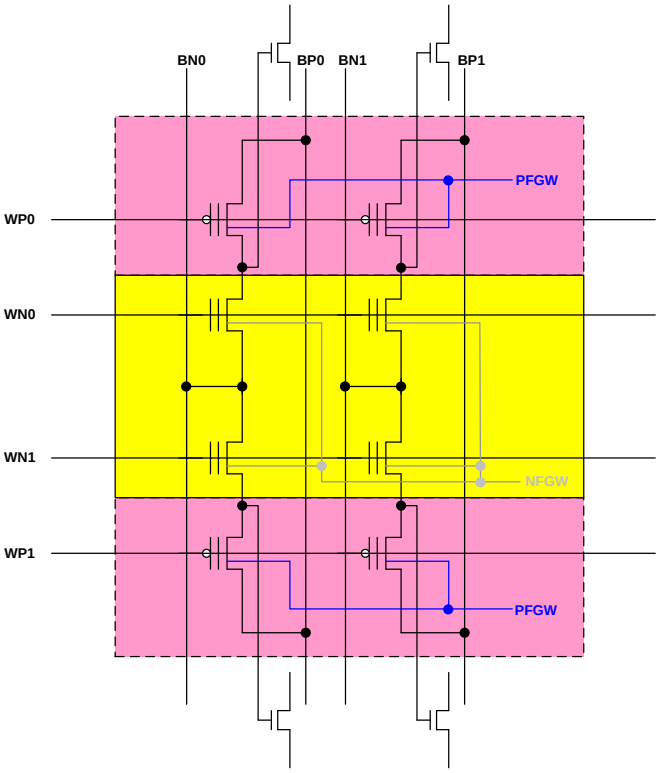
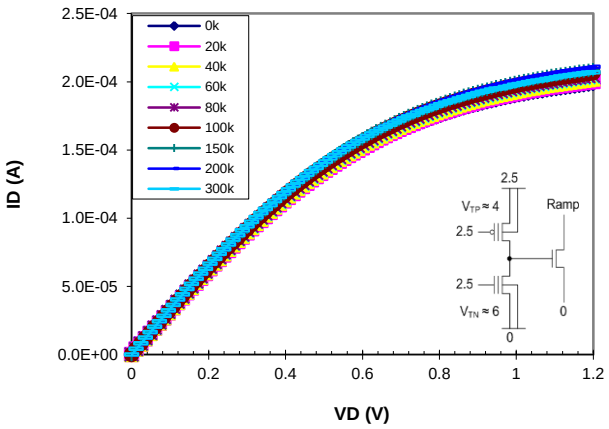


Fig. 9 Schematics illustrate 2 × 2 arrays architecture of C-Flash cell.



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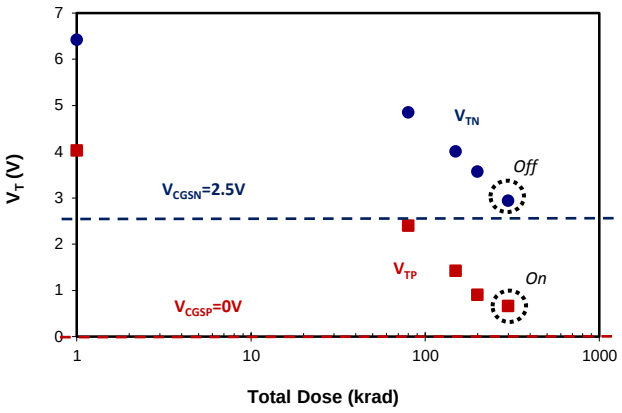
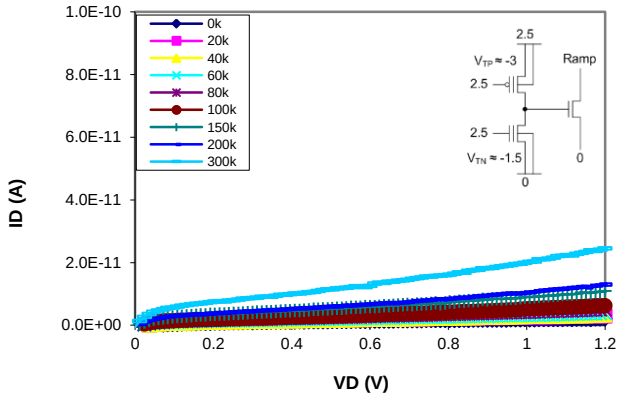


(b)

Fig. 10 Switch-on C-Flash TID characteristics for 0 to 300krad (a) switch I_D-V_D, (b) N-Flash and P-Flash V_T shift.



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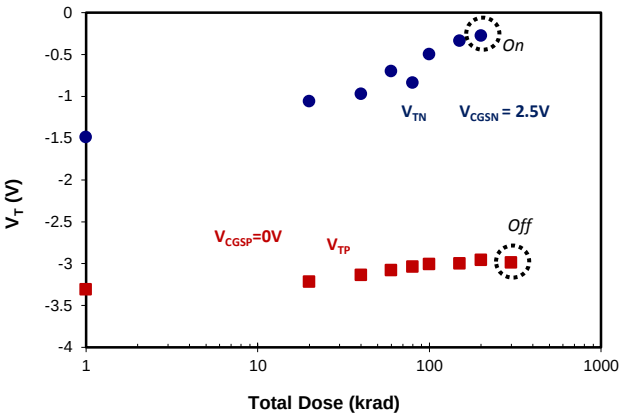
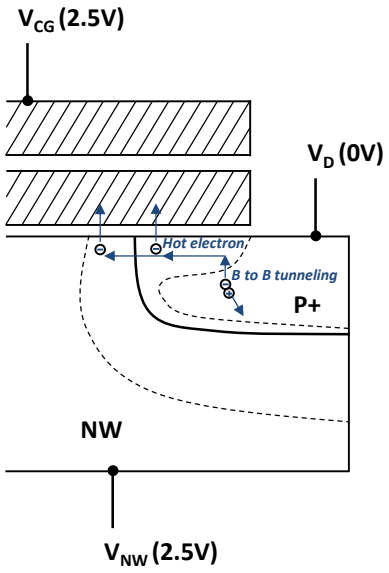
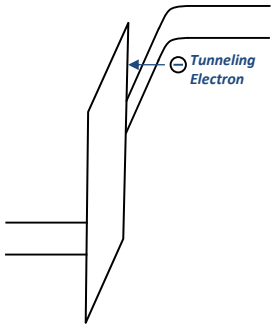


(b)

Fig. 11 Switch-off C-Flash TID characteristics for 0 to 300krad (a) switch I_D-V_D, (b) N-Flash and P-Flash V_T shift.



(a)



(b)

Fig. 12 Schematics illustrate (a) band-to-band tunneling induced hot-electron injection, (b) energy-band diagram showing band-to-band tunneling.

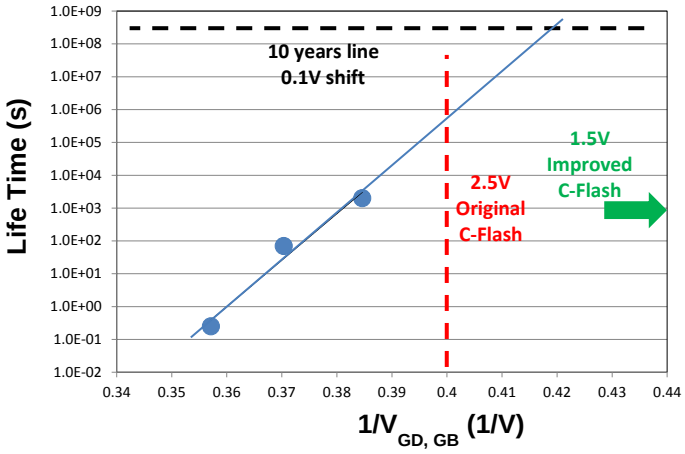


Fig. 13 Retention test results of P-Flash device: V_G and V_S are fixed at 2.5 V while V_D is varied. Using V_T shift of 0.1 V as the critical criterion lifetime versus $1/V_{GD}$ is plotted here. Line marked 2.5 V indicates the lifetime of the old C-Flash.

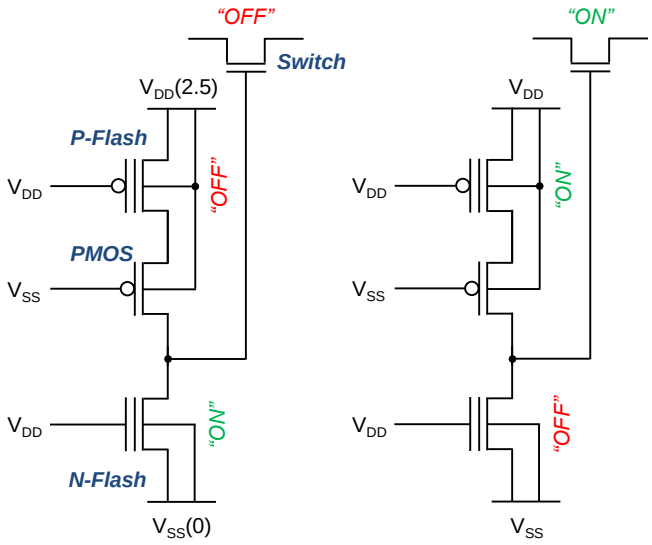
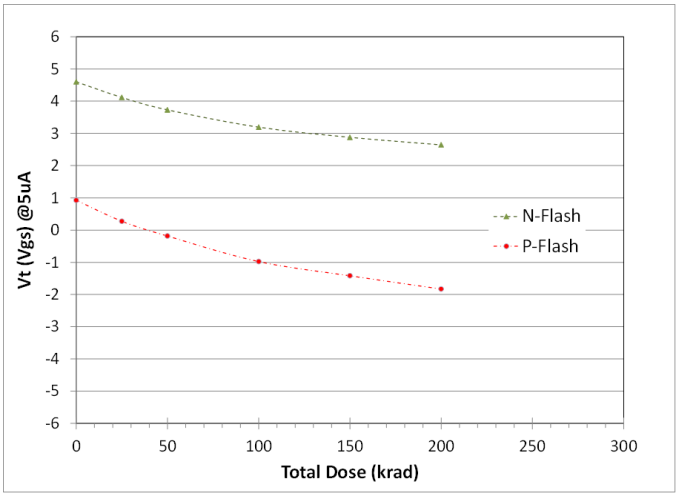
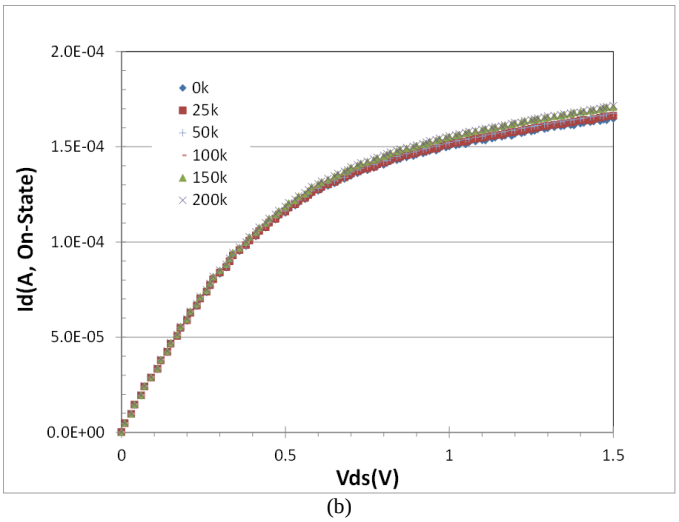


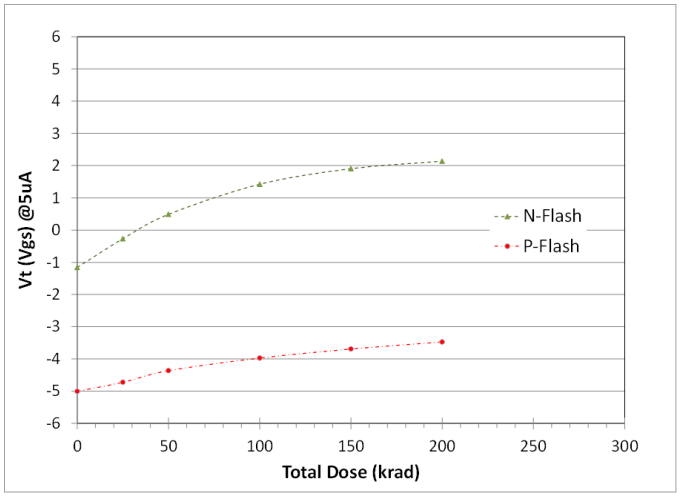
Fig. 14 Schematics illustrate the new Complementary Flash cell at switch-on and switch-off state.



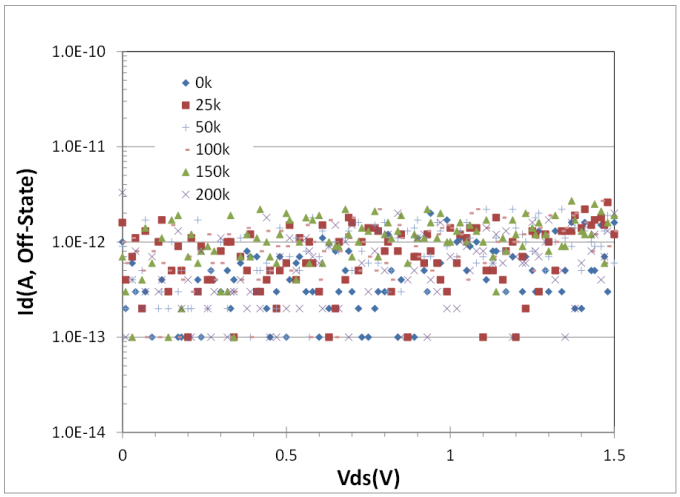
(a)



(b)



(c)



(d)

Fig. 15 Plots illustrate TID characteristics of C-Flash cells: (a) V_T shifts in switch-on state and (b) I_D-V_D of the switch; (c) V_T shifts in switch-off state and (d) I_D-V_D of the switch.

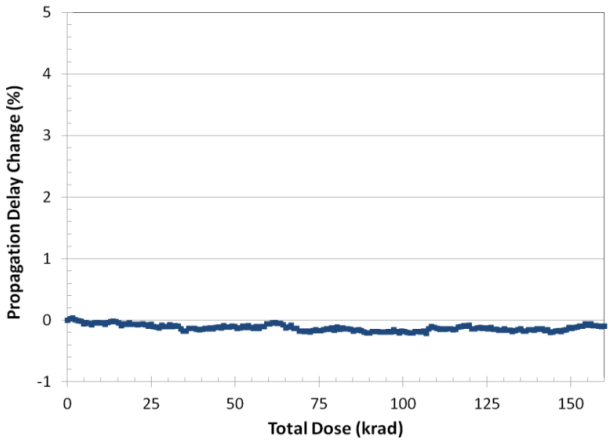


Fig. 16 Plots illustrate TID characteristics of C-Flash cells: (a) V_T shifts in switch-on state and (b) I_D-V_D of the switch; (c) V_T shifts in switch-off state and (d) I_D-V_D of the switch.

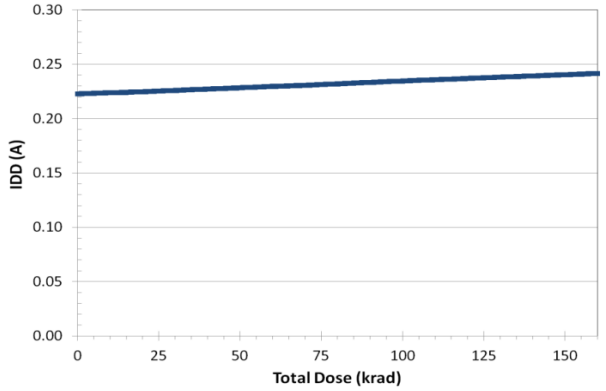


Fig. 17 Plots illustrate TID characteristics of C-Flash cells: (a) V_T shifts in switch-on state and (b) I_D-V_D of the switch; (c) V_T shifts in switch-off state and (d) I_D-V_D of the switch.