



# **Designing with Microsemi SoC FPGAs for Industrial and Motor Control Solutions**

**WP0189 White Paper**

# Designing with Microsemi SoC FPGAs for Industrial and Motor Control Solutions

Industrial systems usually consist of a combination of microcontrollers and FPGAs. The Microsemi<sup>®</sup> SmartFusion<sup>®</sup>2 SoC FPGA-based motor control solution is an example of how an integrated device is more advantageous for industrial designs. This white paper highlights features of the SmartFusion2 device family that are useful in industrial systems and the benefits of using this device over traditional architectures using the concept of total cost of ownership (TCO).

## Introduction

Device selection in industrial systems requires consideration of several factors. Some of these factors are:

- Performance
- Cost of engineering change
- Time-to-market
- Skill set of the personnel
- Possibility of reusing existing IP/libraries
- Cost of field upgrades
- Low power and low cost

Recent developments in the industrial market have driven the demand for high-performance, low-power FPGA devices with a high-level of integration. Designers prefer networked communication over point-to-point communication, which means additional controllers may be necessary for communication, indirectly increasing the bill-of-materials (BOM), board size, and associated non-recurring engineering (NRE) costs.

TCO is a concept used to analyze and estimate the lifetime cost of an acquisition. It is a superset of all the direct and indirect costs associated to a design. These can include engineering costs, cost of installation and maintenance, BOM, and NRE (R & D) cost among others. It might be possible to minimize on the TCO by considering system-level factors, in turn leading to sustainable long-term profitability.

Microsemi offers SmartFusion2 SoC FPGAs with a hard ARM<sup>®</sup> Cortex<sup>®</sup>-M3 microcontroller and IP integration, cost optimized packages, and features to reduce BOM and board size. With low power consumption and wide temperature range, these devices can be reliably operated under extreme conditions without cooling fans. Integrating a hard ARM Cortex-M3 IP with the FPGA fabric also allows greater design flexibility and faster time-to-market. Microsemi offers an ecosystem with several multi-axis motor control reference designs and IPs for motor control algorithm development, which makes it easy to transition from a multi-processor based solution into a single device solution, that is, the SoC FPGA.

## Factors affecting TCO

The following are some factors that affect the TCO of a system.

### Long Life Cycle

FPGAs can be reprogrammed even after they are deployed in the field. This extends the product life cycle, allowing designers to focus on development of new products with faster time-to-market.

### BOM

Microsemi's flash-based FPGAs do not require boot PROM or flash MCU to load the FPGA at power up. They are level zero non-volatile/instant-on devices. Unlike SRAM based FPGAs, Microsemi's flash based FPGAs do not require additional power up monitors as flash switches do not brown out.

## Time-to-Market

The extreme competition among OEMs forces more product differentiation and faster time-to-market. The availability of several tested IP blocks reduces design time considerably. Several IP blocks required to build industrial solutions are already available, while several more blocks are currently being developed. Another unique advantage that is presented by an SoC is debugging FPGA designs. To debug FPGA designs, the microcontroller subsystem (MSS) can be leveraged to extract information from the FPGA through a high-speed interface for debugging.

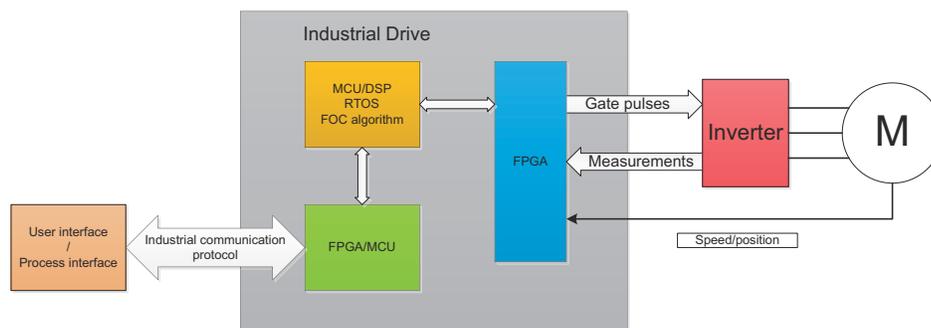
## Cost of Engineering Tools

Contrary to popular notions that FPGA tools are expensive, the Microsemi Libero® System-on-Chip (SoC) or integrated development environment (IDE) required for FPGA development is available with a free gold license. A paid license is only required for development on high end devices.

## Industrial Drive Systems

Industrial drive systems consist of a motor control component and a communication component. The motor control component contains logic to drive the inverter and protection logic. The communications component enables supervisory control to initialize and modify run time parameters.

In a typical drive, multiple controller devices may be used to implement the drive logic. One device may perform computation related to the motor control algorithm, while a second device may run tasks related to communication, and a third device may run tasks related to safety.



**Figure 1: Industrial Drive Systems**

## Multi-Axis Motor Control

Industrial motor control applications traditionally use microcontrollers or digital signal processing (DSP)s to run complex algorithms required for motor control. In most traditional industrial drives, FPGAs are used along with microcontrollers or DSPs for data acquisition and fast acting protections. Apart from data acquisition, pulse width modulation (PWM) generation and protection logic, FPGAs did not play a major role in implementing the motor control algorithm traditionally.

The approach that uses a microcontroller or DSP for implementing motor control algorithms is not easily extendable to control more than one motor running at independent speeds (multi-axis motor control). Microsemi SmartFusion2 device can implement an integrated and complete multi-axis motor drive control using a single device.



### ***PI Controller***

The proportional-integral (PI) controller is a feedback mechanism that is used to control a system parameter. The PI controller has two tunable gain parameters which control the dynamic response of the controller—the proportional and integral gain constants. The proportional component of the PI controller is a product of the proportional gain constant and the error input, while the integral component is a product of the accumulated error and the integral gain constant. The two components are then added together. The integral stage of the PI controller can cause instability in the system because of uncontrolled increase in the data value. This uncontrolled rising of data is called wind-up. All PI controller implementations include an anti-windup mechanism which ensures that the controller output is limited. The Microsemi PI controller IP block uses a hold-on-saturation algorithm for anti-windup. The block also offers additional features to set the initial value of the output.

### ***FOC Transformations***

FOC is an algorithm, which can supply optimal current to a motor by determining and controlling the torque and magnetization current components independently. In permanent magnet synchronous motors (PMSMs), the rotor is already magnetized, and hence the current supplied to the motor contributes to torque only. FOC is computationally intensive, but the Microsemi motor control reference design has been built to optimally use device resources. The FOC algorithm consists of the Clarke, Park, inverse Clarke, and inverse Park transforms.

### ***Position and Speed Estimator***

FOC needs precise rotor position and speed as inputs. Determining rotor angle accurately is essential to ensure low power consumption. Adding physical sensors to determine position and speed add to the system cost and reduce reliability. Sensorless algorithms help in eliminating the sensor, but increase the computational complexity.

### ***PLL***

The phase-locked loop (PLL) is used to synchronize signals. PLLs are useful in several applications, such as angle estimation and grid-synchronization of inverters.

### ***Rate Limiter***

The rate limiter block enables a smooth change of a variable or input to the system. For example, in a motor control system, if there is a sudden change in desired speed of the motor, the system may become unstable. To avoid such scenarios, a rate limiter block is used to transition from the initial speed to the desired speed. The rate limiter block can be configured to control the rate of change.

### ***Space Vector Modulation***

The space vector modulation block improves DC bus utilization and eliminates short pulses to transistor switches. It improves DC bus utilization by 15% compared to using sinusoidal PWM.

### Three-Phase PWM Generation

At the end of all computations, the three phase motor voltages are available. The voltages are used to generate switching signals for transistors in the inverter. The PWM block produces switching signals for six (three high-side and three low-side) transistors, and has advanced features such as dead time and delay time insertion. The programmable dead time insertion feature helps avoid a catastrophic short circuit condition on an inverter leg which could occur because of the transistor turn-off time. The block also has a programmable delay time insertion feature, which allows synchronization of analog-to-digital converters (ADC) measurement with PWM signal generation. The block can be configured to work with inverters consisting of N-MOSFETs only or both N-MOSFETs and P-MOSFETs.

### Debugging FPGA Designs in SoC

Generally, debugging a design on a microcontroller is relatively easier compared to debugging on an FPGA. In an SoC, the high performance of an FPGA can be utilized, while retaining the advantage of faster debugging in a microcontroller. The microcontroller subsystem and the FPGA fabric in the Microsemi SmartFusion2 SoC FPGA can communicate with each other through an AMBA APB or AXI bus. This allows injecting test data into the FPGA fabric, or logging debug data from the FPGA fabric, which in-turn helps in visualizing internal data at runtime for real-time debugging. The firmware code can be run in steps and breakpoints can be set in the code to analyze the FPGA register data.

The SmartFusion2 SoC FPGA based multi-axis motor control solution connects to a host PC through USB, and communicates with a graphical user interface (GUI) to start and stop the motor, set motor speed value and other system parameters, and plot upto four system variables such as motor speed, motor currents, and rotor angle.

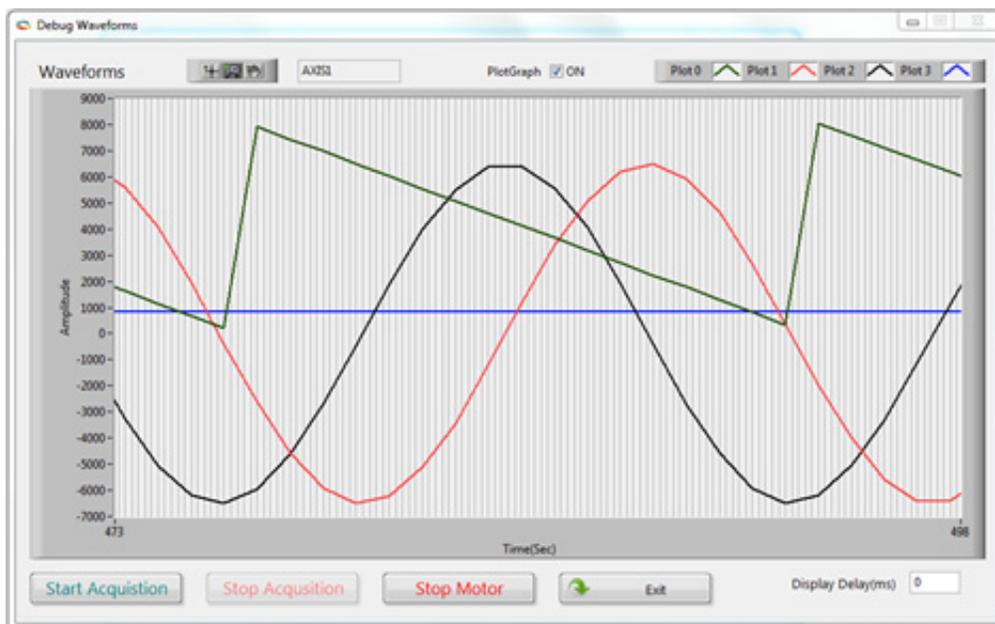


Figure 4: Screenshot of the GUI - Plotting Internal Parameters: Rotor Angle (green),  $V_{\alpha}$  (red),  $V_{\beta}$  (black), Motor Speed (blue)

## **Ecosystem**

Microsemi provides a rich set of IP libraries consisting of IP blocks for several motor control functions that were discussed in previous sections. These blocks are customizable easily and can be ported across Microsemi devices. These blocks can be configured and connected together graphically using SmartDesign tools of Libero SoC software. With the help of these IP blocks, designers can significantly reduce the time required to implement the motor control algorithm in FPGA.

These IP blocks have been tested with motors running at speeds as high as 30,000 RPM and switching frequency of 400 kHz.

## **Industrial Communication Protocols**

The trend in industrial networks is to migrate towards faster communication through networks instead of point-to-point communication. Implementation of such high speed communication demands for support of higher bandwidths which is not easy for a microcontroller or DSP to handle along with motor control algorithm simultaneously. In many cases, an additional microcontroller or FPGA is used to handle the communication with each motor controller. Commonly used Ethernet based protocols are Profinet, EtherNet/IP and EtherCAT standards that are still evolving. Other protocols include CAN and Modbus. The advantage of using an SoC in this context is supporting multiple industrial Ethernet protocol standards on a single FPGA platform.

Depending on the end system goals, it might be possible to optimize the system for cost by reusing IP and protocol stacks (for communication), or optimize performance by carefully partitioning of the functions into hardware (FPGA) and software (ARM Cortex-M3 processor).

Microsemi's SmartFusion2 SoC FPGA has built-in CAN, high-speed USB, and a gigabit Ethernet block as part of the MSS. A high-speed SERDES block is available for implementing protocols involving serial data transfer.

Several IP blocks are available through Microsemi's IP partners. For more information, refer to <http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

## **Security**

SmartFusion2 SoC FPGAs offer several design and data security features. Design security features such as differential power analysis (DPA) certified anti-tamper protection and cryptographic features help protect the user's IP. The SoC FPGA devices also include data security features such as error correction codes (ECC) hardware accelerators, AES-128/256, and SHA-256 services. For data security, EnforcIT IP Suite and CodeSEAL software security building blocks are available. The EnforcIT IP suite contains a set of customizable cores (as netlists), effectively moving security layers into hardware. CodeSEAL injects counter measures into the firmware, and can be used independently, or as an enhancement with EnforcIT. The flexibility in implementing protocols allows designers to use multiple layers of security to authenticate incoming messages from a central supervisory controller.

## **Reliability**

High reliability requirements are driven by growth in safety standards in several markets. SmartFusion2 is designed to address the requirements of high availability, safety critical, and mission critical systems. The following are some reliability features available in SmartFusion2 SoC FPGAs.

### **SEU Immune Zero FIT Rate Configuration**

High reliability operations require single event upset (SEU) immune Zero failure in time (FIT) rate FPGA configuration. The SmartFusion2 architecture is immune to alpha or neutron radiation because it employs flash memory to configure transistors used in the routing matrix and logic modules. SRAM based FPGAs can have FIT rates from 1k to 4k at sea level and much more at 5000 feet above sea level. The acceptable FIT rates for high reliability applications are less than 20, which makes SmartFusion2 most suitable for them.

## **EDAC Protection**

An error detection and correction (EDAC) controller is present in SmartFusion2 devices to protect against SEU errors in the MSS memories, which are increasingly more common even at the ground level.

## **No External Configuration Device**

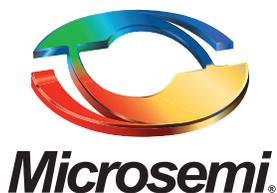
In complex systems with a large number of FPGAs, using an external configuration device reduces reliability. On powering up, the FPGA takes time to configure and this brings in design complexities in applications that use multiple FPGAs. SmartFusion2 SoC FPGAs contain the configuration memory within the device, which has an added advantage of turning on as soon as the device is powered up.

## **Military Temperature Grade Devices**

SmartFusion2 SoC FPGA devices are fully tested for military temperature conditions. Military grade devices are available between 10k and 150k logic element variants along with security features which allow access to cryptographic accelerators and data security features.

## **Summary**

Microsemi's SmartFusion2 SoC FPGA device offers several features which reduce TCO in industrial designs using highly optimized motor control IP blocks and proven reference designs. Customers migrating from microcontrollers will be able to reuse some of their legacy code, while FPGA designers will be able to leverage the FPGA fabric and the ARM Cortex-M3 processor to create an efficient architecture that allows both the motor control blocks and communication blocks to reside in a single device. The presence of an ARM Cortex-M3 processor enables flexible designs and intelligent partitioning that can be optimized for performance and cost. The MSS can also accelerate debugging FPGA designs by injecting and logging data in runtime. The SmartFusion2 platform also provides a wide range of options in implementing industrial communication protocols. It offers several security features for both design and data security. It also provides features to meet high reliability requirements. The SmartFusion2 family of devices is supported by a strong ecosystem that can help in development of industrial solutions with minimal TCO.



**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo,  
CA 92656 USA

**Within the USA:** +1 (800) 713-4113  
**Outside the USA:** +1 (949) 380-6100  
**Sales:** +1 (949) 380-6136  
**Fax:** +1 (949) 215-4996

**E-mail:** [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

© 2015 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at [www.microsemi.com](http://www.microsemi.com).

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.