Package Miniaturization: Embedded Die Technology

Microsemi's embedded technology provides unparalleled miniaturization in a proven robust package capable of meeting the most stringent quality requirements.

Microsemi has developed a technology for embedding the die between PCB laminations that enables the die to become a near zero area occupancy.

This allows integrators to reduce the size of their device or maintain size with additional functionality.

Case studies show that in certain applications the technology can provide real estate savings of up to 400% of the original PCB area.

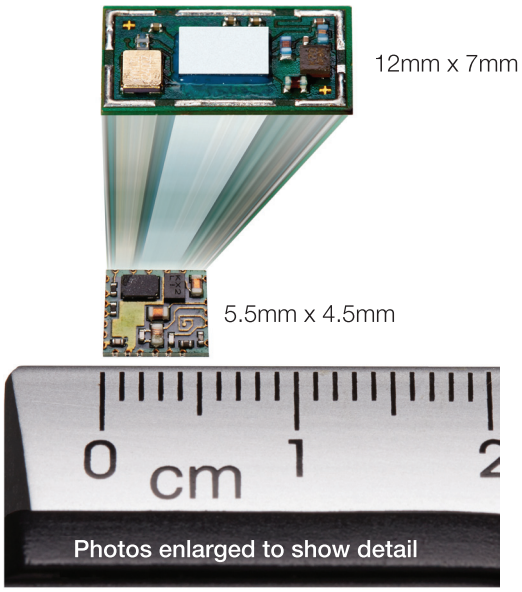
This technology offers customers the flexibility to design a package and module footprint that can be adapted to meet the system requirements.

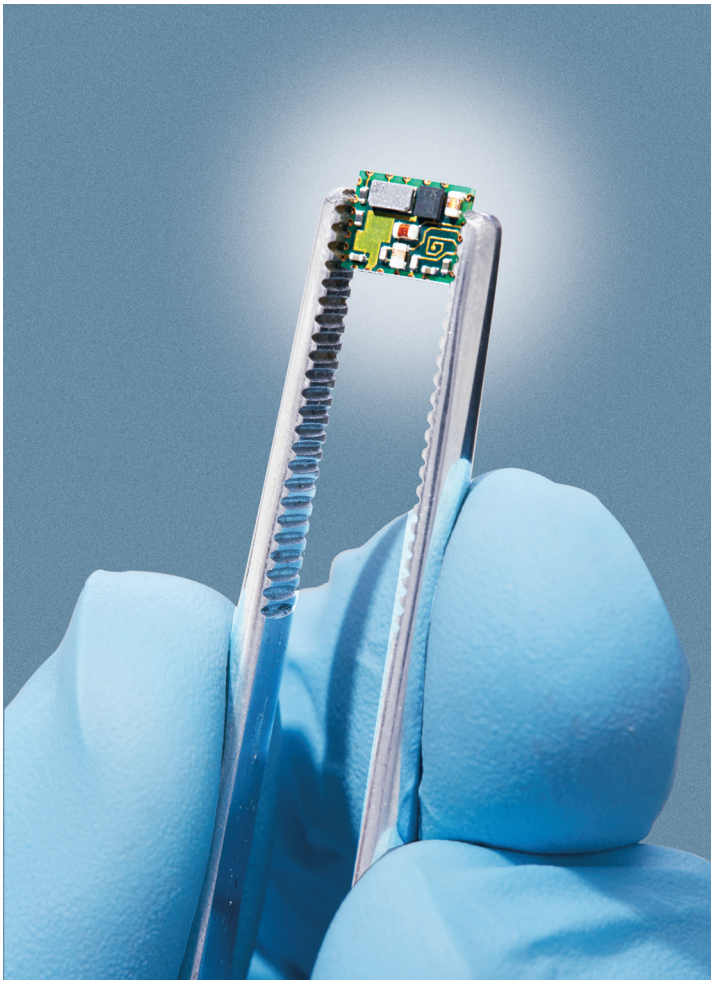
Further features include increased robustness by providing a mechanical barrier supporting the die and increased security against counterfeiting.

Qualified to Mil standard for implantable devices proves package integrity and reliability.

Typical Footprint Reduction

Both boards shown below contain: 1 x transceiver, 1 x crystal, 1 x SAW filter, 4 x inductors, 2 x resistors and 5 x capacitors. Consider how this degree of miniaturization could help you achieve your product design goals.





Applications

- Medical Implants
- Wearables
- Security
- Military
- Industrial sensing

Features

Significant reductions in XY by:

- Embedding die within substrate
- Vertical component integration
- Increased security against counterfeit
- Reduced signal path loss
- Robustness (vibration)
- Inbuilt RF screening

Microsemi Corporation

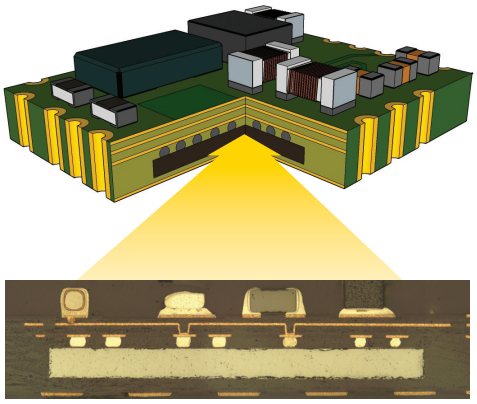
One Enterprise, Aliso Viejo, CA 92656 Ph: 949-380-6100 Fax: 949-215-4996 sales.support@microsemi.com www.microsemi.com

Rev. 1.0 6.14

Package Miniaturization: Embedded Die Technology

Microsemi
Power Matters.™

Module Parameters	
Minimum substrate thickness	450um (assumes 4 copper layers and minimum 75um die thickness)
Minimum feature size	75um
Minimum module XY size	die XY dimension + 1.4mm
Encapsulation	yes
Traceability	yes
Embedded components	yes
SMD components on top layer	yes
Packaging	JEDEC tray or tape and reel.
Footprint	LGA



Die is embedded inside circuit board, reducing board size, increasing security and improving performance.

Test Group	Test Standard	Result
Moisture Sensitivity Preconditioning:	JESD22-A113F, IPC/JEDEC J-STD-020 Level 2a	
Temperature Cycling	-40°C to 60°C, 5 cycles	
Bake	125°C for 24 hrs	✓
Moisture Soak	120 hrs, 60°C/60%RH	
3x Reflow	JESD22-A113F, 260°C	
Thermal Stress:		
Low Temperature Storage	-40°C, 72 hrs	
High Temperature Storage	125°C, 72 hrs	✓
Temperature Cycling	MIL-STD-883 Method 1010, Condition B, -55°C to 125°C, 20 cycles	
Mechanical Stress:		
Mechanical Shock	MIL-STD-883 Method 2002, Condition B, 5 shocks, 1500g	
Mechanical Vibration	MIL-STD-883 Method 2007, Condition A, 20-2000Hz, 20G	✓
Constant Acceleration	MIL-STD-883 Method 2001, 10,000G	
Steady State Life Testing:		
Low and High Temperature Testing	0°C, 55°C	✓
HTOL	125°C, 1000 hrs	
Exposure:		
Resistance to Solvents	MIL-STD-883 Method 2016	✓
ESD	MIL-883 Method 3015, 1000V HBM	
Assembly:		
Component Shear	MIL-STD-883 Method 2019/2011	
External physical dimensions	MIL-883 Method 2016	✓
Solderability	MIL-STD-883 Method 2003.8/2022.2	
Ionic Cleanliness	IPC-TM-650	

Microsemi Corporation

One Enterprise, Aliso Viejo, CA 92656 Ph: 949-380-6100 Fax: 949-215-4996 Sales.Support@microsemi.com www.microsemi.com

Rev. 1.0 5.14