Libero SoC PolarFire

Release Notes

3/2017

Microsemi
Power Matters.™

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions;

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Revision History

Revision 1.0

This is the initial release of these Release Notes.

Revision 2.0

Revision 2.0 includes a critical Synplify bug fix and steps to follow to use the new Synplify Pro release that includes the bug fix.

Alert

A critical bug has been found in the Windows version of Synplify Pro included in this Libero SoC release. A beta version of Synplify Pro (L2016.09M_PolarFire_Beta) which has the bug fix is available for download. Follow these steps to use the updated version of Synplify Pro along with Libero SoC PolarFire.

1. Download the Synplify Pro release from here.
2. Install Synplify Pro L2016.09M_PolarFire_Beta
3. Change the Libero SoC Tool Profile for Synthesis (**Libero SoC > Project > Tool Profiles > Synthesis**) to point to the location of the newly-installed Synplify Pro executable (in the Synplify install folder, “bin/synplify_pro.exe”)
4. Make sure that the updated tool profile for Synthesis is the Active profile (The Active radio button is checked).

Reference Documents

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide (Updated 02/2017)

PO0137: PolarFire FPGA Product Overview (02/2017)

DS0141: PolarFire FPGA Datasheet (02/2017)

UG0680: PolarFire FPGA Fabric User Guide (02/2017)

UG0684: PolarFire FPGA Clocking Resources User Guide (02/2017)

UG0686: PolarFire FPGA User I/O User Guide (02/2017)

UG0677: PolarFire FPGA Transceiver User Guide (02/2017)

UG0685: PolarFire FPGA PCI Express User Guide (02/2017)

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide (02/2017)

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide (Updated 02/2017)

UG0676: PolarFire FPGA DDR Memory Controller User (02/2017)

UG0748: PolarFire FPGA Low Power User Guide (02/2017)

UG0743: PolarFire FPGA Debugging User Guide (02/2017)

UG0714: PolarFire FPGA Programming User Guide (02/2017)

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide (02/2017)

UG0726: PolarFire FPGA Board Design User Guide (02/2017)

UG0752: PolarFire FPGA Power Estimator User Guide (02/2017)

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide (02/2017)

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide (02/2017)

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide (02/2017)

DG0755: PolarFire FPGA JESD204B Interface Demo Guide (02/2017)

Contents

1 Libero SoC PolarFire™ Software Release Notes

The Libero® system on chip (SoC) PolarFire™ release is specific to designing with Microsemi PolarFire FPGAs. PolarFire FPGAs are the fifth generation nonvolatile FPGA devices from Microsemi, built on 28-nm flash technology. The PolarFire cost-optimized FPGAs deliver lowest power at mid-range densities.

For more information about the Libero SoC PolarFire release, see the Microsemi website.

1.1 Overview

The Libero SoC PolarFire release provides a comprehensive toolset that allows users to create designs targeting the PolarFire FPGA family.

The Libero SoC PolarFire release includes the following features:

- Design Creation: SmartDesign, VHDL, Verilog, and SystemVerilog for design and test bench development
- Pre-synthesized Design Simulation using ModelSim ME Pro featuring mixed-language simulation
- Synthesis using Synopsys Synplify Pro ME
- Constraint Management: I/O constraints, timing constraints, floorplan constraints, and netlist constraint management. The I/O Constraint Editor has enhanced capabilities to manage Transceiver and Memory Interface (DDR) assignments.
- Timing-driven Place and Route, including Min Delay Repair and Multiple Pass options
- Static Timing Analysis with SmartTime using advance timing data
- Power Analysis with SmartPower using advance power data
- Chip Planner – For floorplanning and cross-probing from the Chip Planner to the post-compile flattened netlist view (only in Netlist Viewer embedded inside Chip Planner) or from SmartTime
- Netlist Viewer – For probing into the netlist at various design stages: pre-synthesis (RTL view), post-synthesis (hierarchical view) and post-compile (flattened view).

1.2 Limitations of This Release

This release has the following limitations:

- Programming and SmartDebug are not supported.
- Post-synthesis and post-layout simulations are not supported.
- Max Delay Slacks and Clock Frequencies reported in the Timing Reports may be overly pessimistic and slower than the actual PolarFire device's timing performance.
- IBIS generation is not supported.
- Block Flow is not supported.

1.3 System Requirements

- Windows 7 OS or Windows 8.1 OS
- RHEL 5 and RHEL 6*, CentOS 5 and CentOS 6*

- 64-bit OS
- A minimum of 32 GB RAM

Note: Setup instructions for using Libero SoC on Red Hat Enterprise Linux OS are available on the Libero SoC Documents web page.

1.4 Device Support

Table 1 Libero SoC PolarFire Device Support

Device	Package	Speed Grade	Core Voltage	Required License
MPF200TS_ES	Fully bonded package	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
MPF300T_ES	FCG1152E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG484E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG784E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCSG536E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCVG484E	-1, STD	1.0/1.05V	Eval/Platinum
MPF300TS_ES	FCG1152E	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCG484E	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCSG536E	-1, STD	1.0 /1.05V	Eval/Platinum

2 PolarFire Features

2.1 FPGA Fabric Resources

The fabric is the digital logic section of the PolarFire FPGA, which the user configures with Verilog or VHDL. The PolarFire FPGA fabric consists of the following resource types:

- Logic element – basic building blocks in the FPGA for digital logic design, which consists of sequential logic elements and 4-input LUTS (Look-Up Tables) for combinational functions.
- Embedded memory blocks – large SRAM (LSRAM), microSRAM (µSRAM), and microPROM (µPROM)
- sNVM – Secure Non-Volatile Memory accessible through System Services
- Math Blocks – built-in multiplier, pre-adder, and adder

All PolarFire devices have these resources, but the quantity of each resource type varies with the die and package. For details, see UG0680: PolarFire FPGA Fabric User Guide.

2.2 Clocking Resources

PolarFire devices have rich clocking resources which are crucial to any design project using FPGAs. The PolarFire FPGA has three types of clocking resources:

- Clock routing resources – to support optimal routing of clock networks across the fabric.
- On-chip oscillators – two on-chip RC oscillators (2 MHz and 160 MHz) for generating free-running clocks.
- Clock Conditioning Circuitry (CCC) – A hard block embedded in each corner of the device. Each CCC block consists of two phase-locked loops (PLLs) and two delay-locked loops (DLLs) to provide flexible clock management and synthesis capabilities.
- High Speed I/O Clocks

For details, see UG0684: PolarFire FPGA Clocking Resources User Guide.

2.2.1 Clock Conditioning Circuitry (CCC)

The PolarFire CCCs perform the following functions:

- Frequency synthesis (integer and fractional)
- Spread-spectrum clock generation
- Clock Delay and phase adjustment
- Clock duty-cycle correction

The PolarFire Clock Conditioning Circuitry (CCC) configurator can configure up to four PLL/DLL-based output clocks of different frequencies and phases, with or without clock feedback delay.

2.2.2 Oscillators

PolarFire devices offer two on-chip RC oscillators (2 MHz and 160 MHz) to generate free-running clocks. The oscillators' clocks can be routed to the FPGA fabric, and the Clock Conditioning Circuitry (CCC). The on-chip oscillators are accessible using the oscillator macros available in the Libero SoC IP catalog.

2.3 Embedded Memory Solutions

The PolarFire FPGA fabric has the following embedded memory blocks:

- LSRAM - the embedded 20 KB SRAM blocks (RAM1k20) are arranged in multiple rows within the fabric, and can be accessed through the fabric routing. The LSRAM can be configured to operate in dual-port or two-port modes. LSRAMs can be initialized during power-up. The number of available LSRAM blocks varies with the die.
- µSRAM - the embedded 768-bit SRAM blocks (RAM64x2) are arranged in multiple rows within the fabric, and can be accessed through the fabric routing architecture. The number of available µSRAM blocks varies with the die.
- µPROM - Each PolarFire device has a single embedded non-volatile read-only memory block that can be accessed through the fabric routing resources. The size of the µPROM varies with the die. The µPROM is loaded during device programming.
- sNVM - Each PolarFire device has 56Kbytes of Secure Non-Volatile Memory (sNVM) The sNVM is organized into 221 pages of 236 bytes or 252 bytes depending on whether the data is stored as plain text or encrypted/authenticated data.

See UG0680: PolarFire FPGA Fabric User Guide for details.

2.4 Memory Interface Solutions

The PolarFire DDR subsystem addresses memory solution requirements for a wide range of applications with varying power consumption and efficiency levels. The subsystem can be configured to support DDR4, DDR3, and DDR3L memory devices.

The PolarFire I/O advanced features allow I/O gearing (serial-to-parallel and parallel-to-serial conversion) of multiple FPGA fabric data bits to/from a single device I/O, with clock frequency division between the I/O and the fabric. It can deserialize the high-speed DDR input data and transfer it to FPGA fabric at lower speed. It can also serialize the lower speed FPGA fabric data and transfer the data to high-speed DDR output.

See UG0676: PolarFire FPGA DDR Memory Controller User Guide for instructions to configure the Memory Solution systems.

2.5 PCIe Express Solution

The PolarFire device family supports up to two fully embedded PCI Express interfaces on every device.

PCI Express (PCIe) is a scalable, high-bandwidth serial interconnect technology that maintains compatibility with existing PCI systems. PolarFire devices contain fully integrated PCIe endpoint and root port subsystems with optimized controller blocks that use the physical layer interface of the PolarFire of the PolarFire transceiver for the PCI Express (PCIe) interconnection within the transceiver block.

Each PolarFire device includes two PolarFire embedded PCIe subsystem (PCIESS) blocks that can be configured separately or configured as a pair using the PCIESS configurator in the Libero SoC software. The PCIESS encompasses features from the physical layer of the transceiver and physical coding sublayer block to the application interface to the FPGA fabric.

See UG0685:PolarFire FPGA PCI Express User Guide for details.

2.6 Transceiver Solutions

PolarFire devices include an embedded low-power and performance optimized transceiver, which provides the physical media attachment (PMA) needed for constructing high-speed serial interfaces using PolarFire devices. The transceiver has both the PMA, associated logic of the protocol physical coding sub-layer (PCS) and interfaces to the FPGA fabric included within the device IP. The transceiver has a multi-lane architecture with each lane natively supporting serial data rates from 250 Mbps to 12.7 Gbps.

The transceiver includes all required analog functions for high-speed data transmission between devices over printed circuit boards (PCB) and over high-quality cables. The block is optimized for lower power operation and is suitable for a variety of device-to-device communication protocols.

Transceivers can be configured using the XCVR, Tx_PLL and XCVR_REF_CLK configurators in the Libero SoC software.

For details, see:

UG0677: PolarFire FPGA Transceiver UG,

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide,

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide

2.7 CDR Interface Solutions (SGMII)

The CDR Interface provides an asynchronous receiver and a transmit interface for serial data transfers. This interface can transmit up to 1GbE transfers. It supports serial protocols and other similar encoded serial protocols. The CDR interfaces use a 10:1 gearing ratio to provide a 10-bit data and clock interface for both transmit and receive modes. In receive mode, a clock recovery circuit is used in the lane controller to generate the recovered clock. The IOD CDR configurator is compatible with CoreTSE, CoreTSE_AHB, and CoreSGMII configured in TBI mode.

See UG0686: PolarFire FPGA User I/Os User Guide for details

2.8 Generic I/O Interfaces Solutions

PolarFire devices support a number of interface modes that can be selected to build the required data interface.

For a list of the supported generic I/O interfaces, see Table 24 in UG0686: PolarFire FPGA User I/Os User Guide.

2.9 I/Os and I/O Banks

A rich set of I/O standards is available across different I/O banks and I/O voltages. Two types of I/Os are supported with the following data rates:

- GPIO (General-purpose I/O) – LVDS, LVCMOS, DDR3 1067, QDR II+ 900 Mbps
- HSIO (High-speed I/O) – DDR3 1333, DDR4 1600, LPDDR2 1067, LPDDR3 1333 Mbps

PolarFire devices also include several I/Os with digital features, including I/O gearing.

See UG0686: PolarFire FPGA User I/Os User Guide for details.

2.9.1 I/O Gearing

I/O gearing is the serial-to-parallel and parallel-to-serial conversion of multiple FPGA fabric data bits to/from a single device I/O, with clock frequency division between the I/O and the fabric. It can deserialize the high-speed DDR input data and transfer it to FPGA fabric at lower speed. It can also serialize the lower speed FPGA fabric data and transfer the data to high-speed DDR output. Libero SoC automatically configures these conversion (gearboxes) based on the application settings.

2.10 Miscellaneous

2.10.1 Power-On Reset

PolarFire devices use advanced power-up circuitry to ensure reliable power-up. When the device is powered on, the Power-on Reset (POR) circuitry and the system controller ensure a systematic POR.

See UG0725: PolarFire FPGA Device Power-Up and Resets User Guide for details.

2.11 PolarFire Cores

PolarFire-specific cores are available online for download and use in PolarFire designs. To see the available cores in the IP catalog, inside Libero SoC, select **Defaults** in the Repositories settings (**Project > Vault/Repositories Settings**) to access the following repositories:

www.actel-ip.com/repositories/SgCore

www.actel-ip.com/repositories/DirectCore

www.actel-ip.com/repositories/Firmware

Table 2 PolarFire Cores

Core Name	Description	Core Version
PF_CLK_DIV	Clock Divider	1.0.100
PF_DRI	Dynamic Reconfiguration Interface	1.0.100
PF_INIT_MONITOR	PolarFire Initialization Monitor	1.0.100
PF_IOD_CDR	PolarFire IOD CDR	1.0.100
PF_IOD_GENERIC	PolarFire IOD Generic Interface	1.0.100
PF_NGMUX	Glitchless Clock Mux	1.0.100
PF_XCVR_REF_CLK	Transceiver Reference Clock	1.0.100
PF_DDR4	PolarFire DDR4	1.0.102
PF_DDR3	PolarFire DDR3	1.0.102
PF_OSC	PolarFire RC Oscillator	1.0.100
PF_TX_PLL	Transmit PLL	1.0.100
PF_XCVR	Transceiver Interface	1.0.210

Core Name	Description	Core Version
PF_PCIE	PCI Express	1.0.213
PF_SRAM_AHBL_AXI	PolarFire SRAM (AHBLite)	1.1.105
PF_DPSRAM	PolarFire Dual-Port Large SRAM	1.1.109
PF_TPSRAM	PolarFire Two-Port Large SRAM	1.1.107
PF_URAM	PolarFire Micro SRAM	1.1.106
PF_UPROM	PolarFire Micro PROM	1.0.107
PF_CCC	Clock Conditioning Circuitry	1.0.101

2.12 OEM Synthesis and Simulation Tools

This release includes the Synplify Pro and ModelSim OEM tools.

Synplify Pro L-2016.09M-G5

Use Synplify Pro L-2016.09M-G5 version to take advantage of PolarFire technology mapping. Synplify Pro infers PolarFire elements such as LSRAM, µSRAM, and math blocks. For more information and HDL template examples for inference, see UG0680: PolarFire FPGA Fabric User Guide.

ModelSim ME Pro 10.5c

This release of ModelSim provides new capabilities such as mixed Verilog and VHDL simulation and improved runtime performance. To run ModelSim ME Pro 10.5c, a Libero SoC license other than Silver is required.

Note: For ModelSim ME Pro 10.5c, the FLEXnet version for the vendor daemon and the license server has changed. For floating license operation, ensure that the FLEXnet version of the vendor daemon (mgcld) and the license server (lmgrd) is equal to or greater than 11.13.0.2. Node-Locked license users can continue as before.

2.13 Power Estimator

The PolarFire FPGA Power Estimator v3e is available for download. It is a spreadsheet-like standalone program into which design parameters can be entered to generate a power consumption estimate for the design. See UG0752: PolarFire Power Estimator User Guide for details.

2.14 Known Issues and Limitations

2.14.1 CCC Known Issues

- In PLL configurator, output clock frequency should always be in descending order with the highest clock frequency assigned to the first enabled output clock
- In DLL- Phase gen mode, the secondary output clocks are not getting the phase shifted correctly in simulations.

2.14.2 DDR3/4 Known Issues

- The default DDR3 I/O standard is set incorrectly to LVCMOS18/SSTL18. Use the I/O Attribute Editor or a physical design constraint (PDC) file to set it to SSTL15.

- Placement fails if DDR4 is configured using a bank group address width value of 1. Change the value to 2 (**DDR4 Configurator > General > Bank Group Address Width**).
- The default DDR4 I/O standard is set incorrectly to LVCMOS18/SSTL18. Use the I/O Editor or a PDC file to set it to POD12 for DM/DBI/DQ/DQS and SSTL12 for address/command pins.
- Write transactions may fail depending on the configuration and design. The delay between the write command and the first DQ bit may not match the selected CAS Write Latency (CWL).

  Workaround: Go to the Diagnostic tab of the DDR3/4 configurator. Edit the parameter DFI_T_PHY_WRLAT in the Diagnostic tab to adjust the delay between the Write command and the first DQ bit. Increase or decrease the value based on the difference between the observed CWL and the specified CWL.
- Full Simulation may take about 30 minutes, depending on the machine resources and the simulator used.
- Multi-rank SDRAM is not supported.
- DBI (DDR4) is not supported.

2.14.3 PCIe Known Issues:

- I/O attributes are not supported for dedicated transceiver reference clocks – XCVR_REF_CLK.
- For BFM simulation of AXI master or slave, the simulator may print out a warning message about AHB signals, such as “HRESP”. The warning message can be ignored.

2.14.4 Transceiver Known Issues

- When the lane data rate is less than 500Mbps, only the PMA mode is supported (for PCS fabric width of 10 bits).
- I/O attributes are not yet supported for dedicated transceiver reference clocks - XCVR_REF_CLK.
- For designs that use any of the PF_XCVR macros, the lanes may lose the LOCK signal after some simulation time as can be seen in the Lane(x)_STATUS_LOCK signal becoming de-asserted sometime after being asserted.

  Workaround:

  For all designs using the PF_XCVR macros, change the default resolution (**Project > Project Settings > Vsim Commands > Resolution**) from the default 1ps to 1fs. Note that switching to a finer simulation time step will incur some simulation runtime penalty.

2.14.5 I/O and I/O Bank Known Issues

- PCI, BUSLVDS25, and MLVDS25 I/O standards cannot be assigned to Output pins or Inout Pins. The Pin column in the I/O Editor is grayed out when these I/O standards are applied to output pins or Inout pins. If the pin assignment with these I/O standards are specified in a PDC constraint file and the PDC constraint file is passed to Place and Route, Place and Route fails.
- The HSTL12I I/O standard cannot be set on a differential I/O. It will fail Place and Route.
- For FCG484/FCVG484: I/O Bank 4 and Bank 5 are merged. If Bank5 is used, configure it to use the same voltage as Bank4.
- The PolarFire differential driver cannot be disabled with OE signal.
- Multiple voltages in an I/O bank are not supported in this release.
- I/Os have no timing (Basic Delay only).

- No power contribution from any IOs in the SmartPower Analysis. Use the power spreadsheet for all bank rails.

2.14.6 Placement DRC Rules

PolarFire devices have strict requirements for connection and placement of I/O Protocol (DDR, XCVR, and so on) solutions. The software enforces compliance with all connectivity and placement DRC rules.

Only a subset of DRC rules are implemented for the MPF200TS_ES die.

2.14.7 Synplify Pro Warns About Unrecognized Part and Device Family

When Synplify Pro is invoked interactively in the Libero SoC PolarFire software, a warning message appears: “Unrecognized Speed Grade -1 specified for Package FBGA896….” This warning message can be ignored.

2.14.8 Libero-Generated Derived Constraints with Brackets fails Place and Route

Place and Route fails to run with a Derived Constraint SDC file if the instance name in the Derived Constraint file contains brackets.

Example:

```
create_clock -name \
{GF_LPM1[1].LPM/U_LPM2_TRANS/GI_TRANS_XI_0.U_LPM3_TRANS_GTH2/U_GTHE3/PF_XCVR_0/L
ANE0/TX_CLK_G}
-period 64 [ get_pins {
GF_LPM1[1].LPM/U_LPM2_TRANS/GI_TRANS_XI_0.U_LPM3_TRANS_GTH2/U_GTHE3/PF_XCVR_0/LA
NE0/TX_CLK_G
} ]
```

Workaround:

Modify the <design>_derived_constraints.sdc file (**Constraint Manager > Timing tab**) to replace the brackets with dots in the instance name and rerun place and route:

```
create_clock -name
{GF_LPM1.1.LPM/U_LPM2_TRANS/GI_TRANS_XI_0.U_LPM3_TRANS_GTH2/U_GTHE3/PF_XCVR_0/LA
NE0/TX_CLK_G}
-period 64 [ get_pins {
GF_LPM1.1.LPM/U_LPM2_TRANS/GI_TRANS_XI_0.U_LPM3_TRANS_GTH2/U_GTHE3/PF_XCVR_0/LAN
E0/TX_CLK_G
} ]
```

2.14.9 MPF200TS_ES Die - I/O Editor and DRC Placement

- For MPF200TS_ES die, the PolarFire I/O Editor Transceiver view does not reflect the true physical connection of the XCVR, XCVR_REF_CLK, and TX_PLL.
- No DRC Placement checks are implemented on MPF200TS_ES die. A Design with Transceiver may fail Place and Route even though the PolarFire I/O Editor gives no error when committing the connections between the XCVR_REF_CLK and TX_PLL, XCVR_REF_CLK and XCVR lanes.

2.14.10 BSDL File Not Up To Date

Libero SoC PolarFire generates a BSDL file for PolarFire but it is not up to date. The safe value for BSDL is not correct. Use the BSDL file for PolarFire devices on the Microsemi website https://www.microsemi.com/products/fpga-soc/design-resources/bsdl-models

2.14.11 SmartDesign Generates Components out of Old Incompatible SG Core Versions

Some PolarFire SmartGen (SG) cores do not have a MAXIMUM version number specifying the highest Libero SoC version that the cores are compatible with. As a result, some SG core versions incompatible with the Libero SoC version may be generated in SmartDesign. These components, if generated, fail later in the design process, either during Synthesis or Place-and-Route.

Workaround:

Update the SG core version to the version supported in this release, and regenerate the SmartDesign component.

2.14.12 No EDIF Source File Import

Do not import an EDIF design source file into the Libero SoC PolarFire project. Import only HDL design source files, or mapped Verilog netlist (*.vm files) from Synthesis as design source files.

2.14.13 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

2.14.14 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** and the software is installed successfully.

2.14.15 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

2.15 Download Libero SoC PolarFire Software

The following are available for download:

Libero SoC PolarFire software Linux or Windows

Note: Installation requires administrative privileges.

PolarFire FPGA Power Estimator

Release Notes