

RTG4\_DEV\_KIT

DVP-102-000418-001 Rev B

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Project Name:

RTG4\_DEV\_KIT

Rev

Part Number:

B1

MICROSEMI DVP-102-000418-001

PACTRON: 305-PD-15-0161

Originator:

GHURU KUMARAVELU

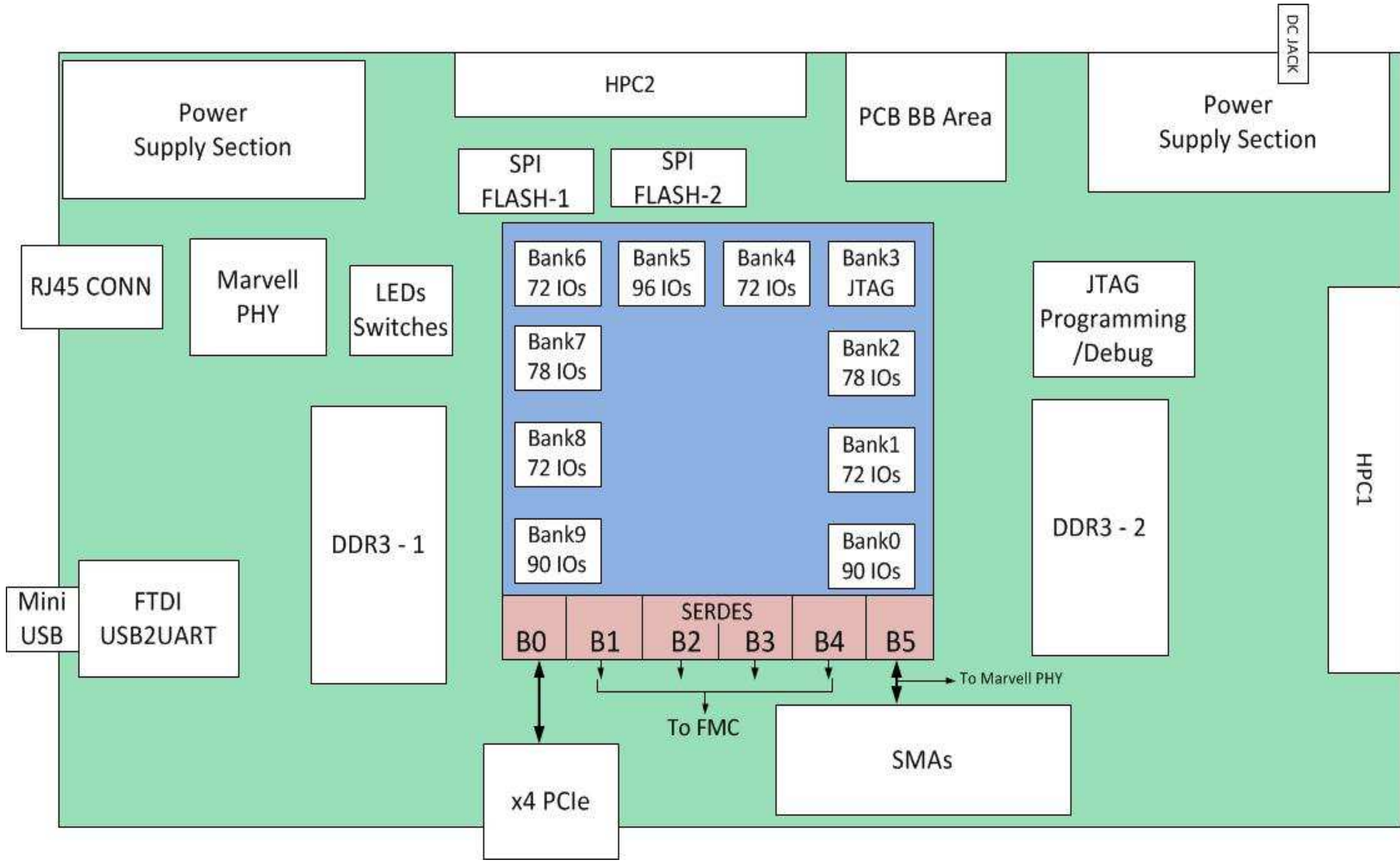
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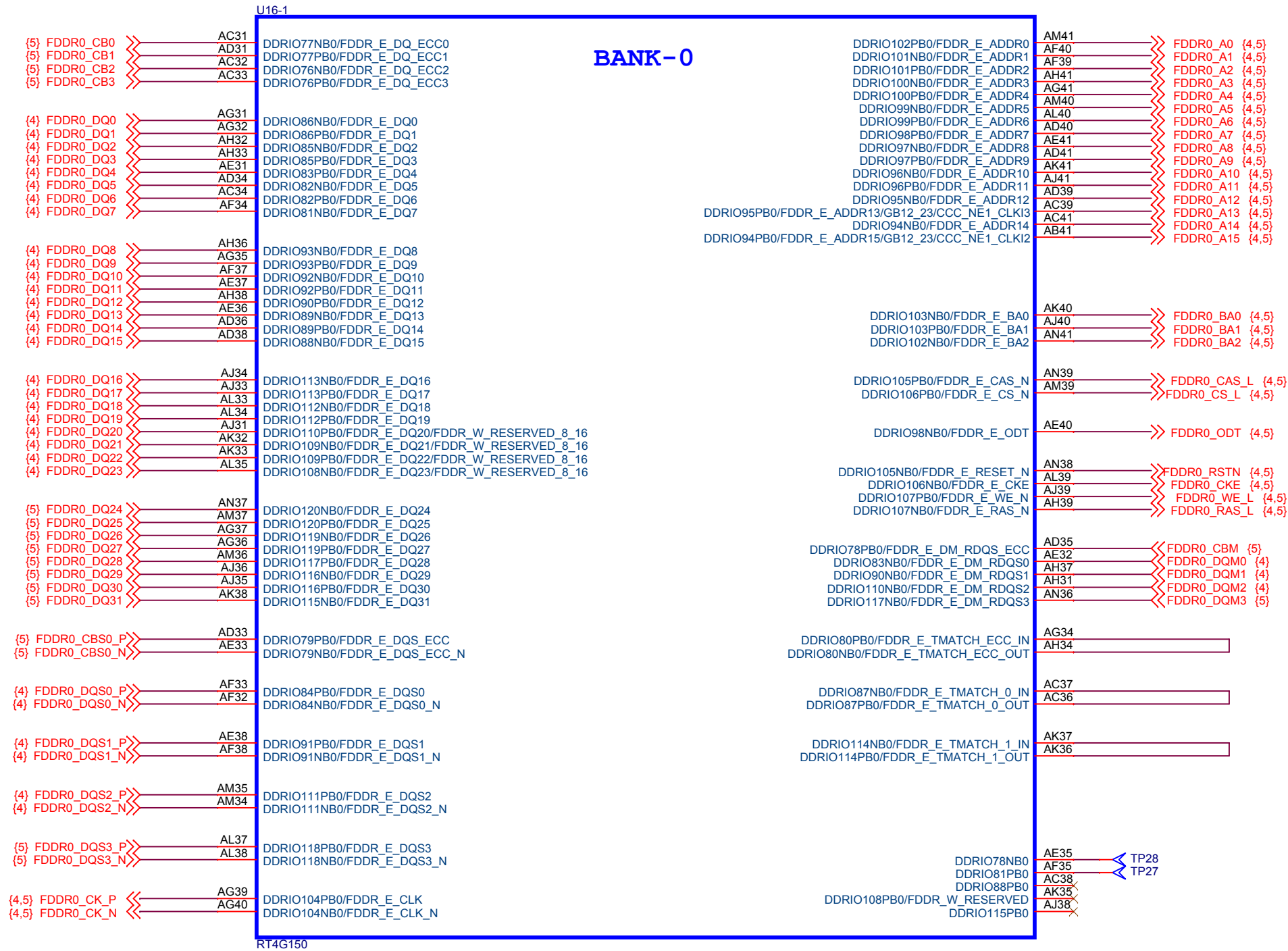
Custom Tuesday, March 22, 2016

Sheet 1 of 45

BLOCK DIAGRAM

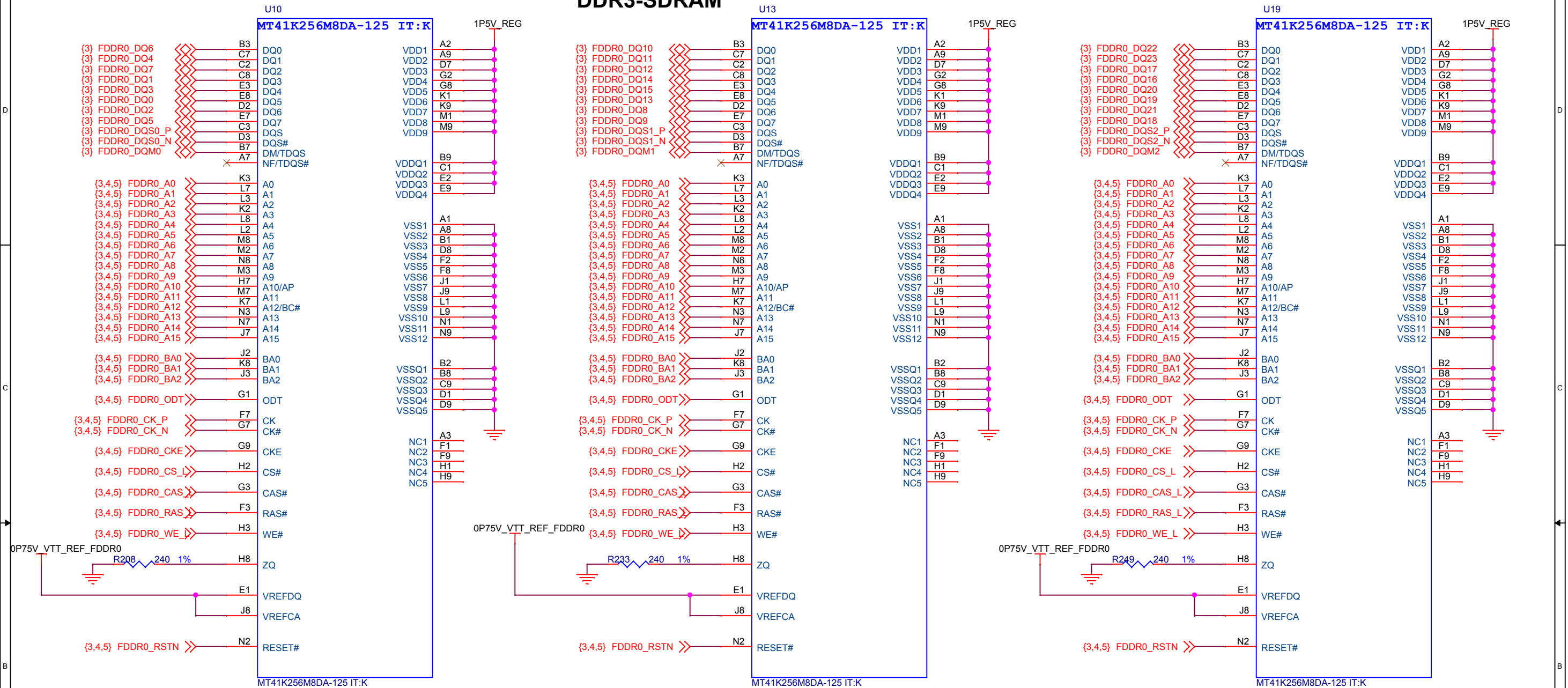


# MEMORY INTERFACE



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DATE: Tuesday, March 22, 2016		SH 3	OF 45

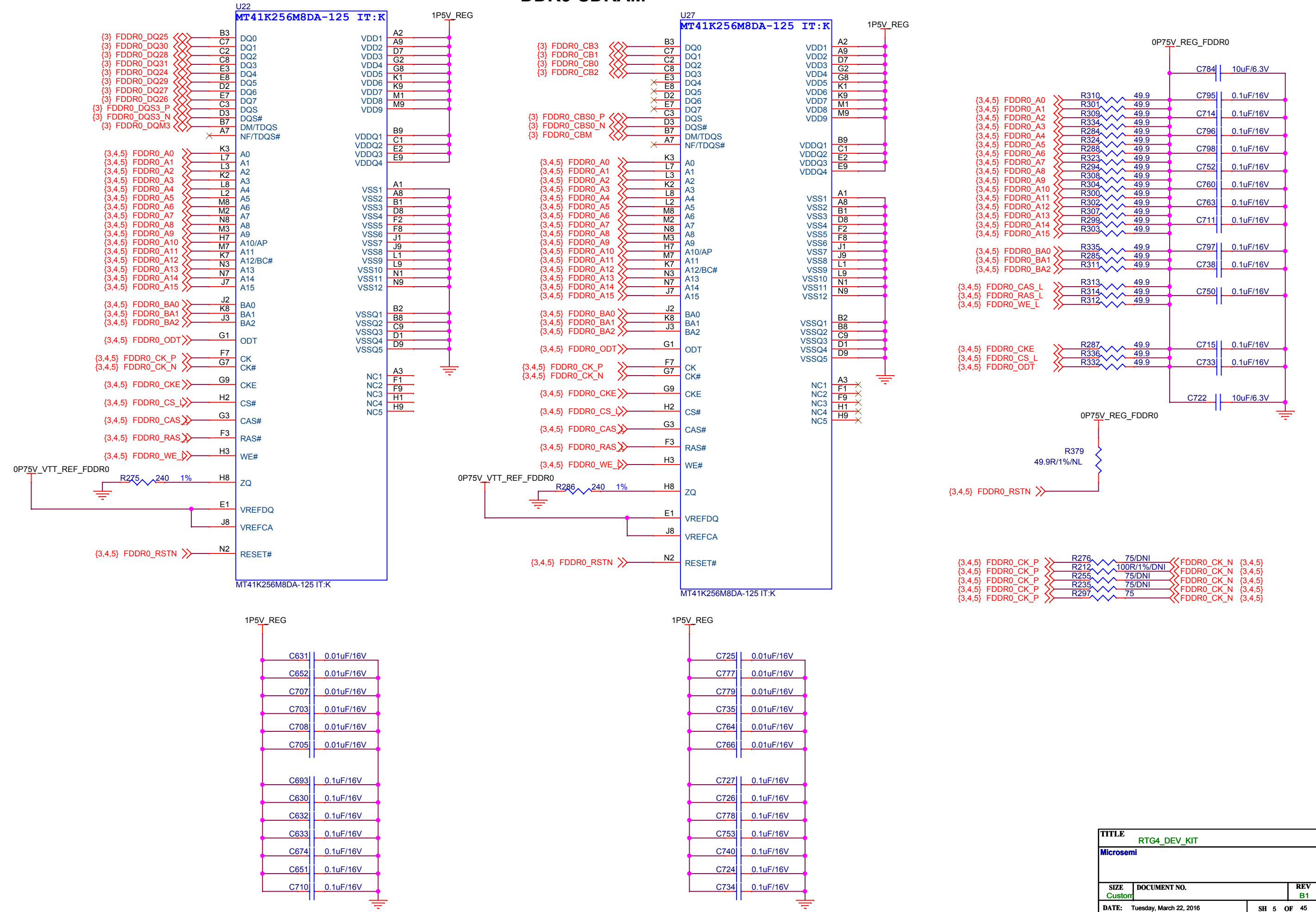
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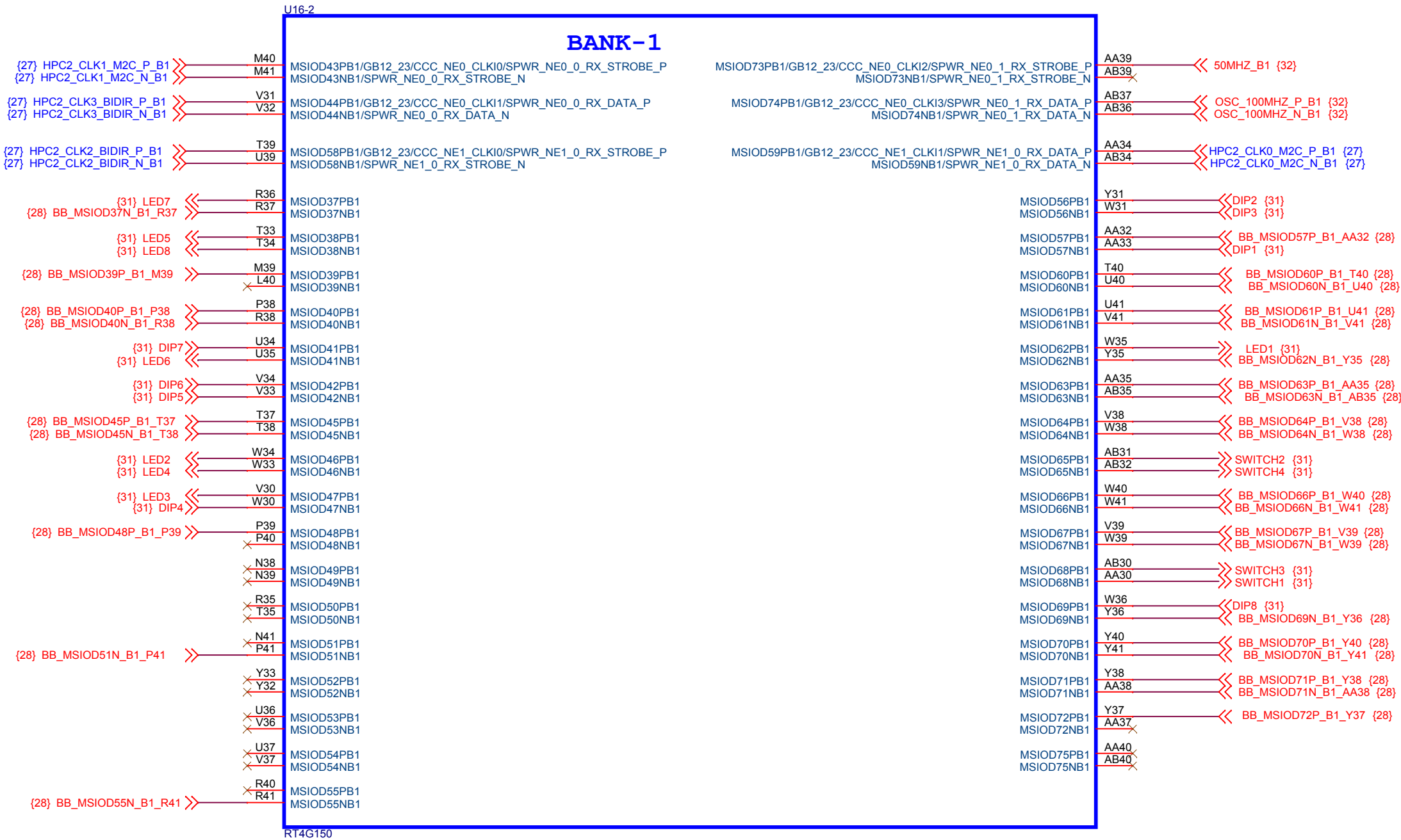
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DDR3-SDRAM

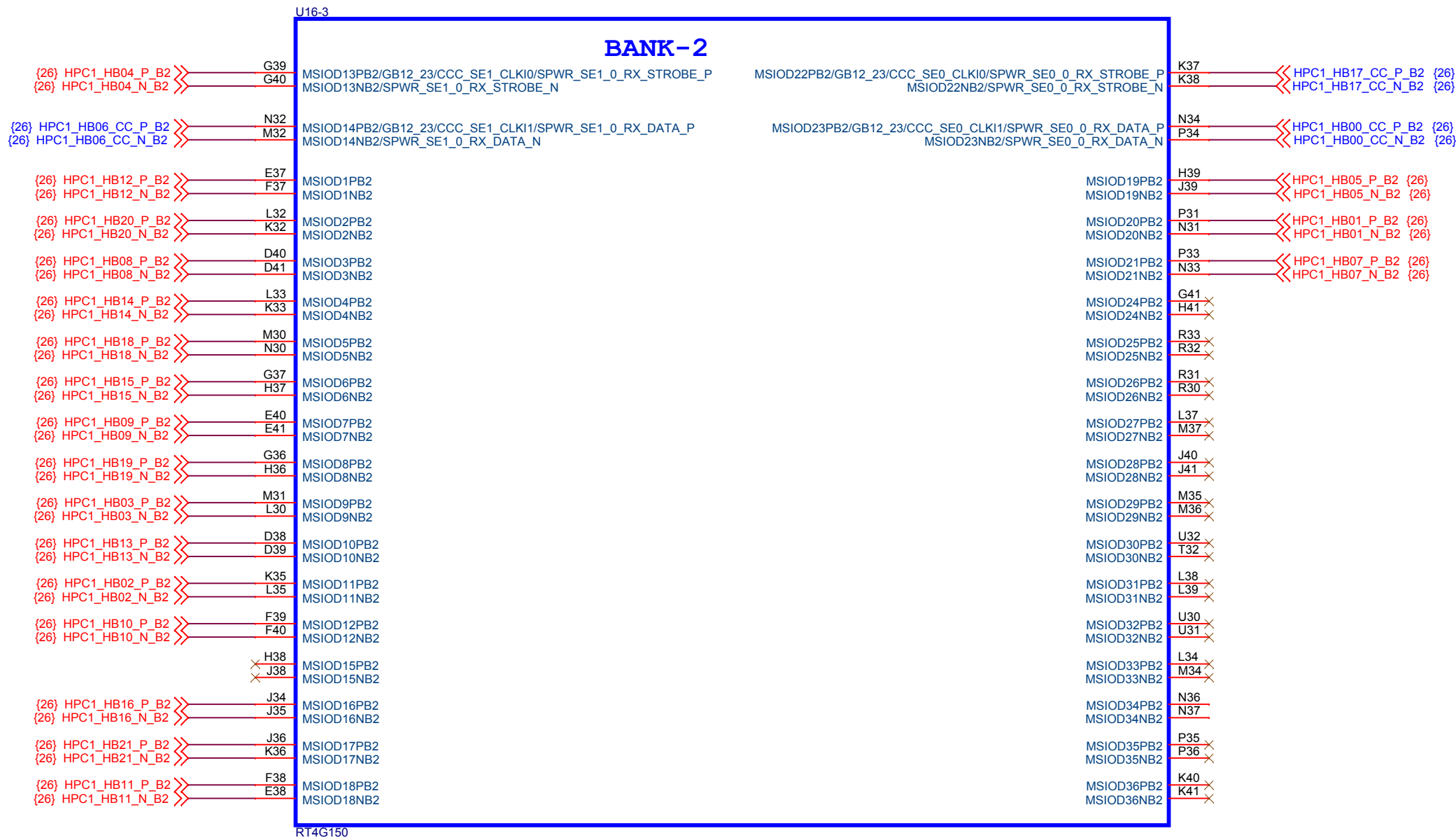


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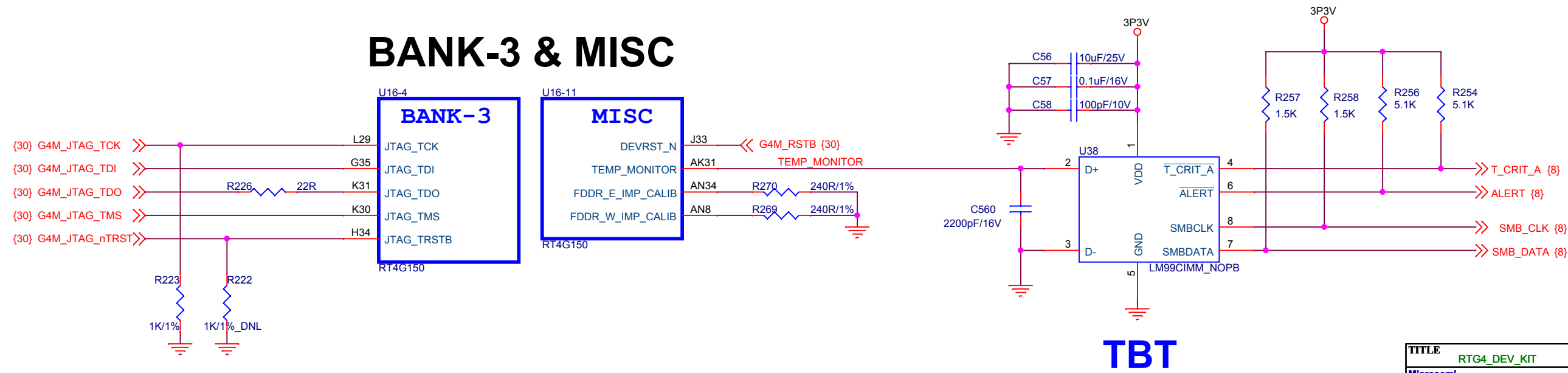


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BANK-2

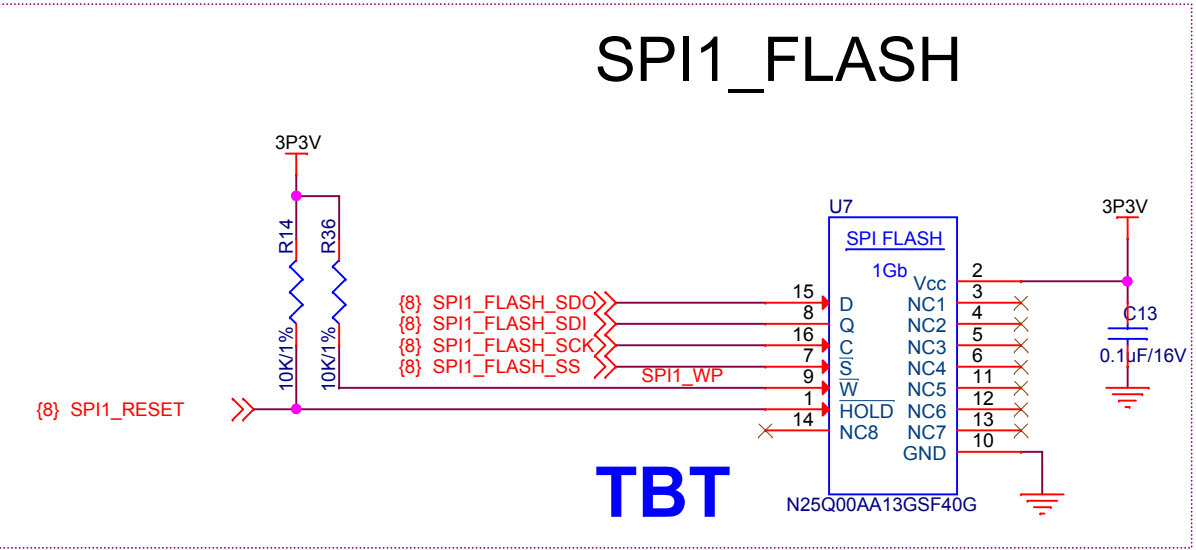
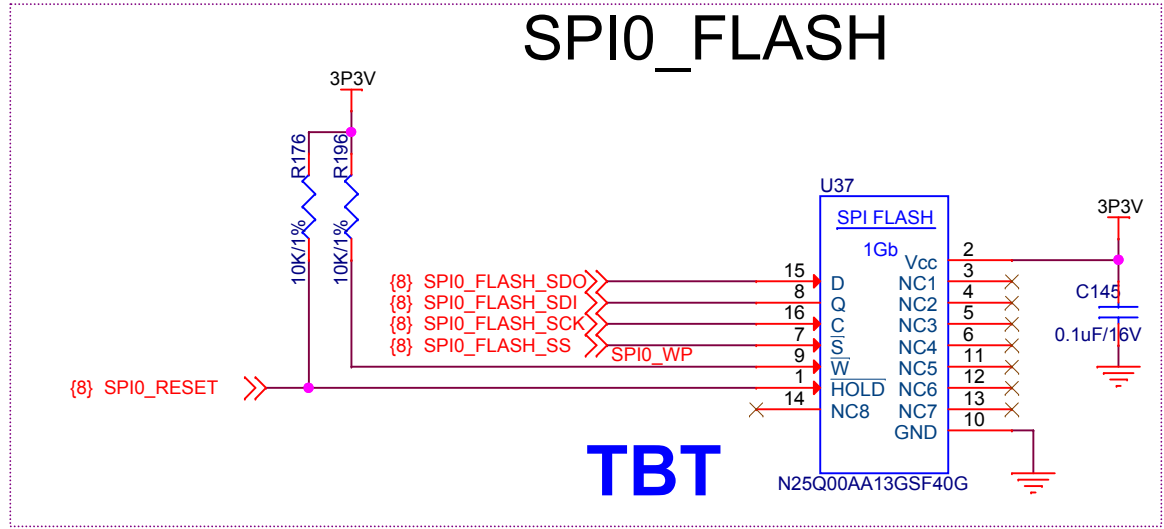
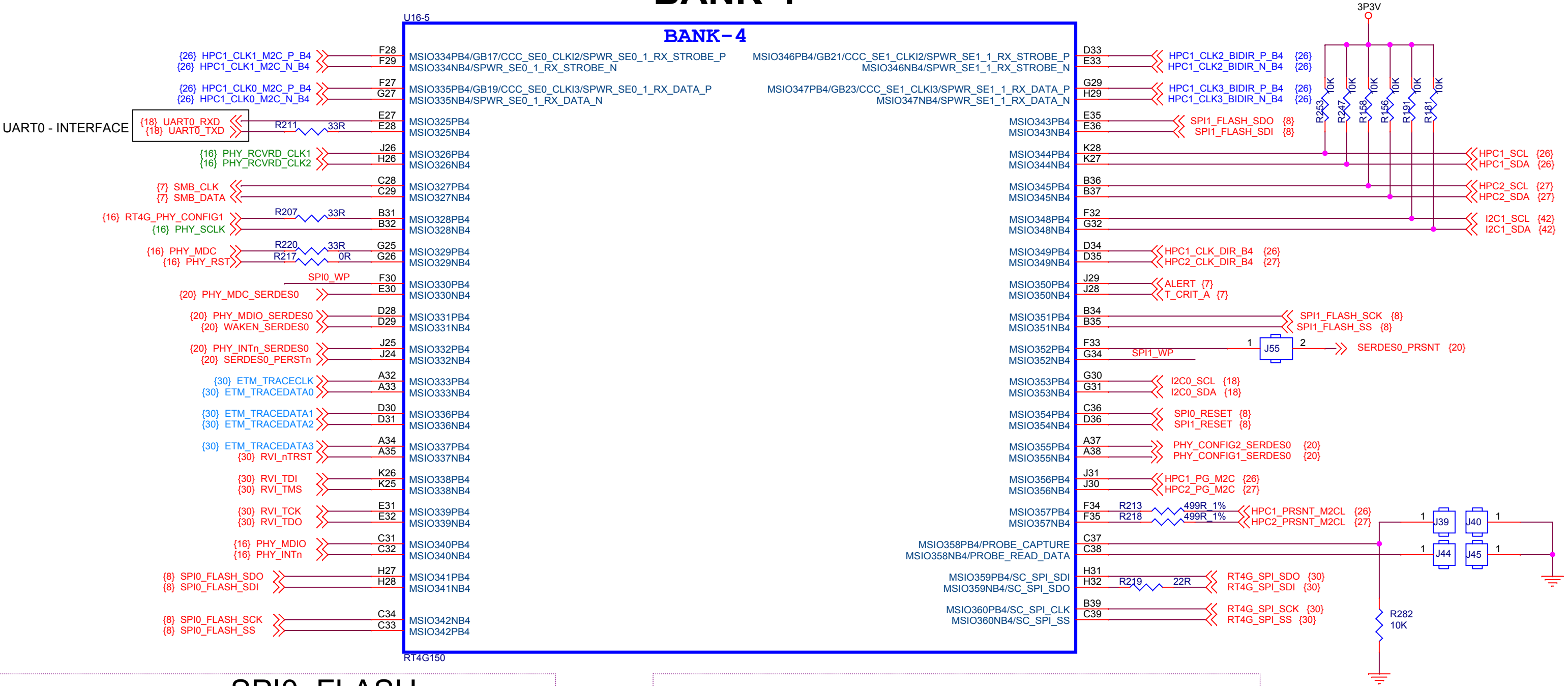


BANK-3 & MISC



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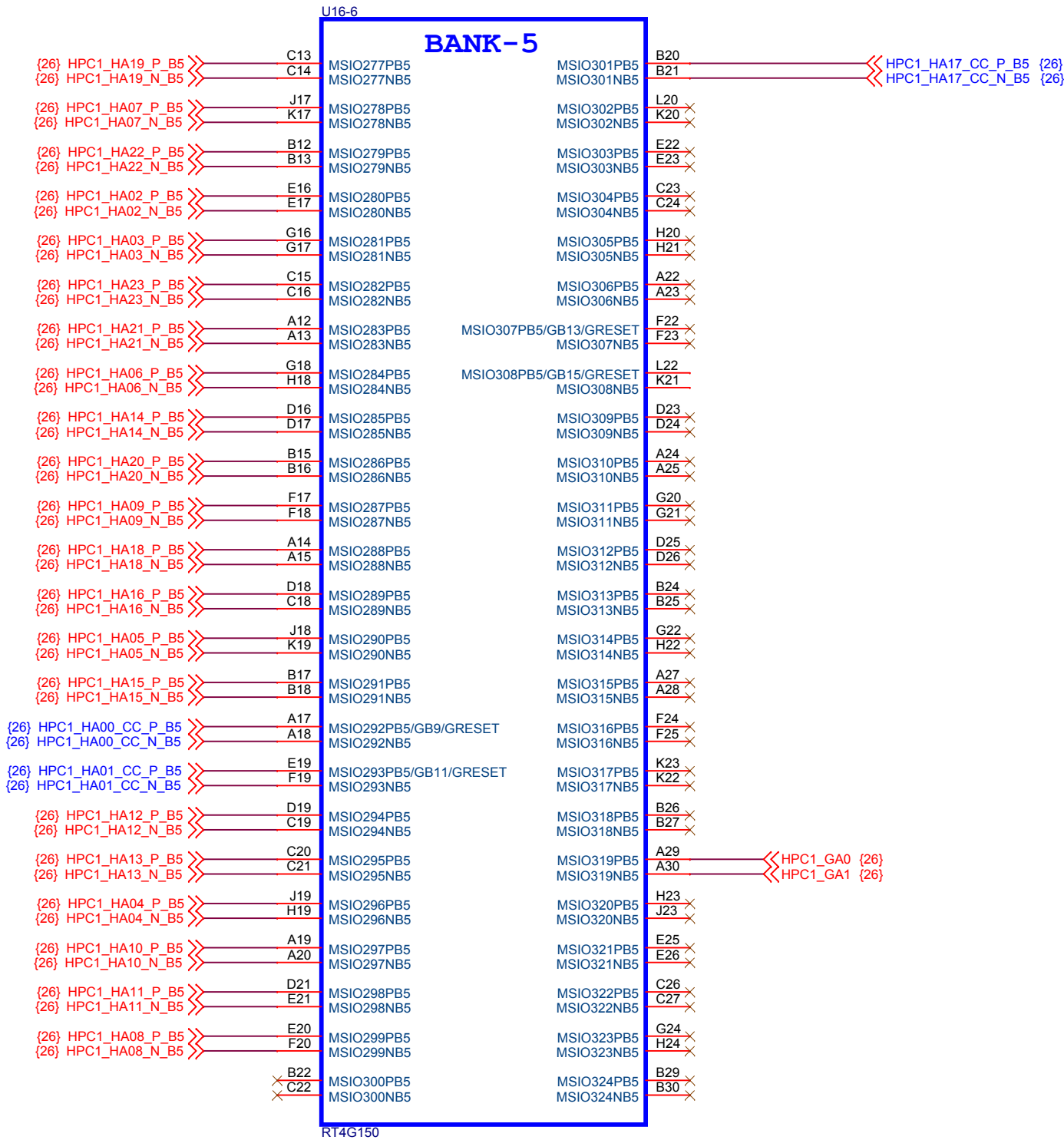
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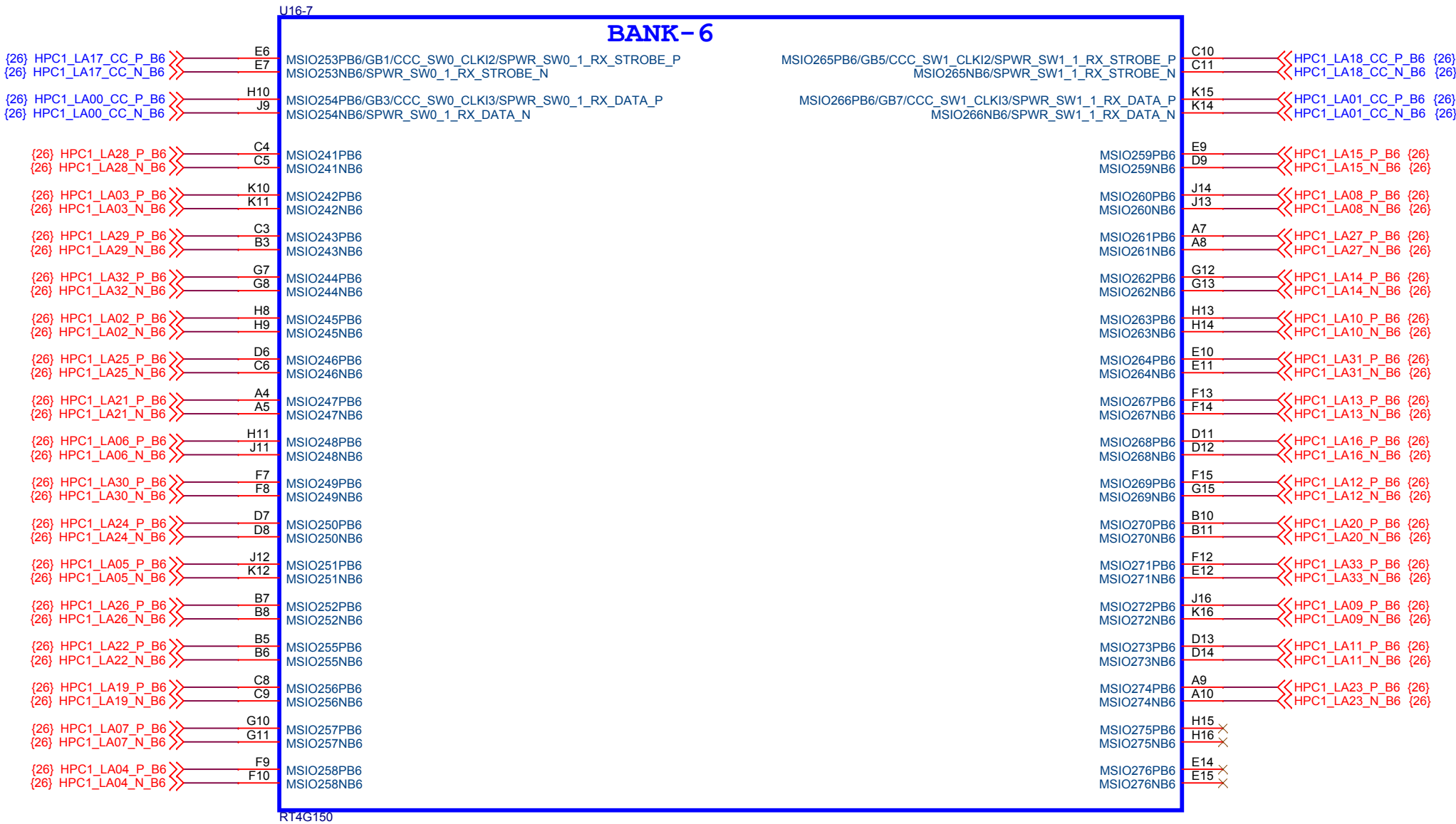


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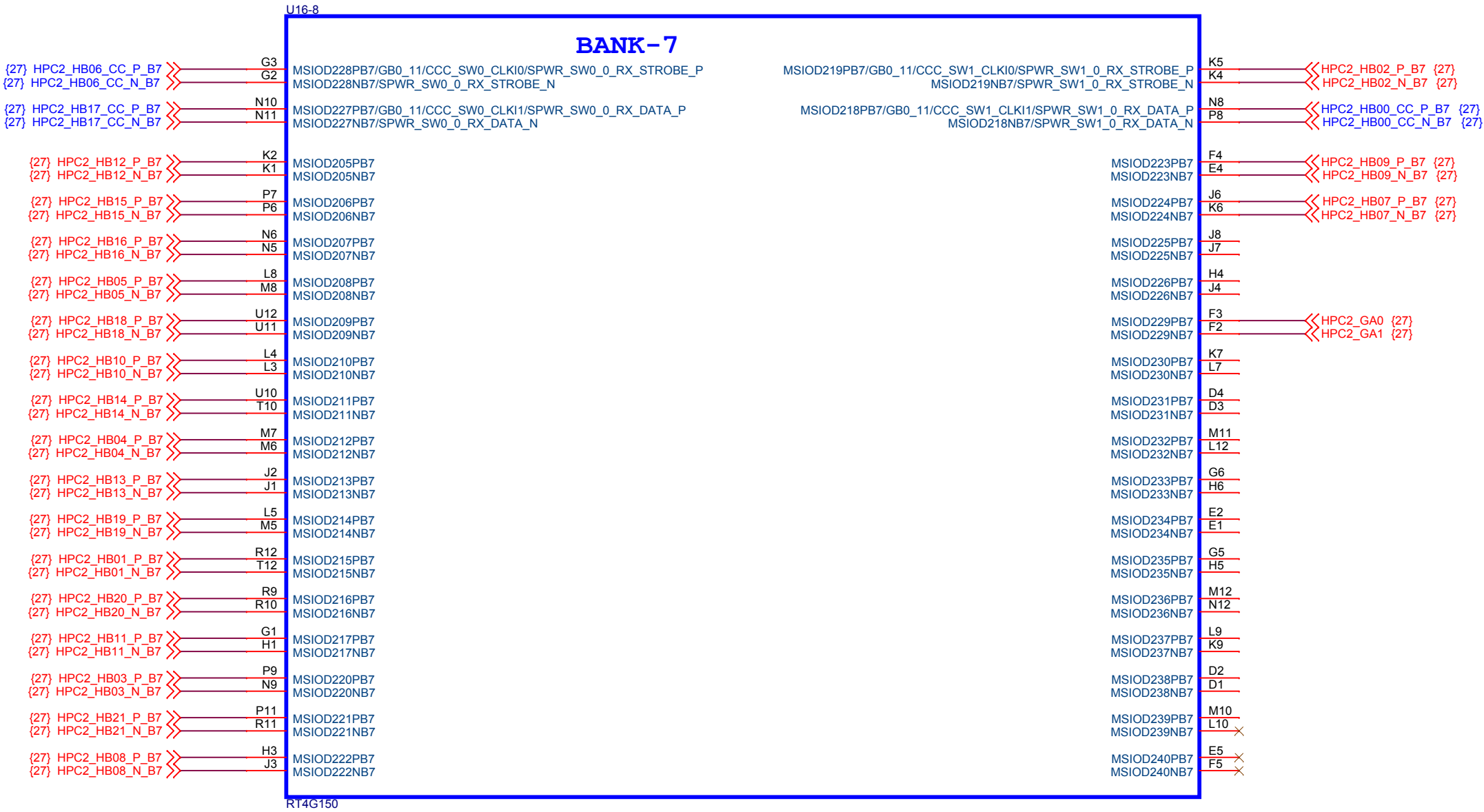
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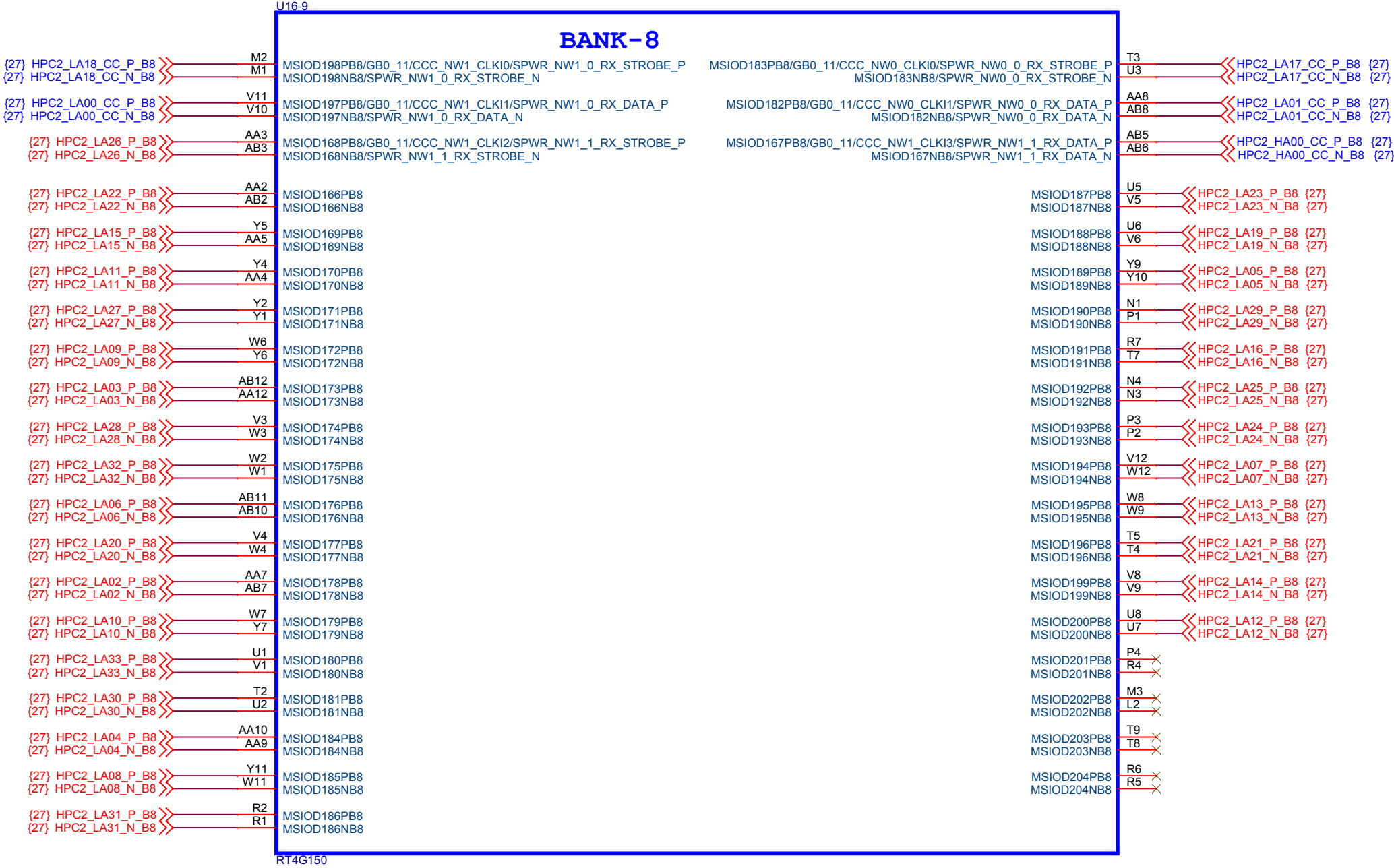
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BANK-7



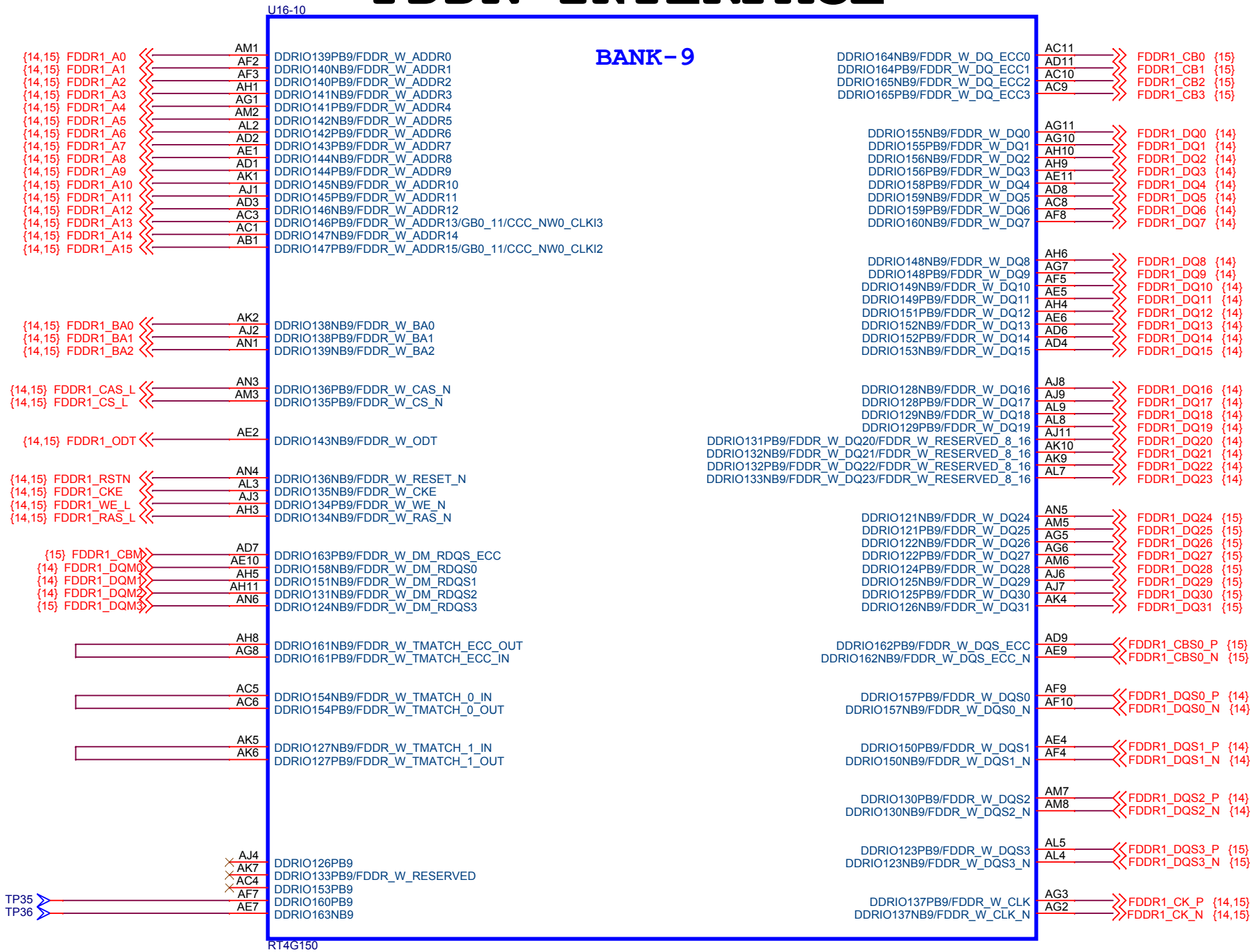
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BANK-8



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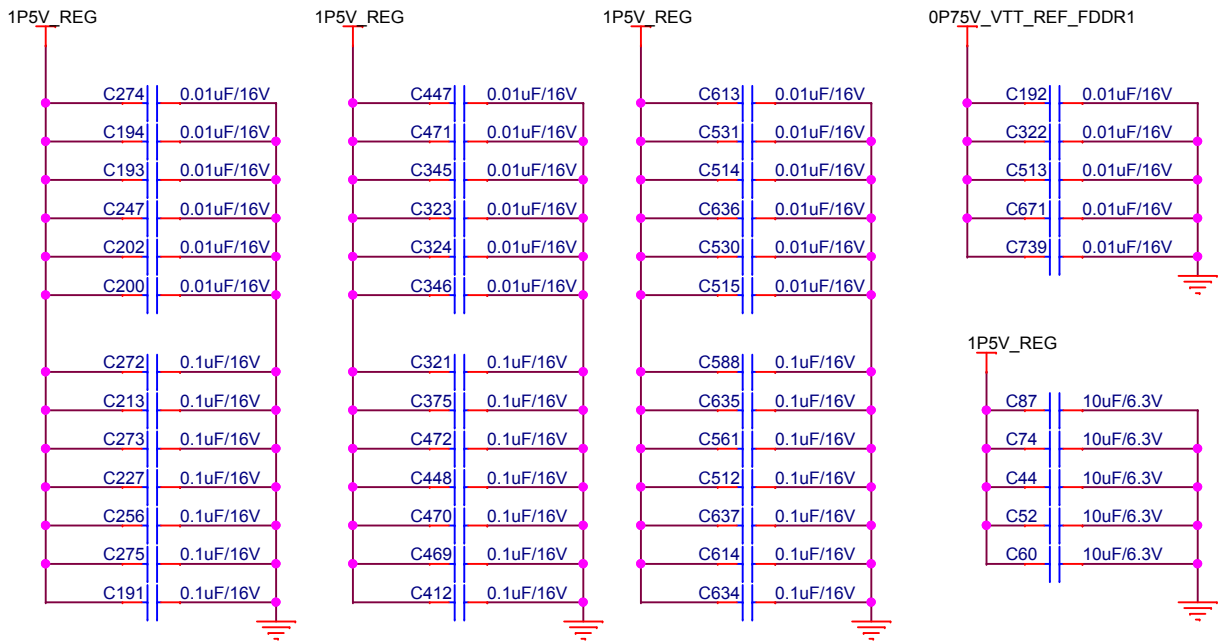
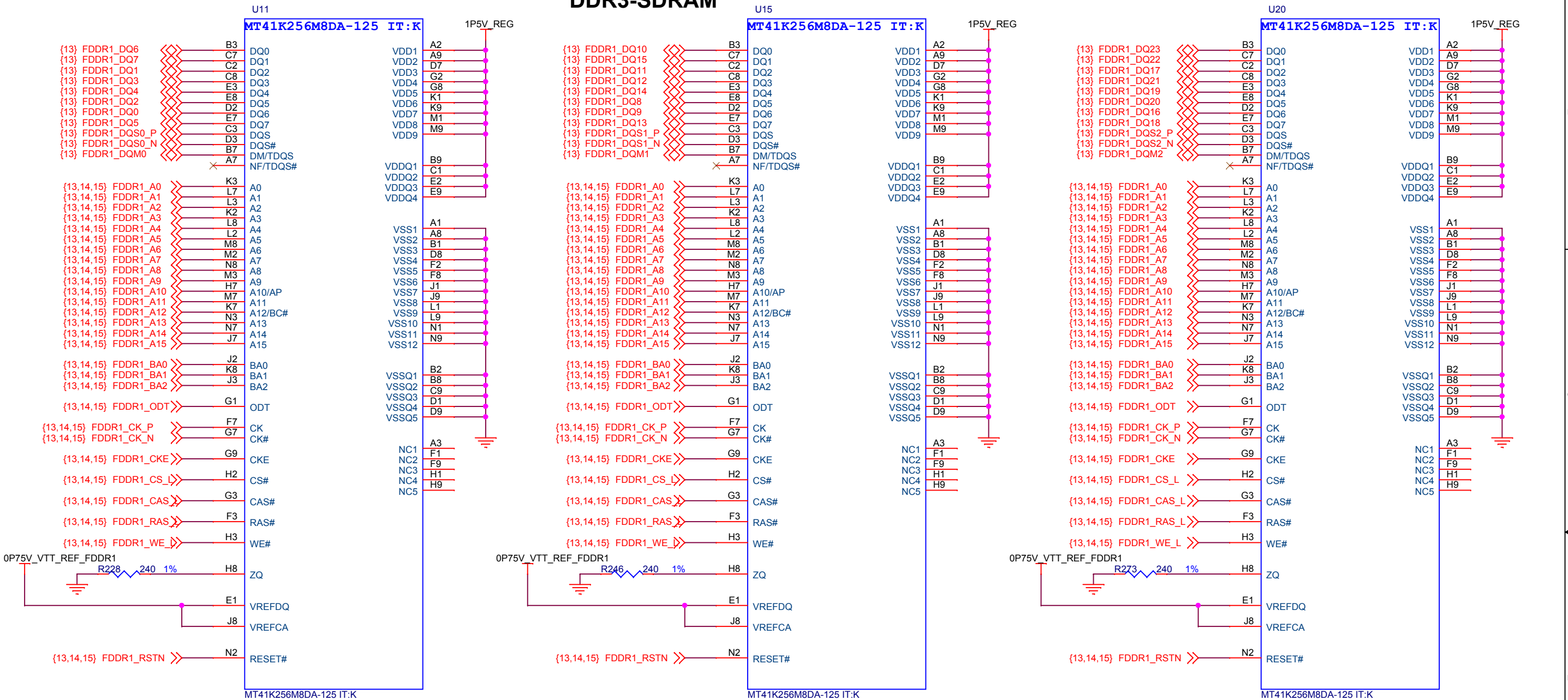
FDDR INTERFACE



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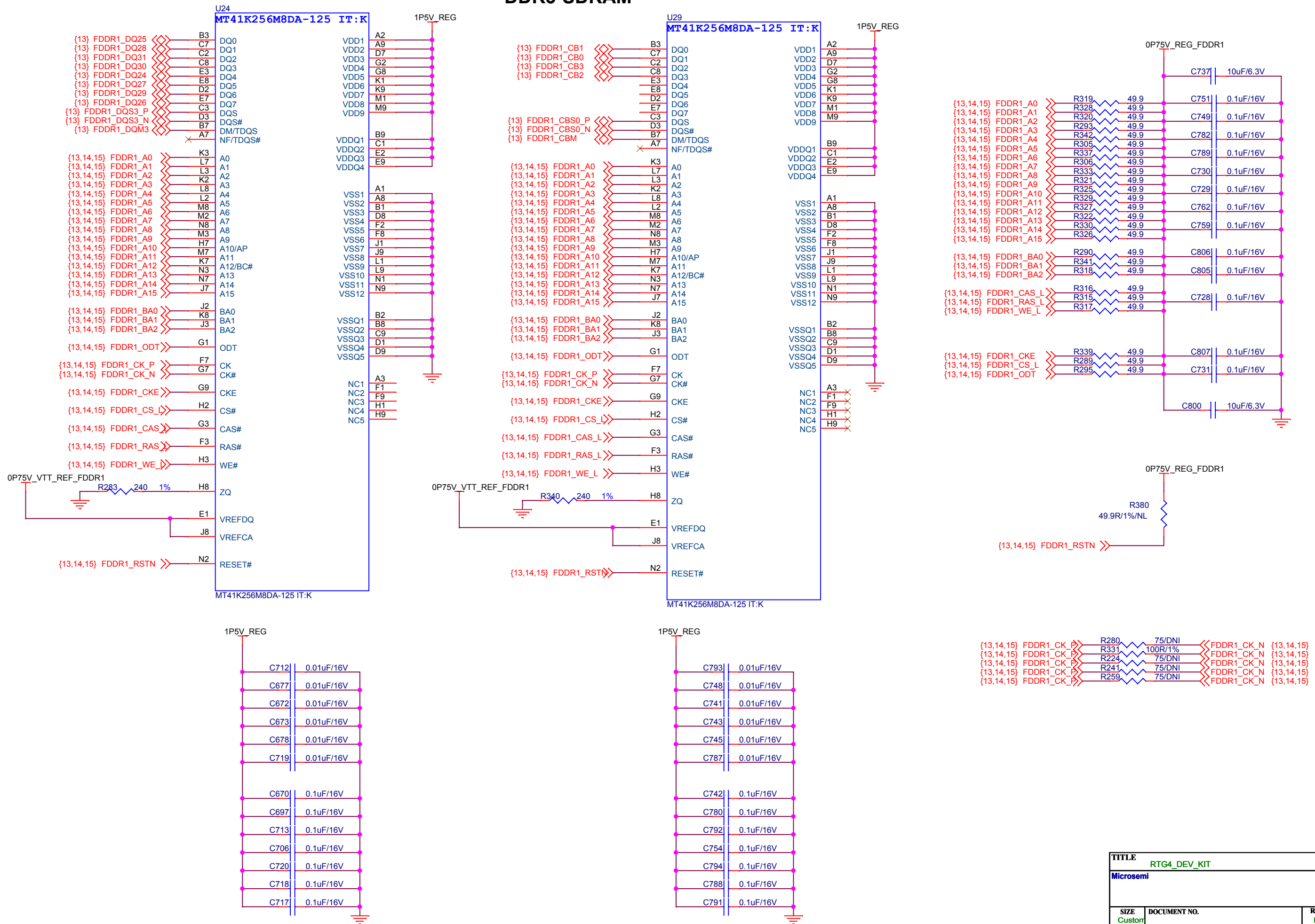


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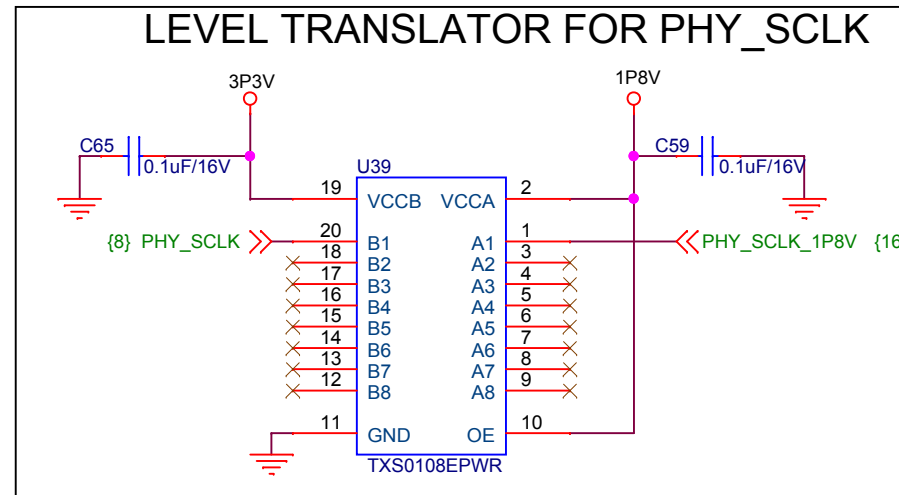
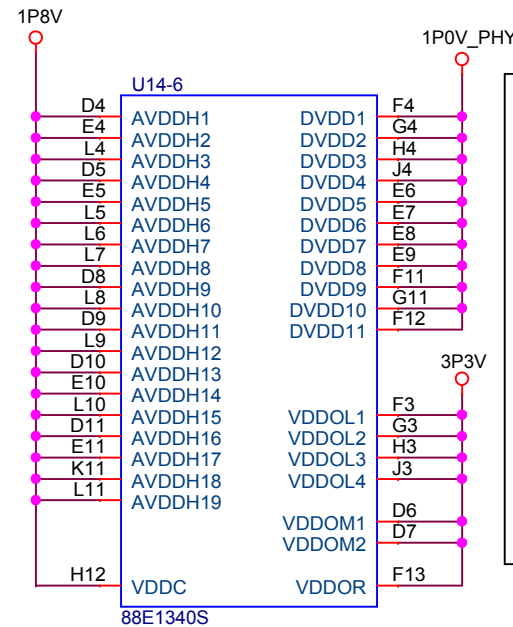
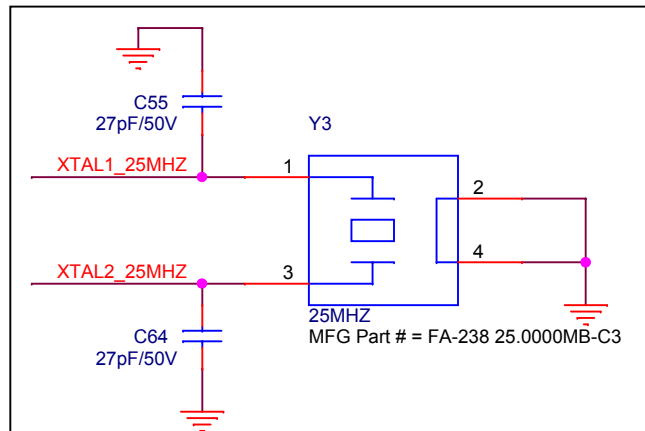
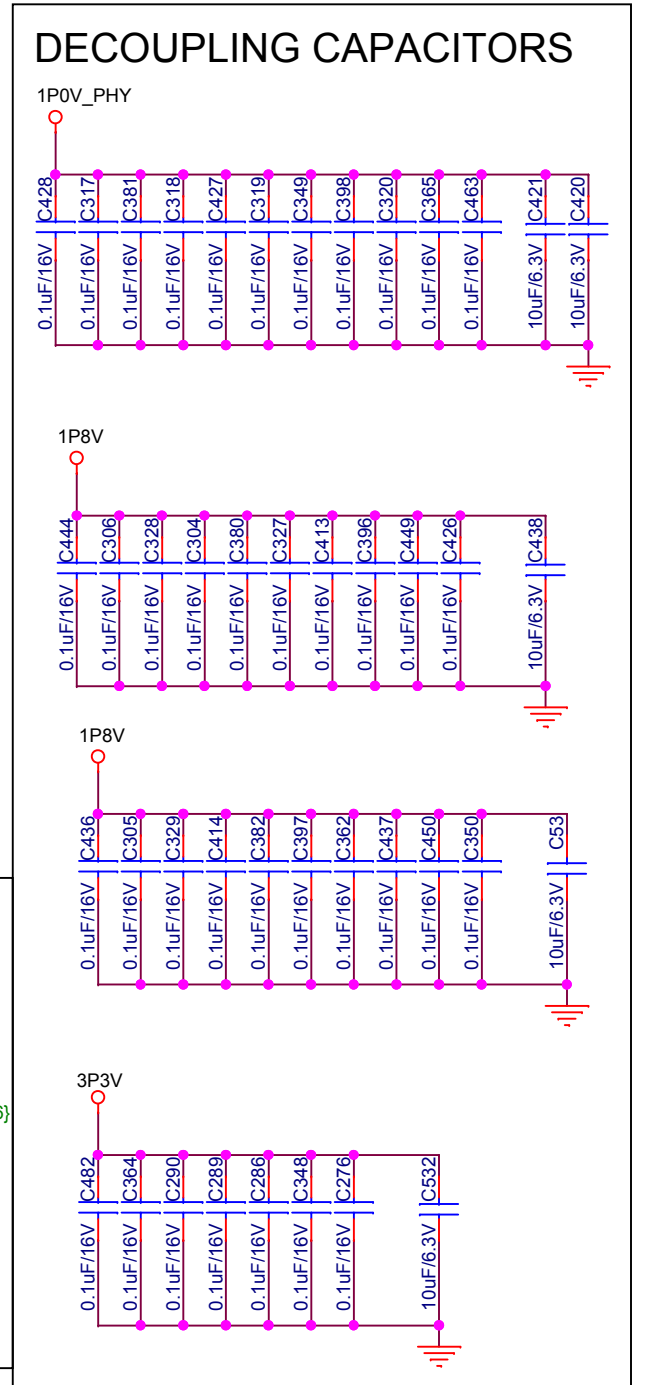
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## DDR3-SDRAM



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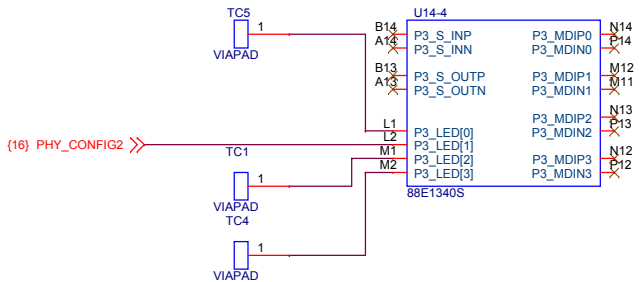
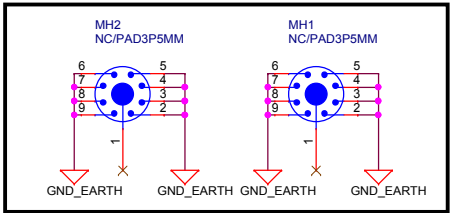
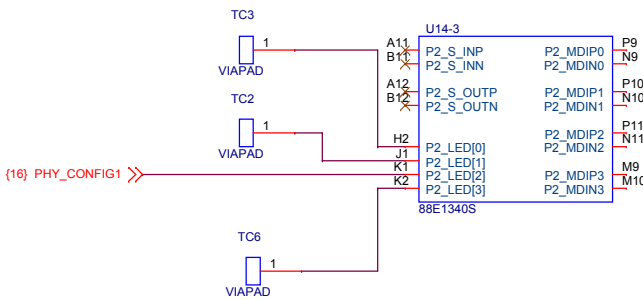
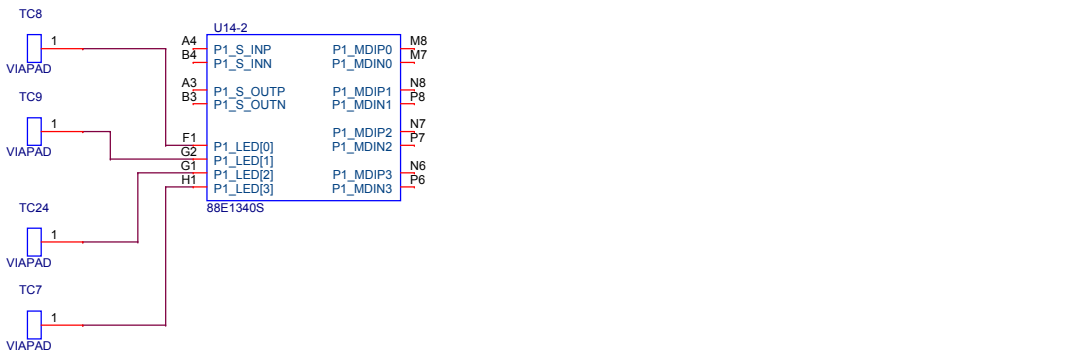
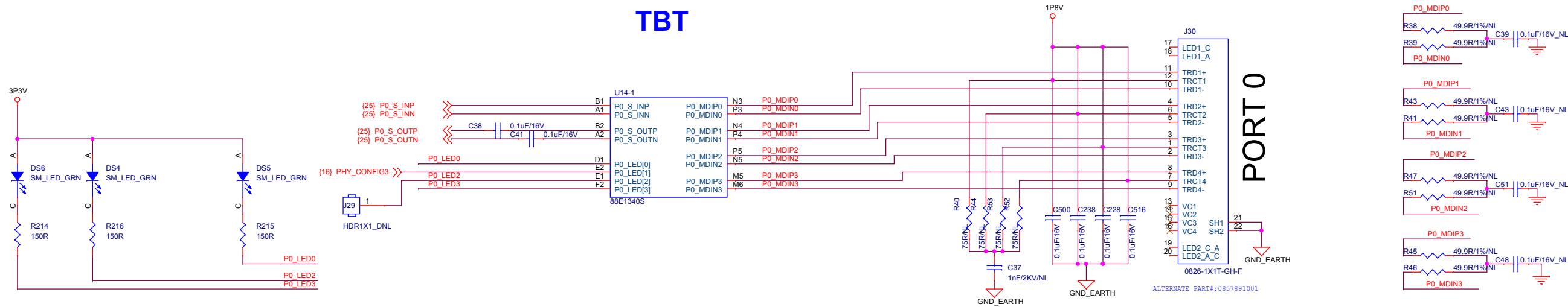
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<b>DATE:</b> Tuesday, March 20, 2016		<b>SH</b> 16	<b>OF</b> 45

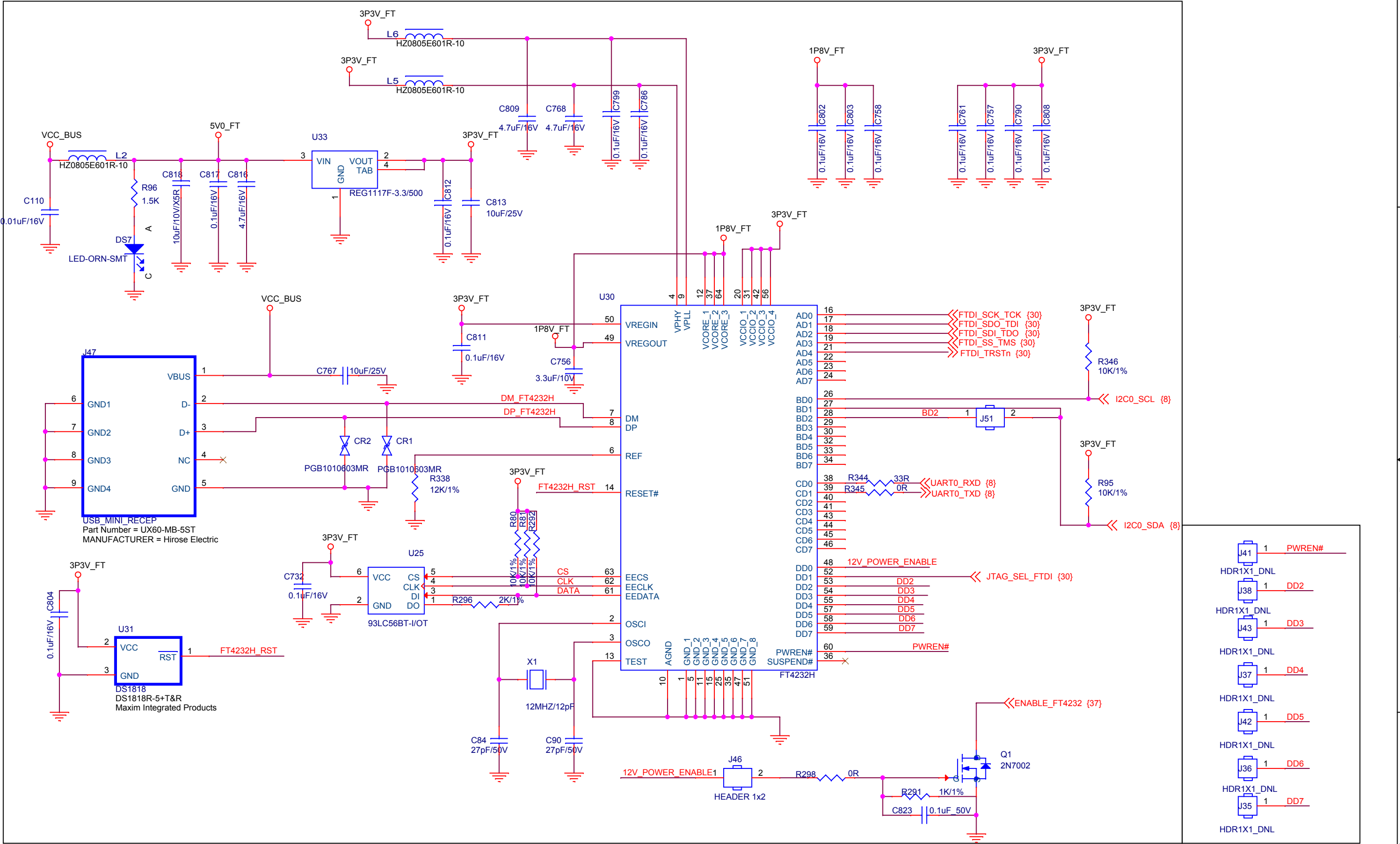
MARVELL PHY - RJ45 INTERFACE

TBT



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FT4232H CIRCUITRY

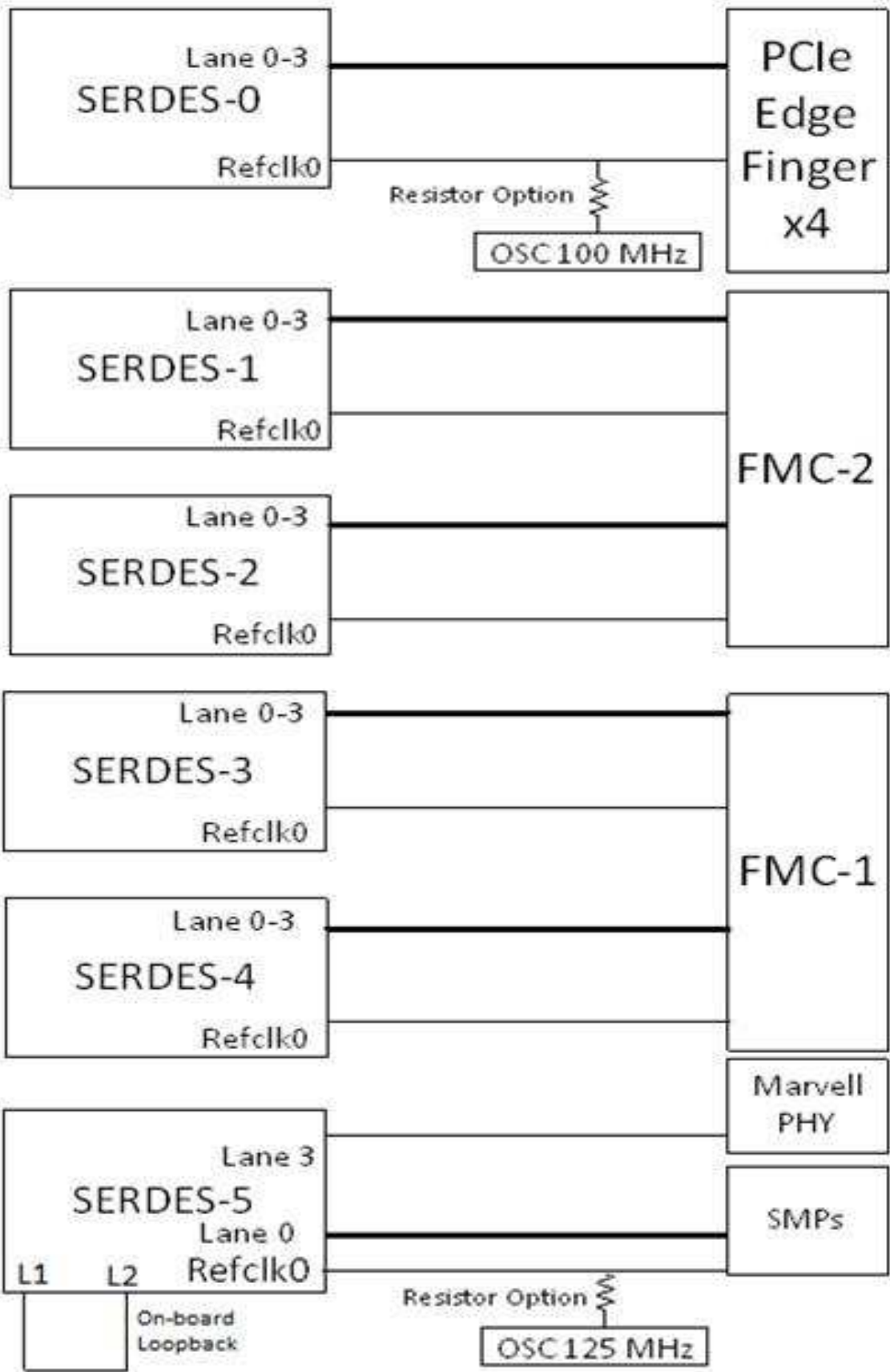


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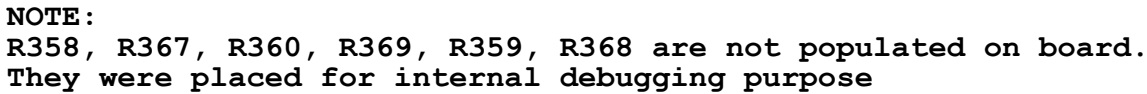
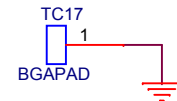
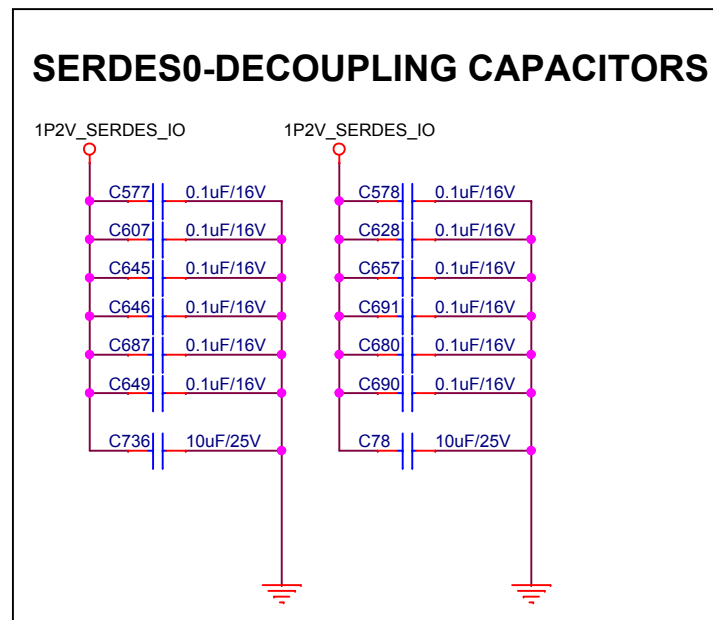
# SERDES BLOCK DIAGRAM

SERDES Block allocation for RTG4 DEV KIT



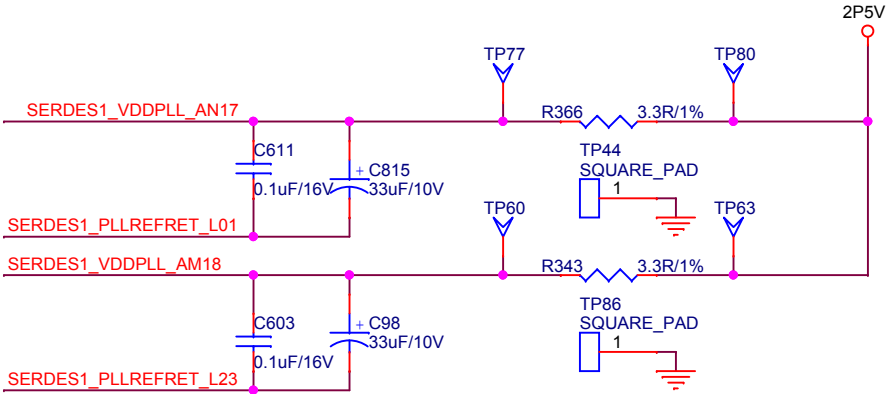
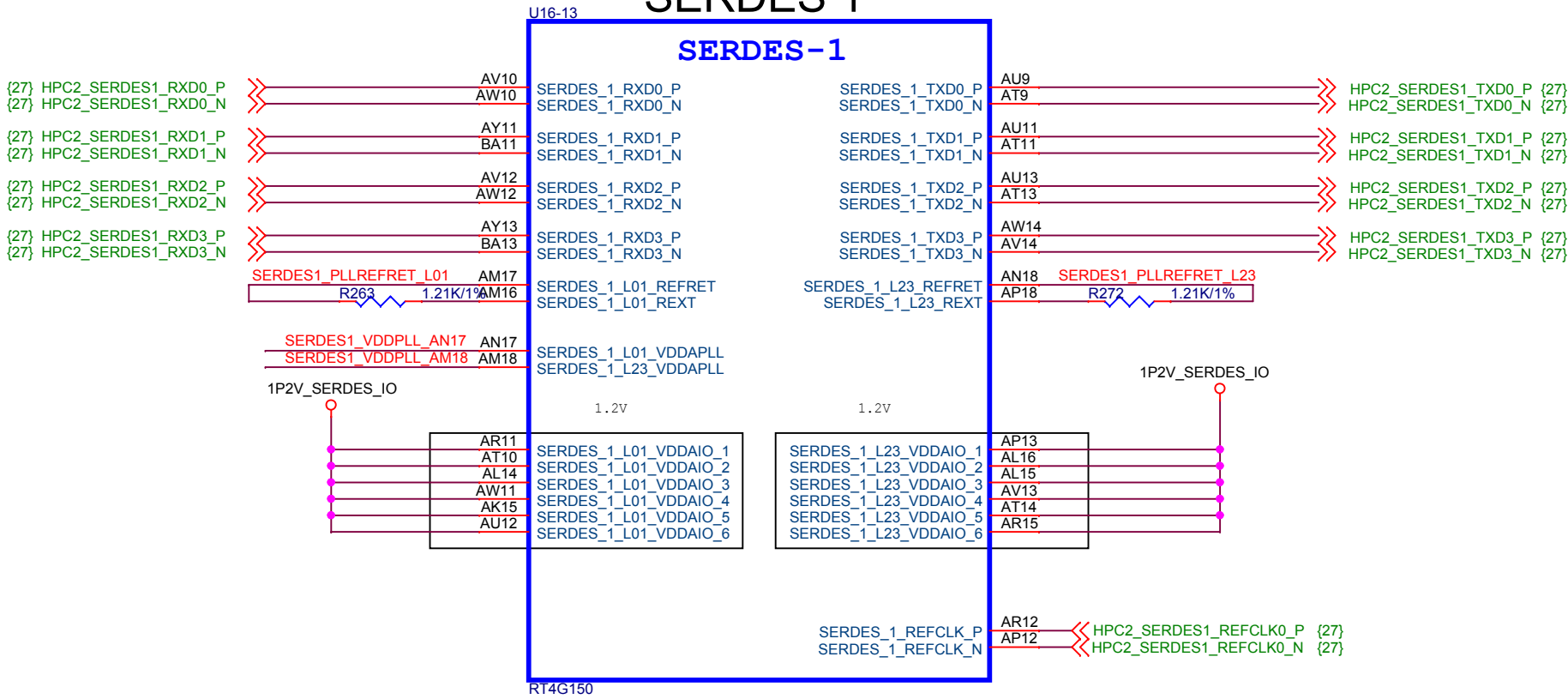
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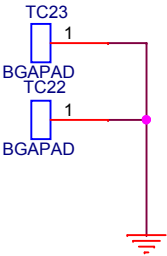
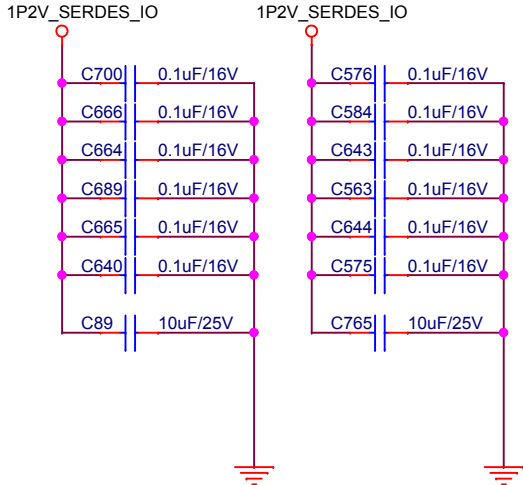
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<b>DATE:</b>	Tuesday, March 20, 2016	SH 20	OF 45

SERDES 1

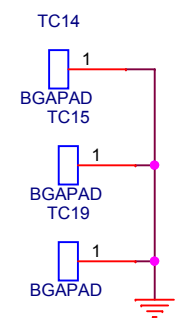
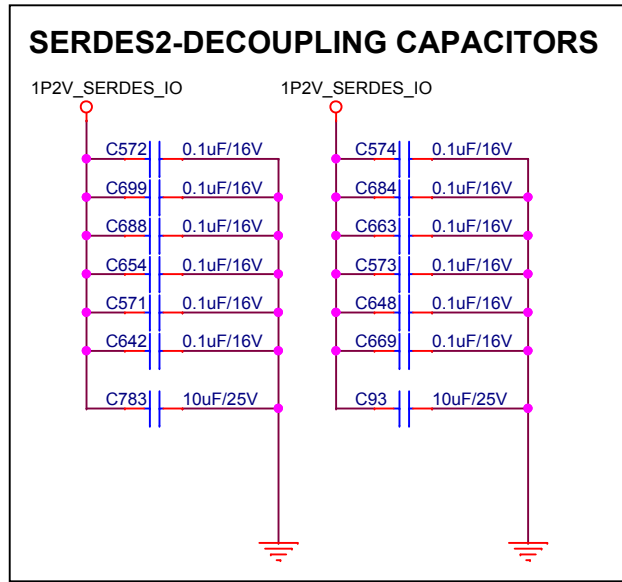
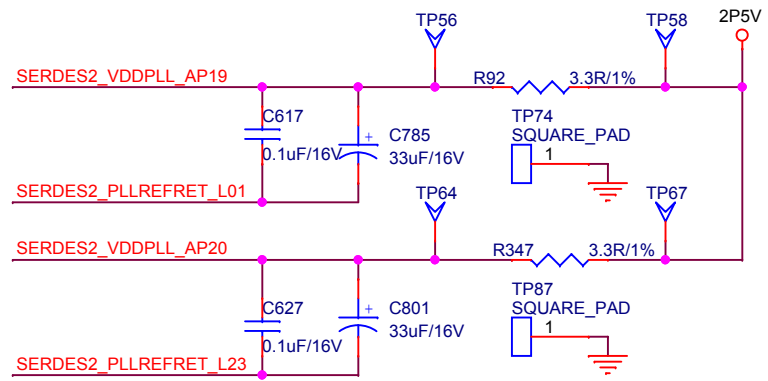
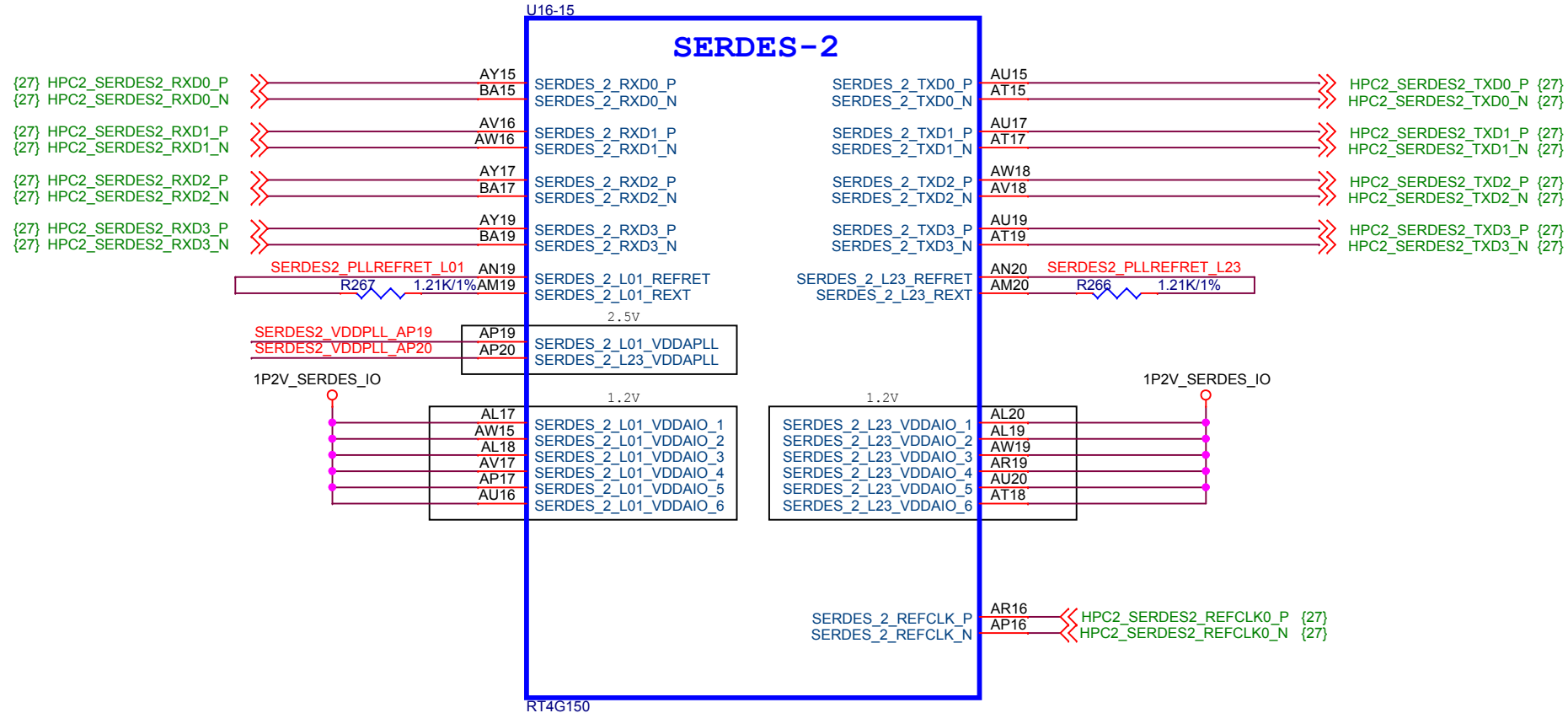


SERDES1-DECOUPLING CAPACITORS



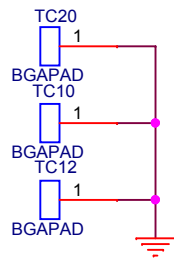
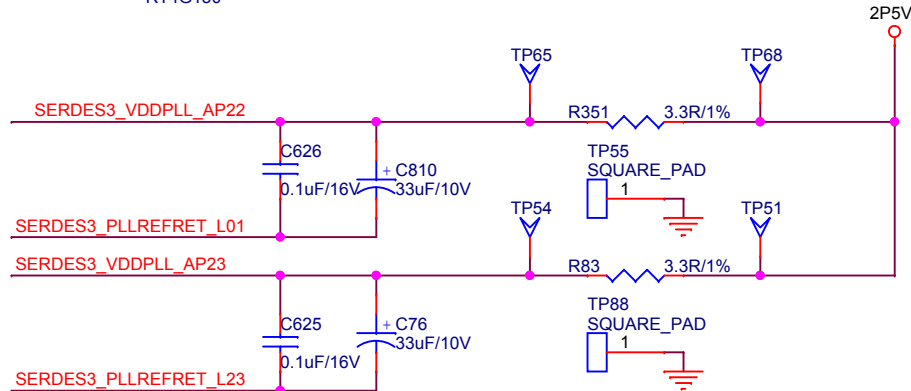
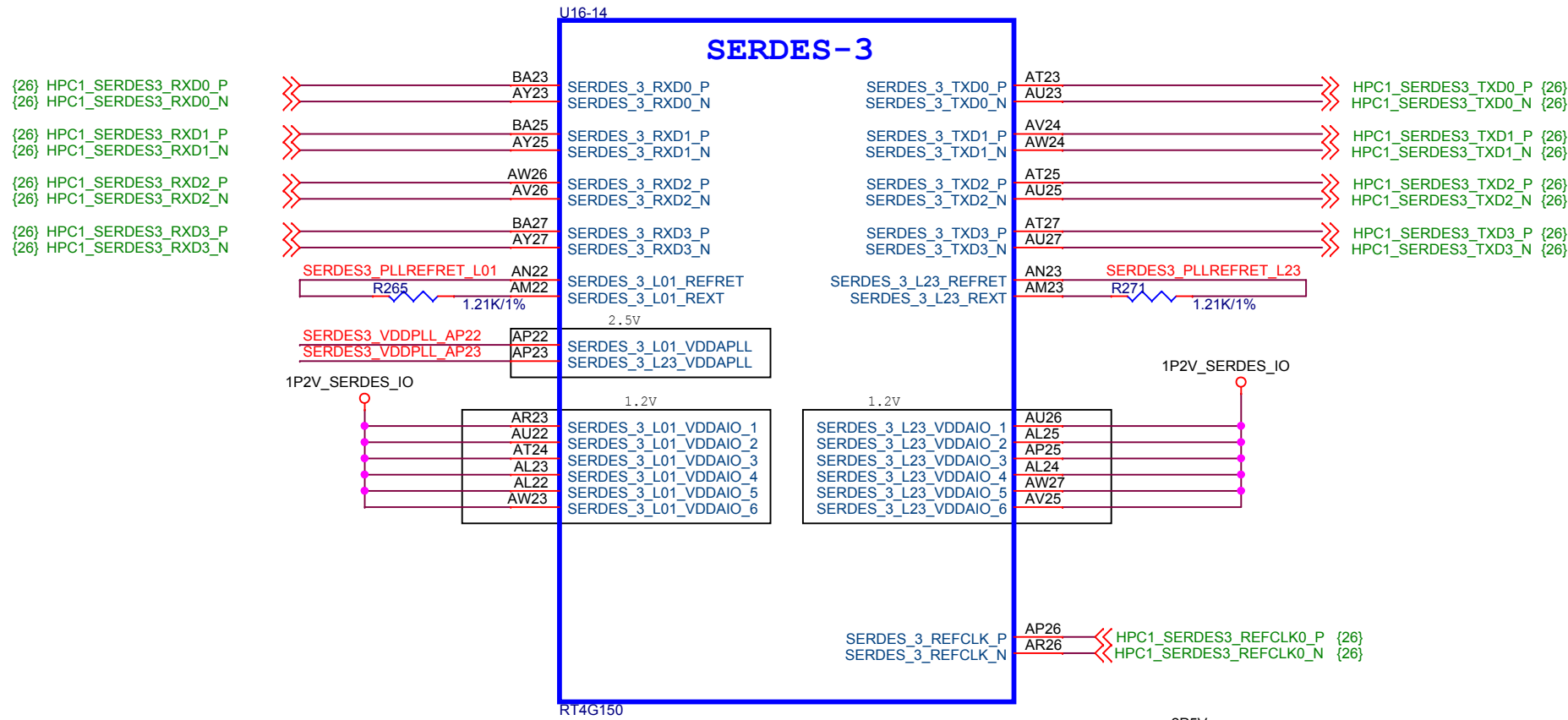
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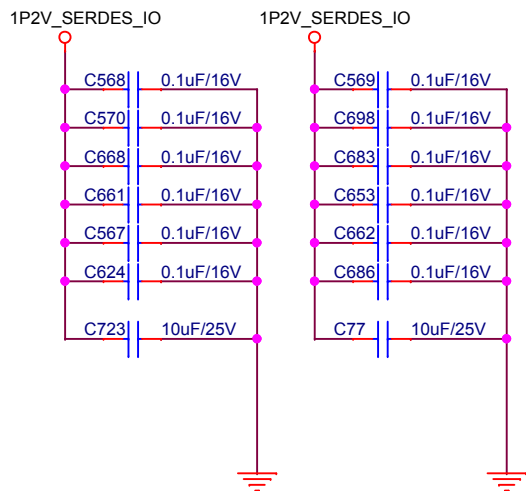


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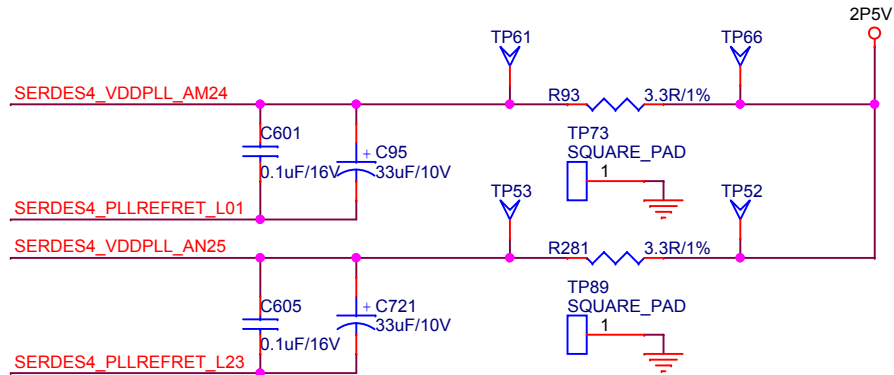
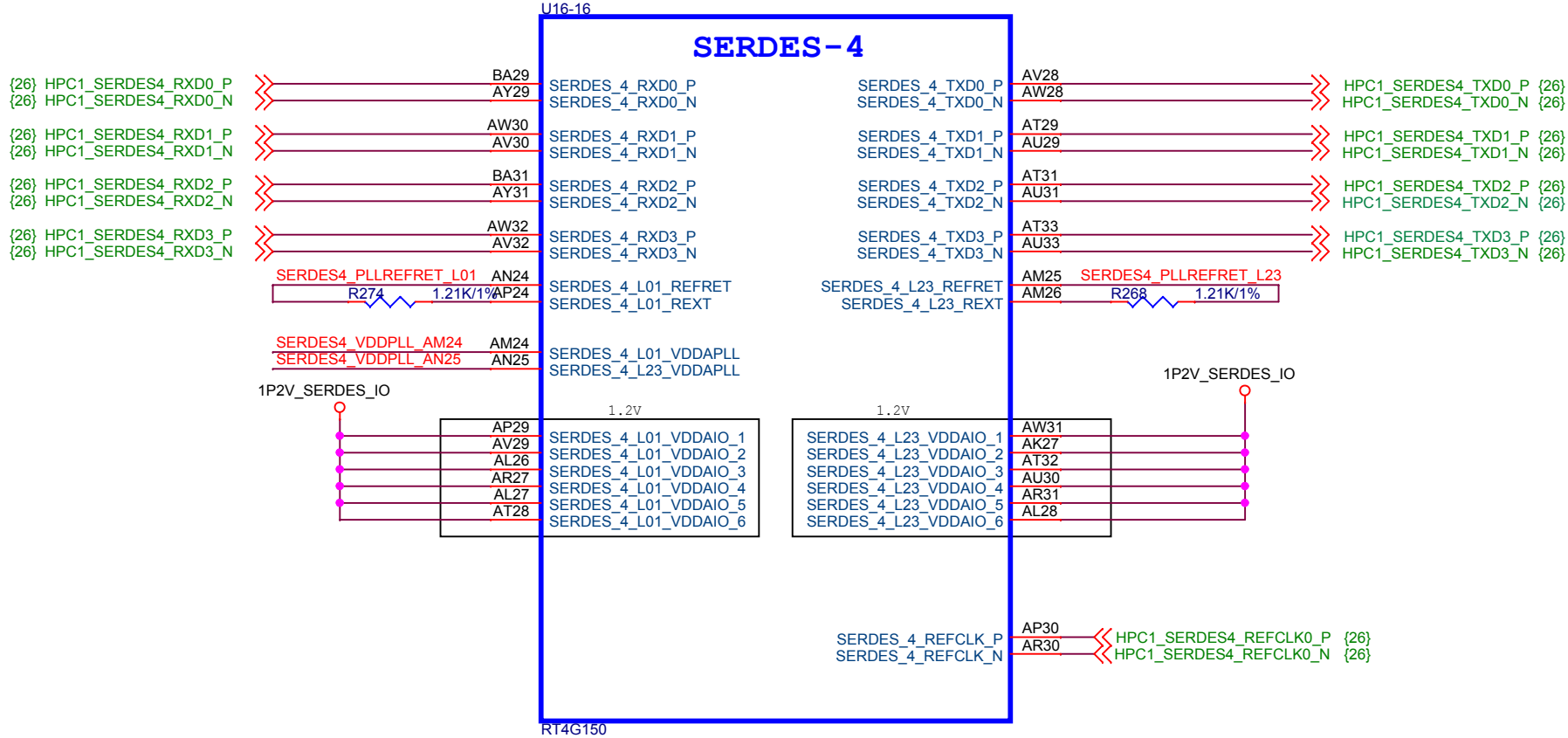
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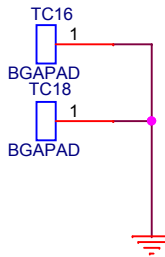
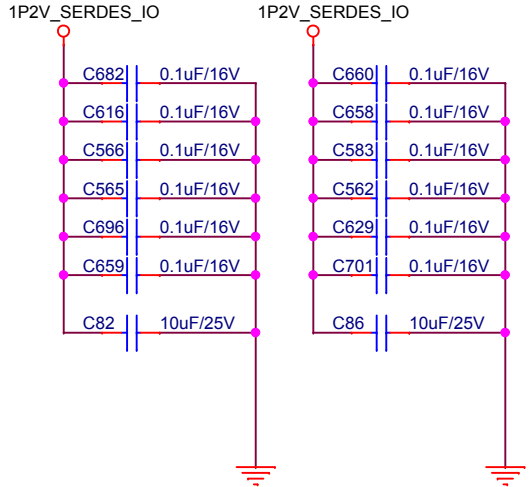
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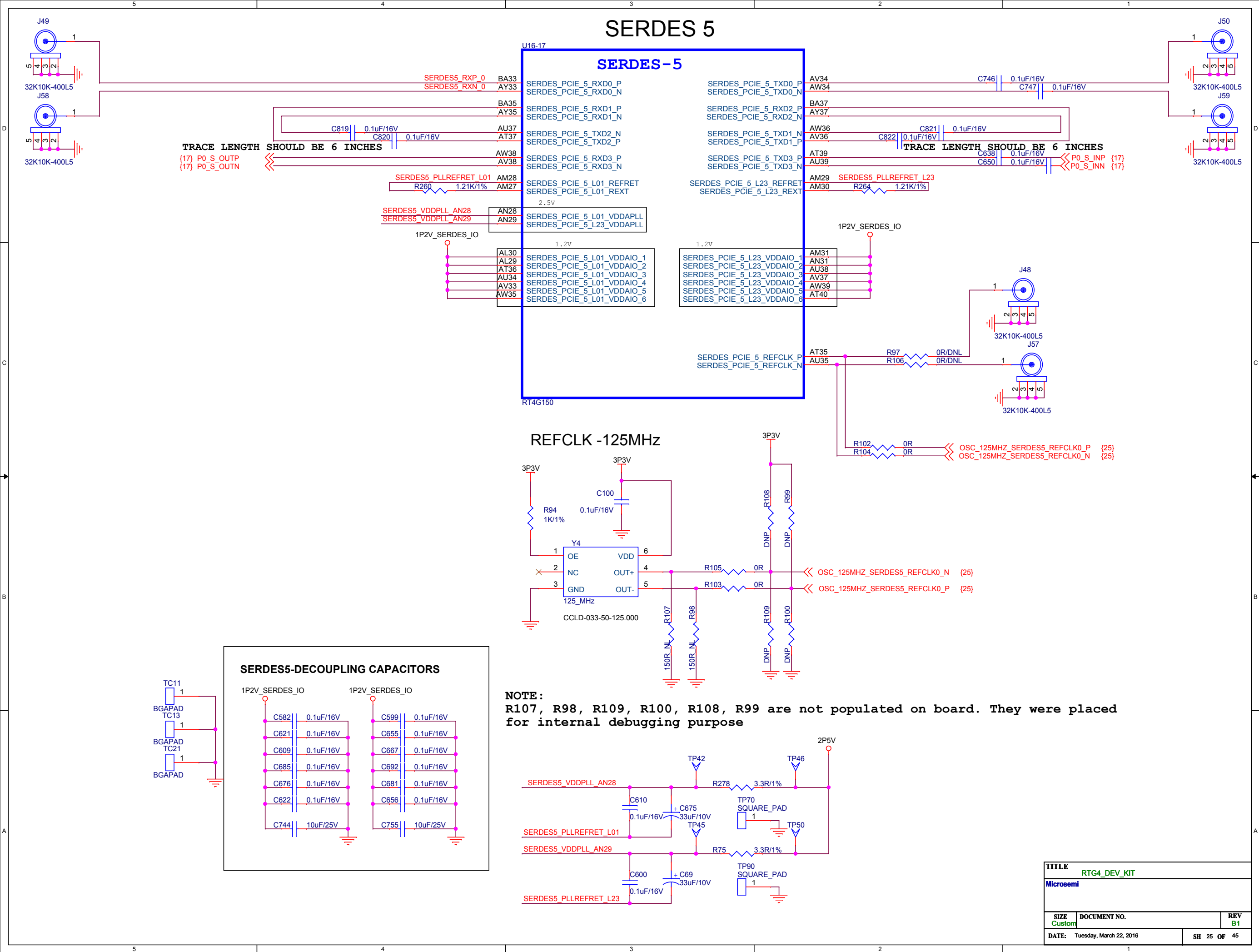
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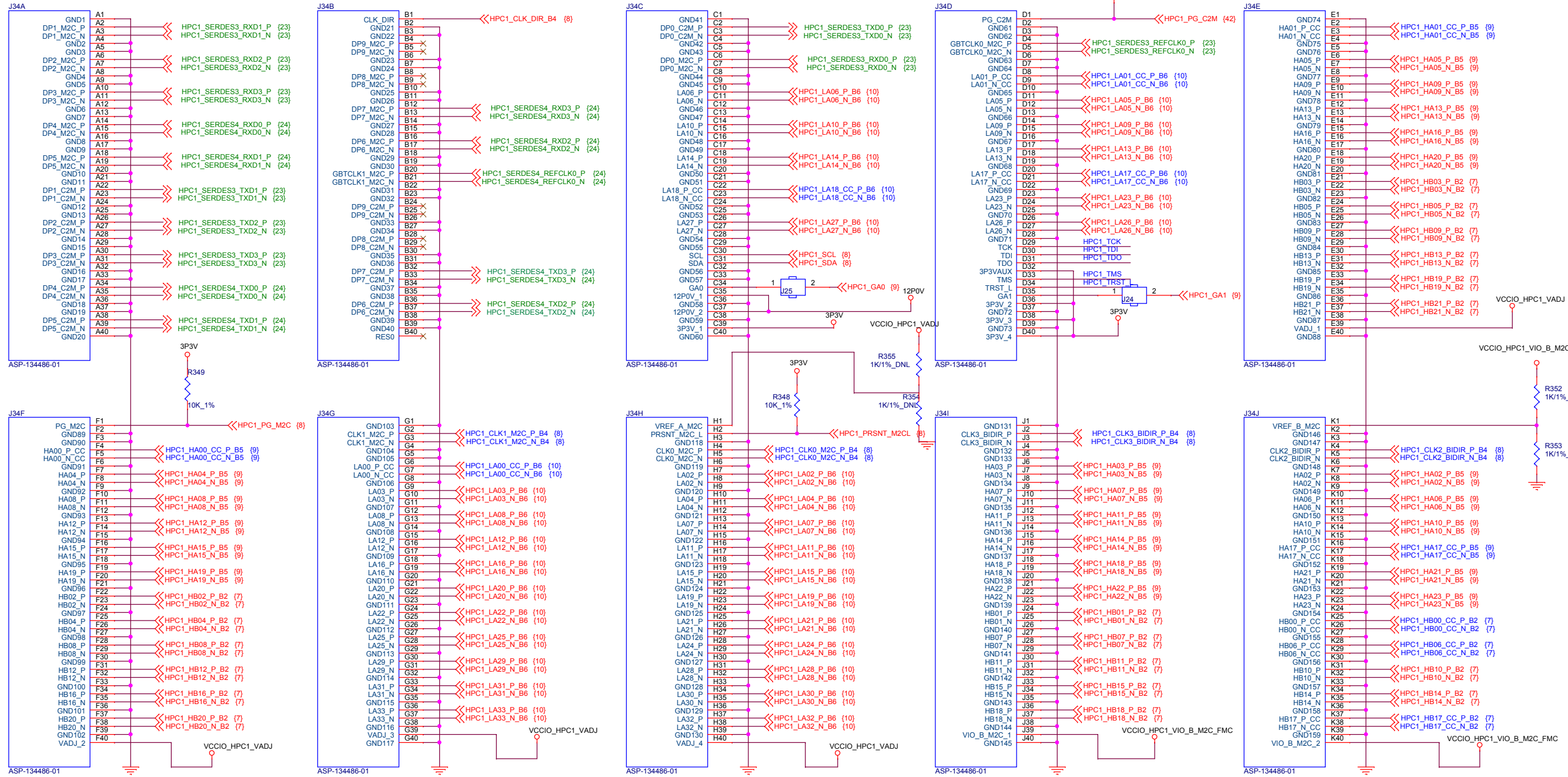
SERDES4-DECOUPLING CAPACITORS



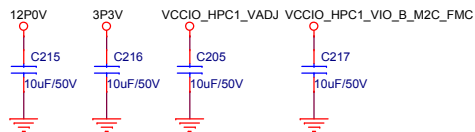
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# FMC CONNECTOR-HPC1



## DECOUPLING CAPACITORS



**NOTE:**

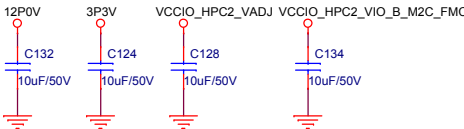
- 1.FMC HPC1 LA & HA bank IO's support maximum of 3.3V.
- 2.FMC HPC1 HB bank IO's support maximum of 2.5V.
- 3.The Supporting Voltages of FMC HPC1(VCCIO\_HPC1\_VADJ) are 1.2V,1.5V,1.8V, 2.5V and 3.3V.

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FMC CONNECTOR-HPC2



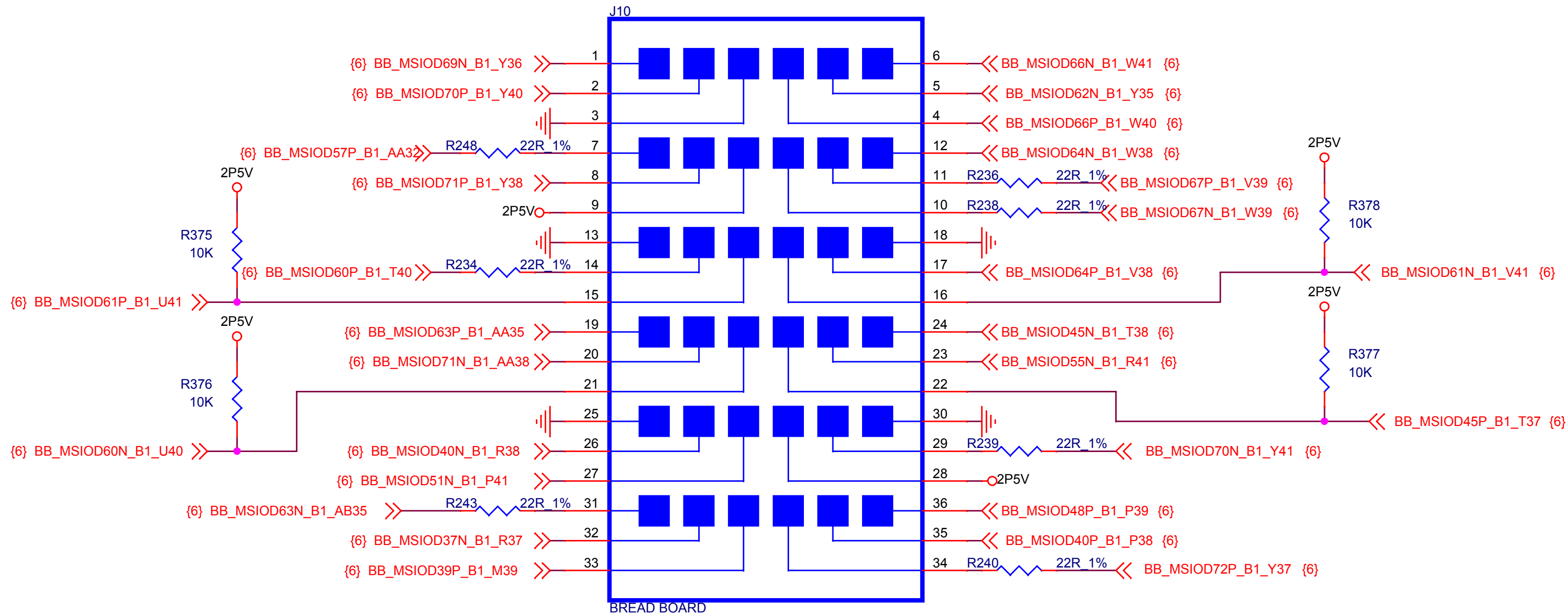
DECOUPLING CAPACITORS



**NOTE:**  
1.FMC HPC2 IO's support maximum of 2.5V  
2.The Supporting Voltages of FMC HPC2(VCCIO\_HPC2\_VADJ) are 1.2V,1.5V,1.8V and 2.5V.

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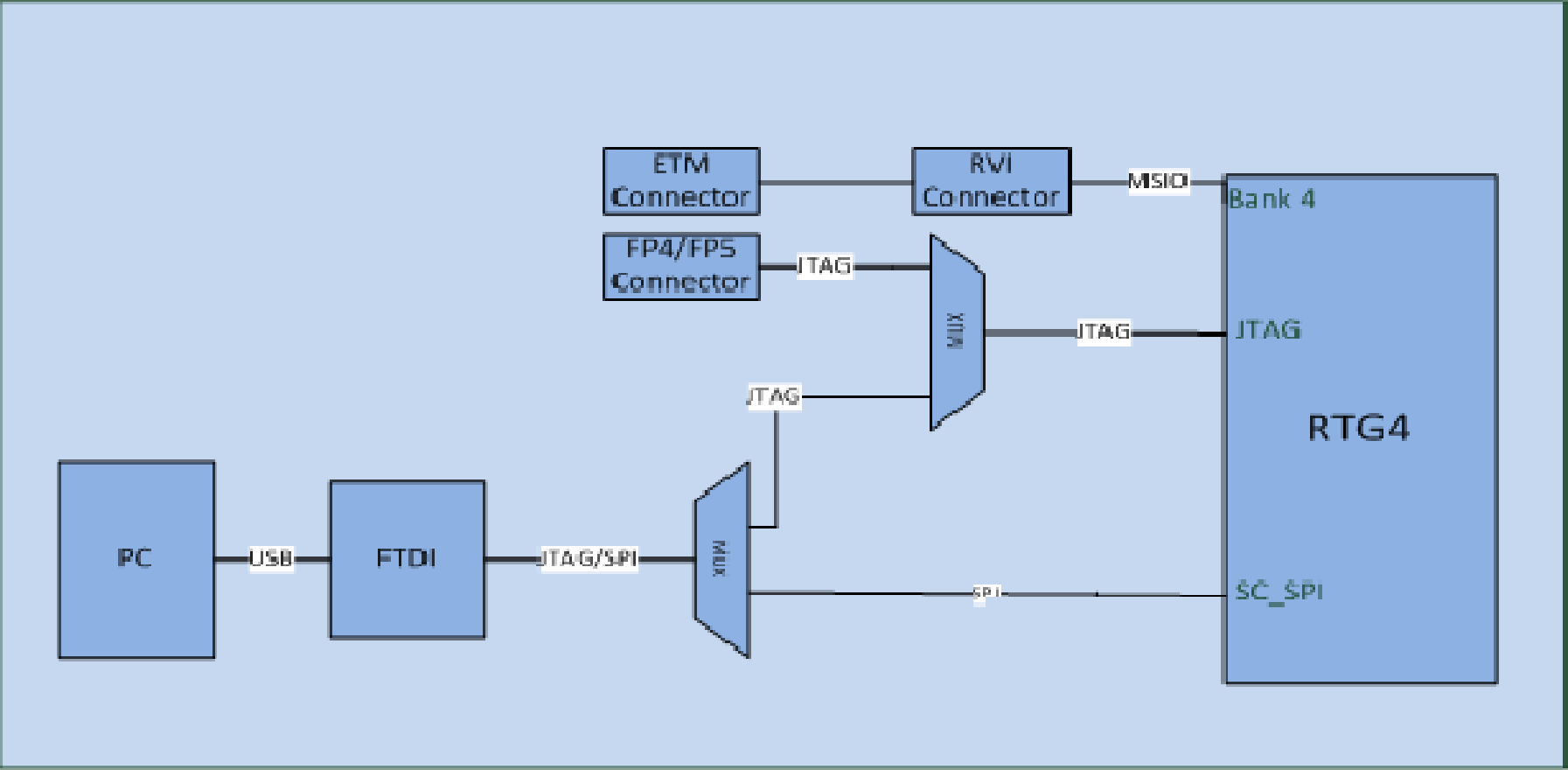
# BREAD BOARD CONNECTOR



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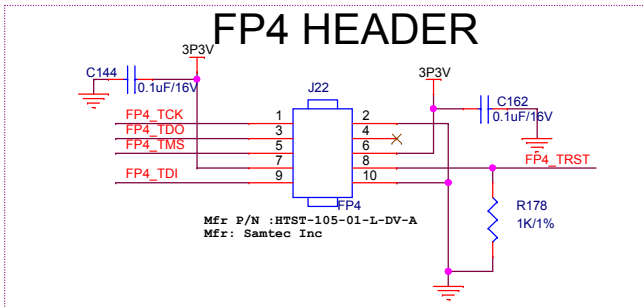
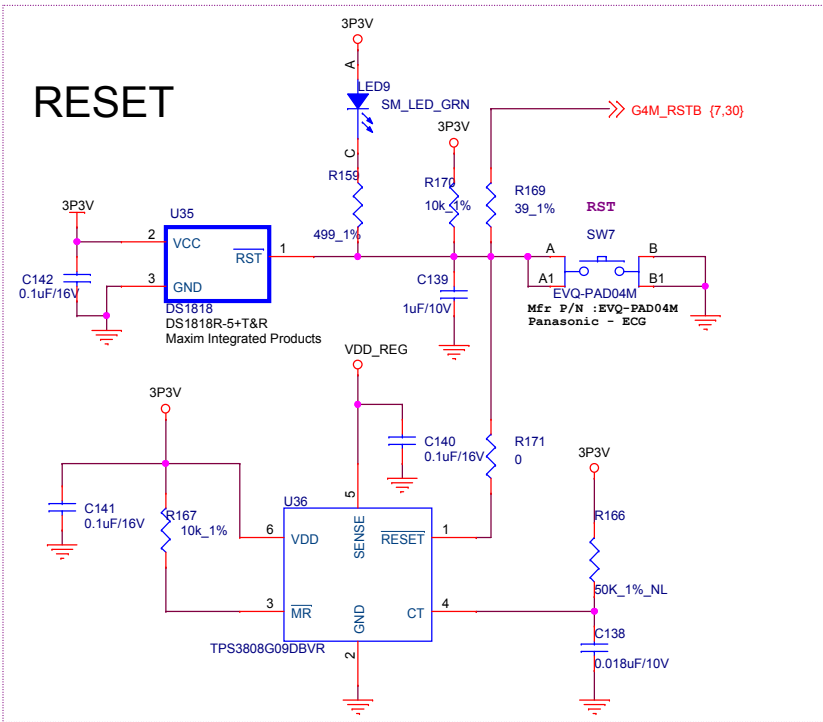
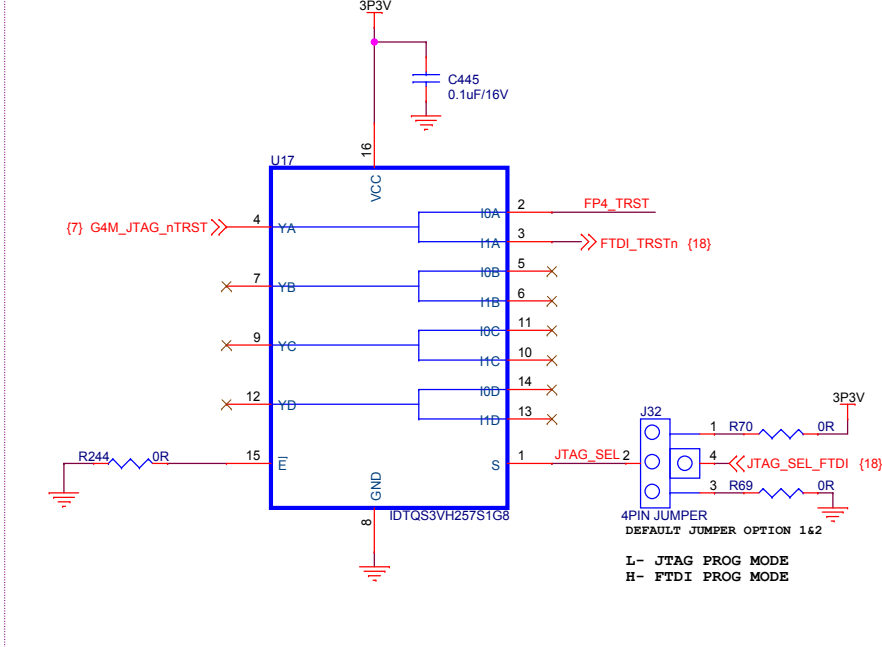
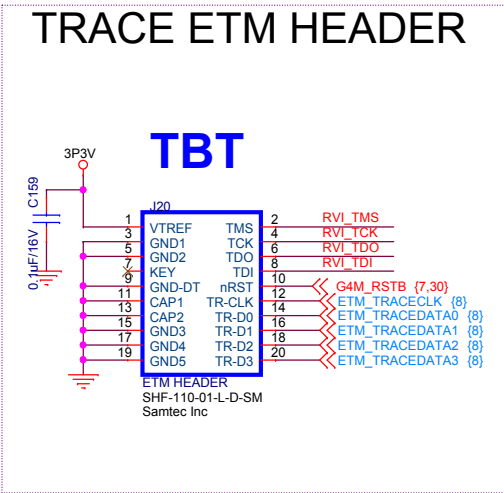
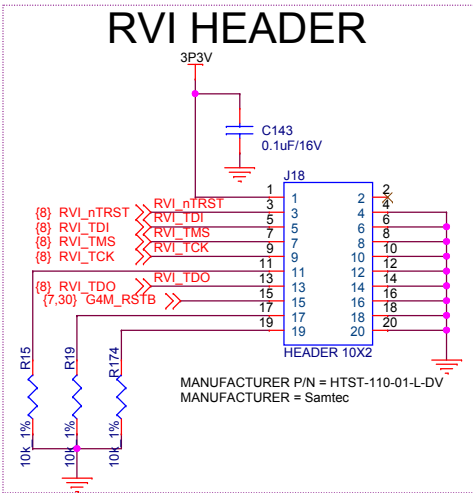
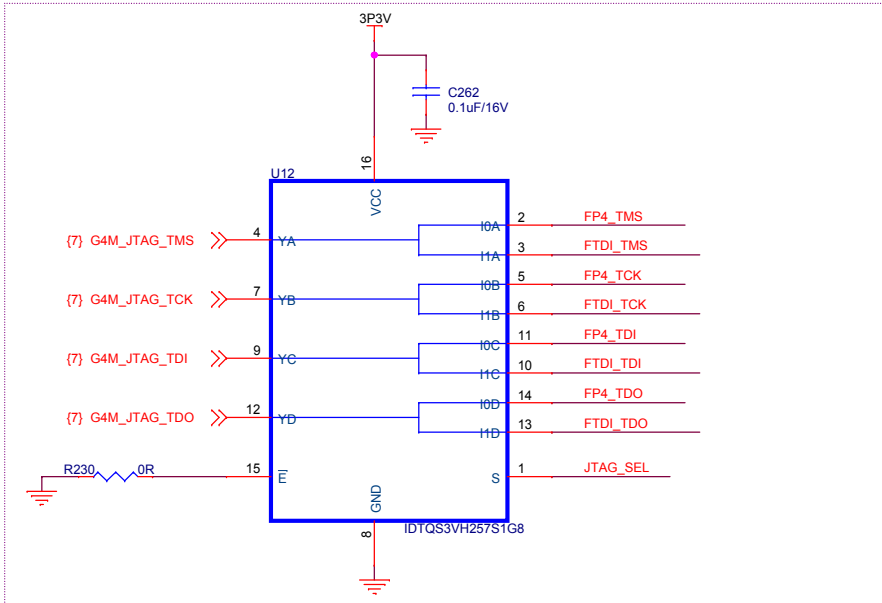
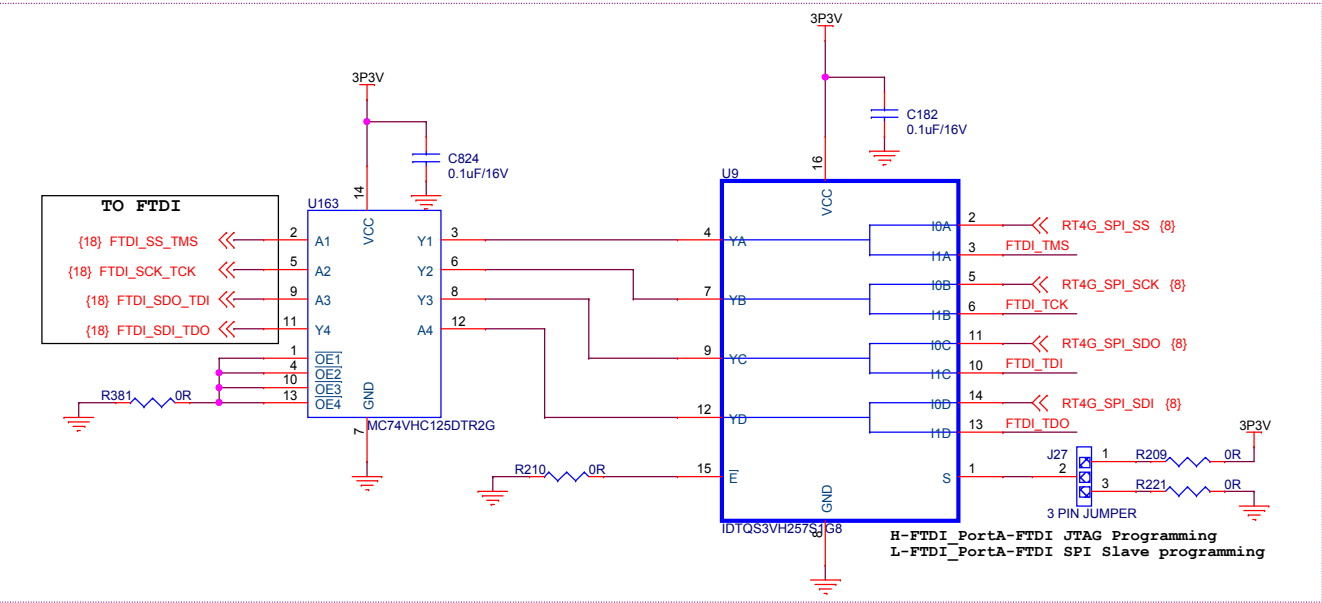


# PROGRAMING SCHEME



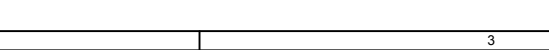
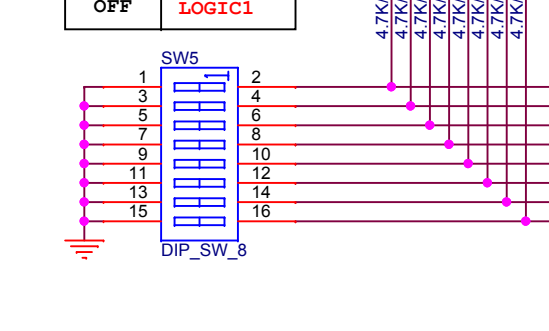
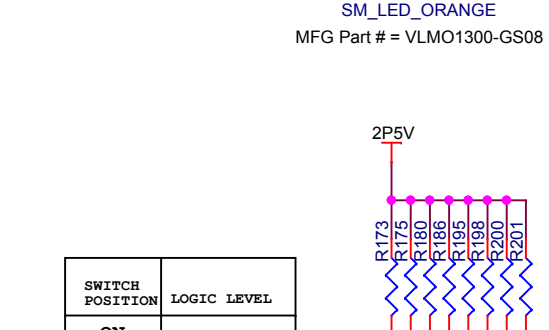
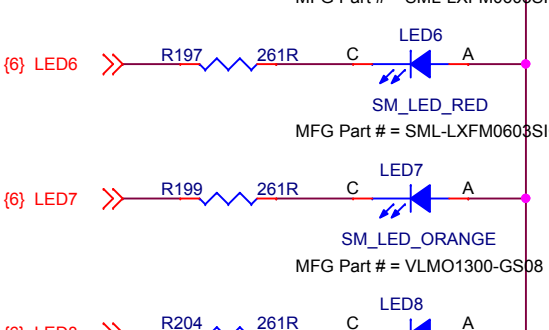
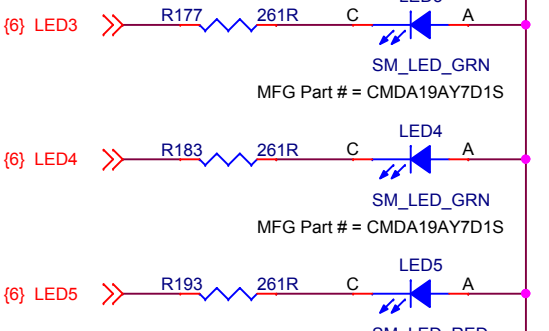
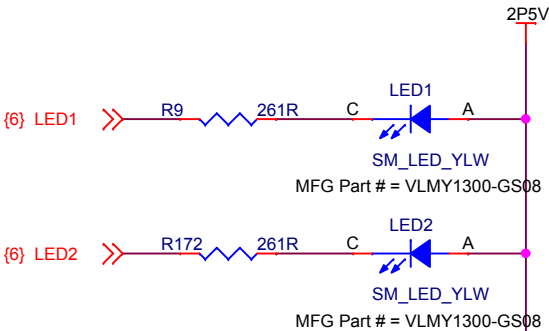
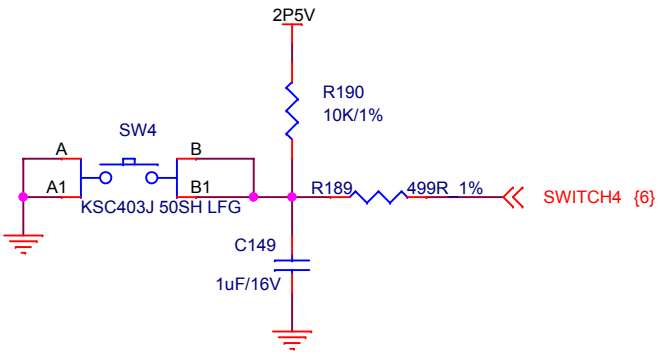
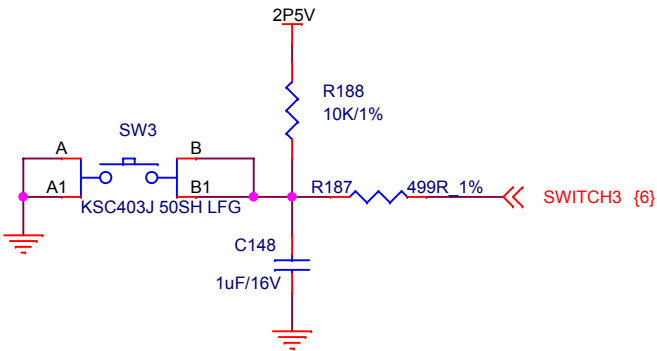
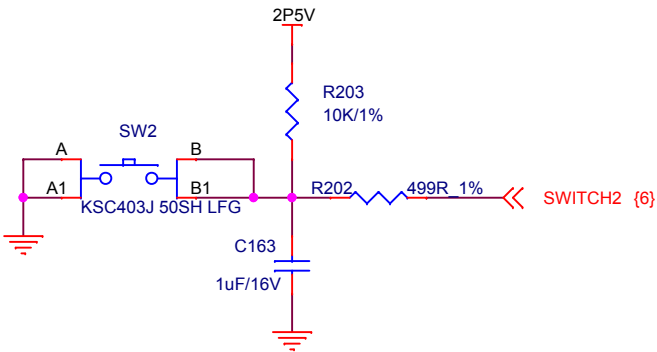
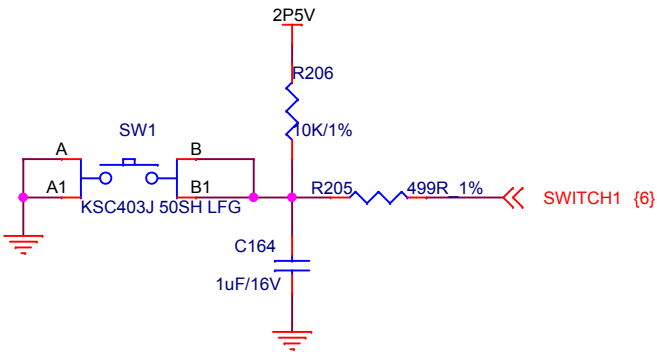
TITLE			
RTG4_DEV_KIT			
Microsemi			
SIZE	DOCUMENT NO.		REV
A			B1
DATE:	Tuesday, March 22, 2016	SH 29 OF 45	

# PROGRAMING CIRCUITRY

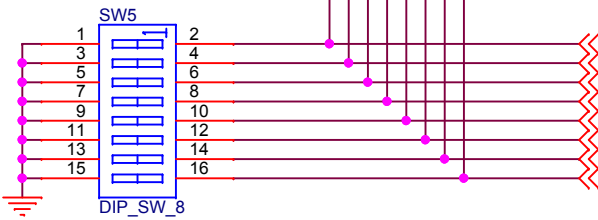


TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE:	Tuesday, March 22, 2016	SH 30 OF 45

DEBUG CIRCUITRY



SWITCH POSITION	LOGIC LEVEL
ON	GND
OFF	LOGIC1



NET NAME	FPGA PIN NAME	FPGA PIN NO
SWITCH1	MSIOD68NB1	AA30
SWITCH2	MSIOD65PB1	AB31
SWITCH3	MSIOD68PB1	AB30
SWITCH4	MSIOD65NB1	AB32

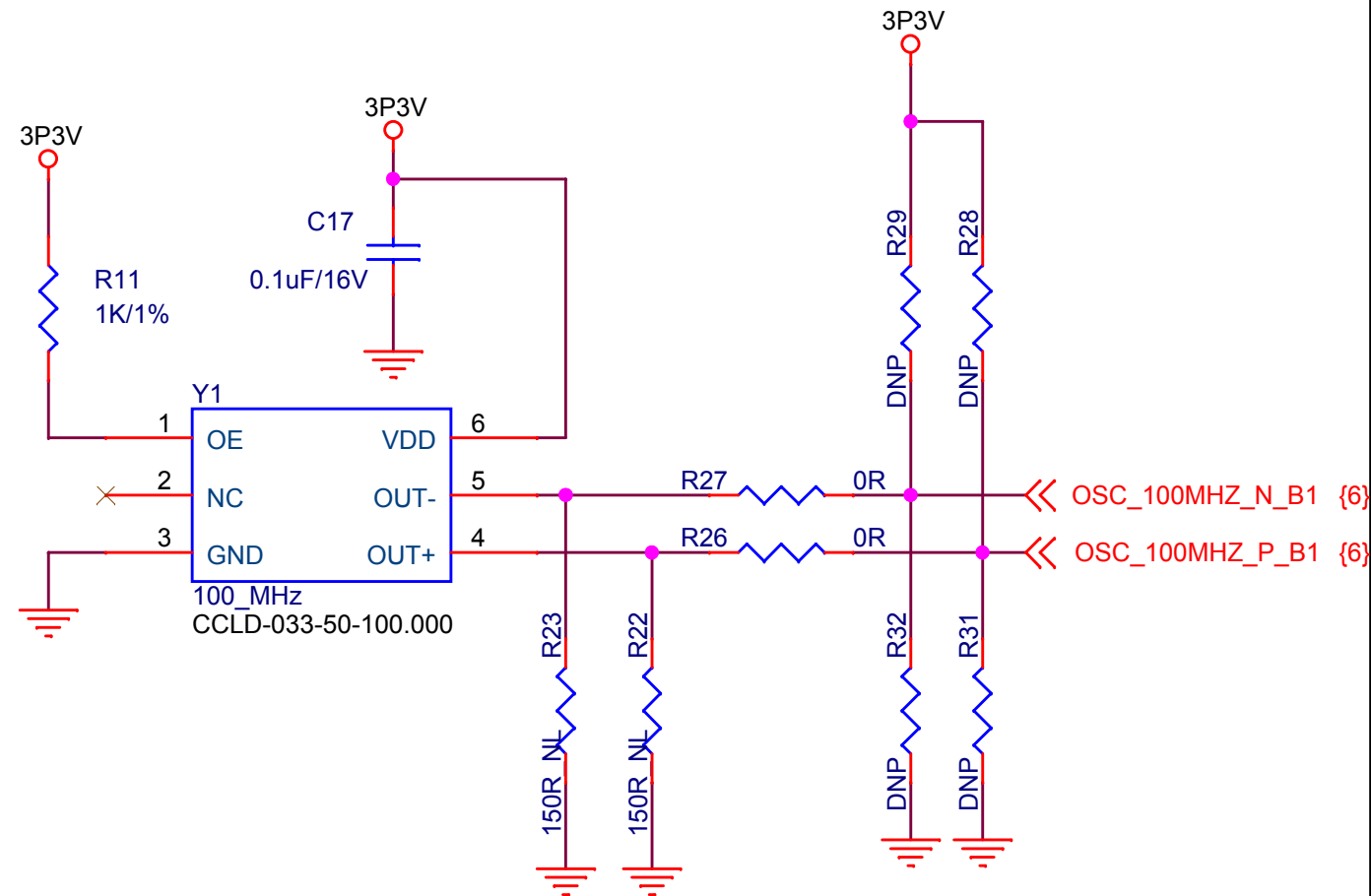
NET NAME	FPGA PIN NAME	FPGA PIN NO
LED1	MSIOD62PB1	W35
LED2	MSIOD46PB1	W34
LED3	MSIOD47PB1	V30
LED4	MSIOD46NB1	W33
LED5	MSIOD38PB1	T33
LED6	MSIOD41NB1	U35
LED7	MSIOD37PB1	R36
LED8	MSIOD38NB1	T34

NET NAME	FPGA PIN NAME	FPGA PIN NO
DIP1	MSIOD57NB1	AA33
DIP2	MSIOD56PB1	Y31
DIP3	MSIOD56NB1	W31
DIP4	MSIOD47NB1	W30
DIP5	MSIOD42NB1	V33
DIP6	MSIOD42PB1	V34
DIP7	MSIOD41PB1	U34
DIP8	MSIOD69PB1	W36

TITLE RTG4_DEV_KIT		
Microsemi		
SIZE Custom	DOCUMENT NO.	REV B1
DATE: Tuesday, March 22, 2016	SH 31 OF 45	

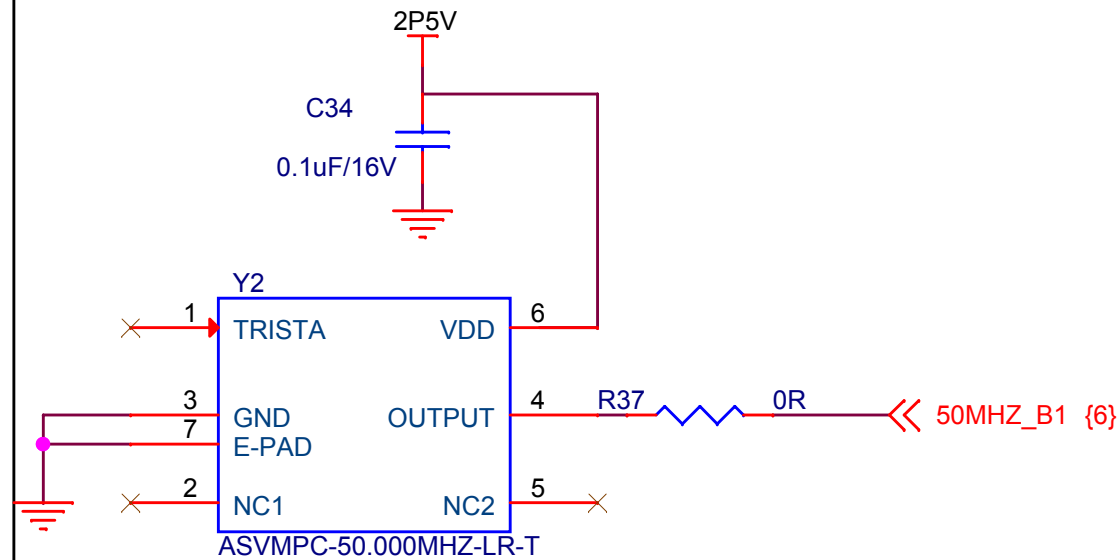
# CLOCK CIRCUITRY

## CLK -100MHz



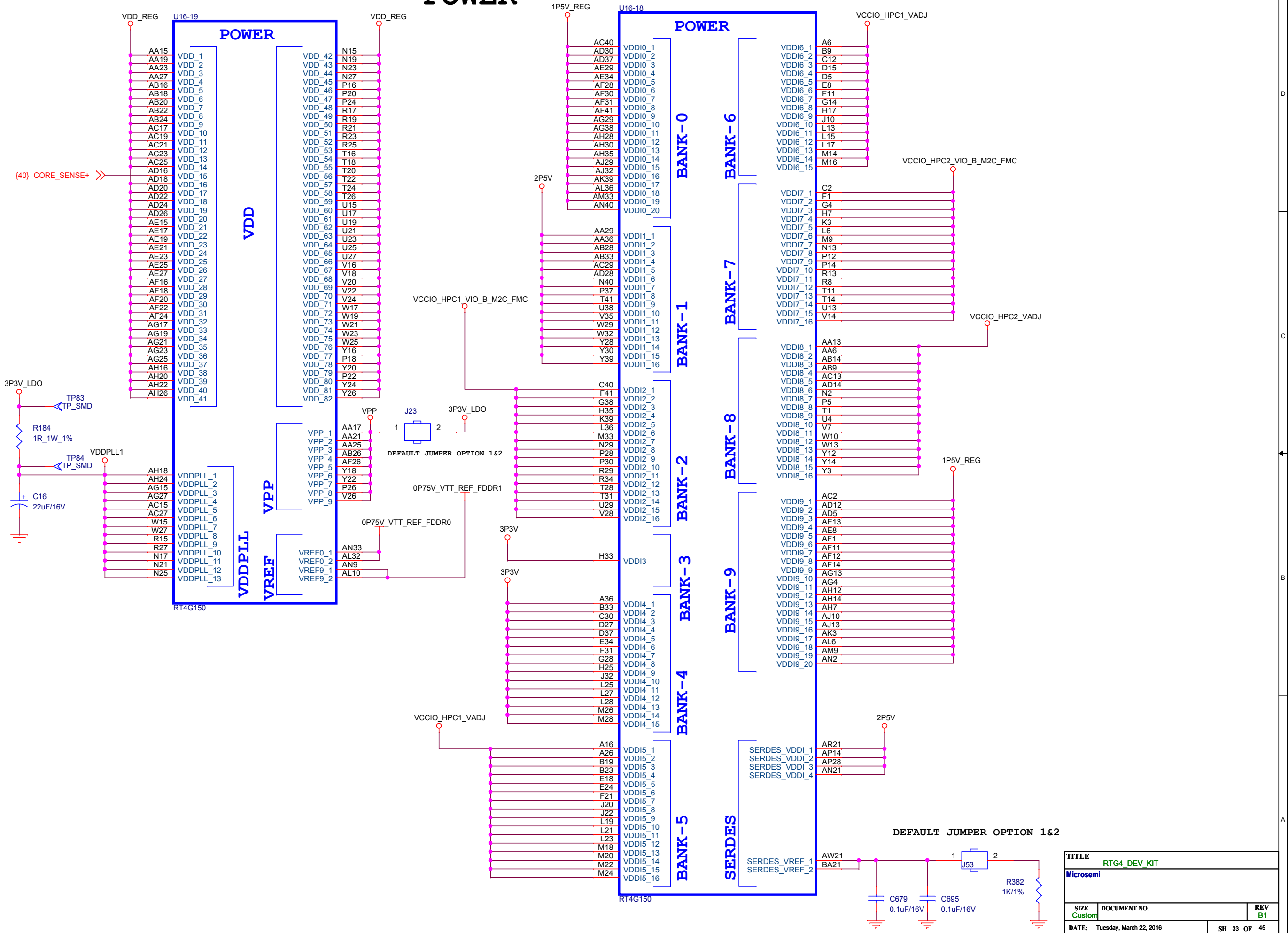
**NOTE:**  
R23, R22, R29, R28, R32, R31 are not populated on board. They were placed for internal debugging purpose

## CLK -50MHz



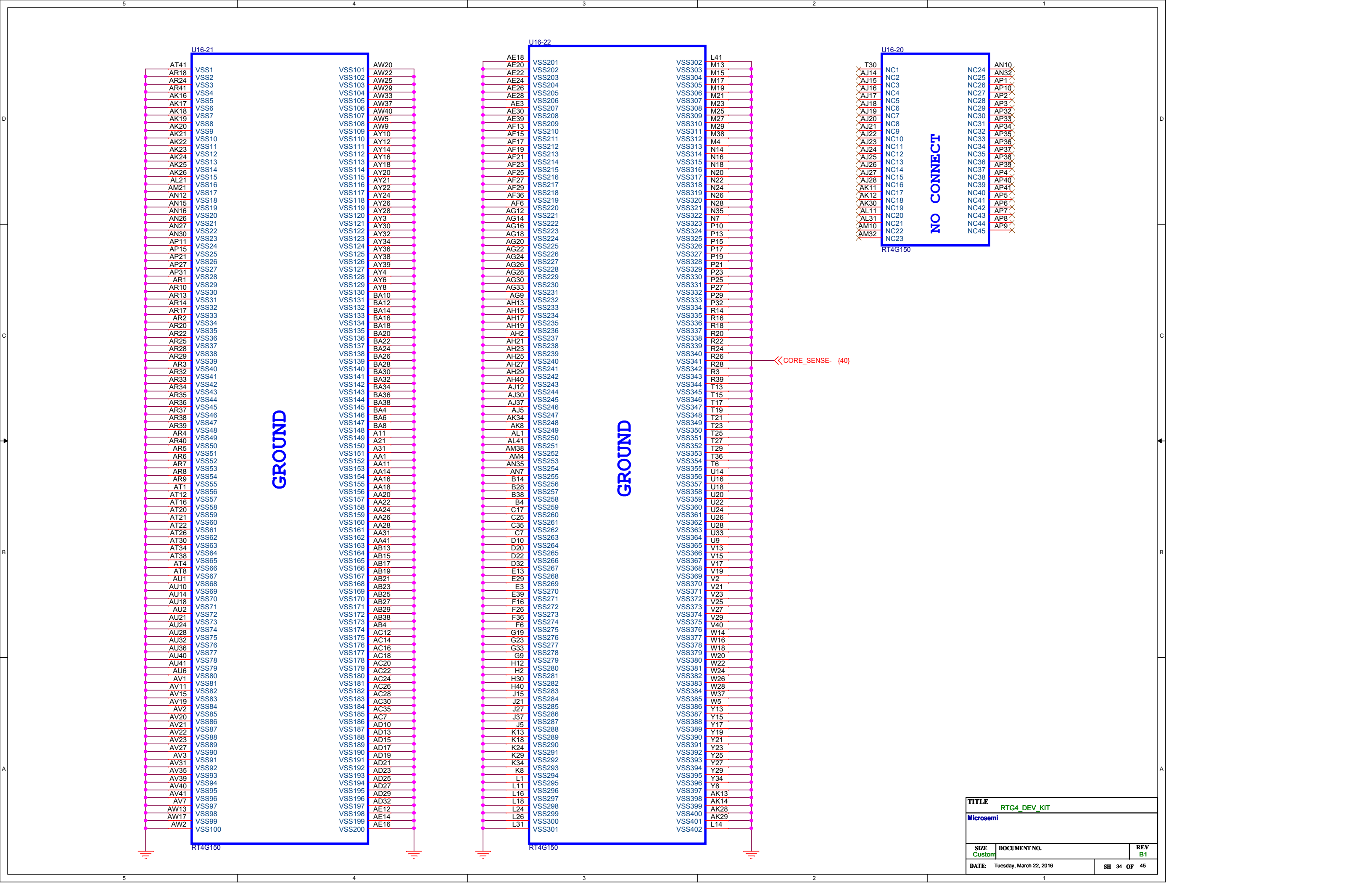
TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
A		B1
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POWER



TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE:	Tuesday, March 22, 2016	SH 33 OF 45





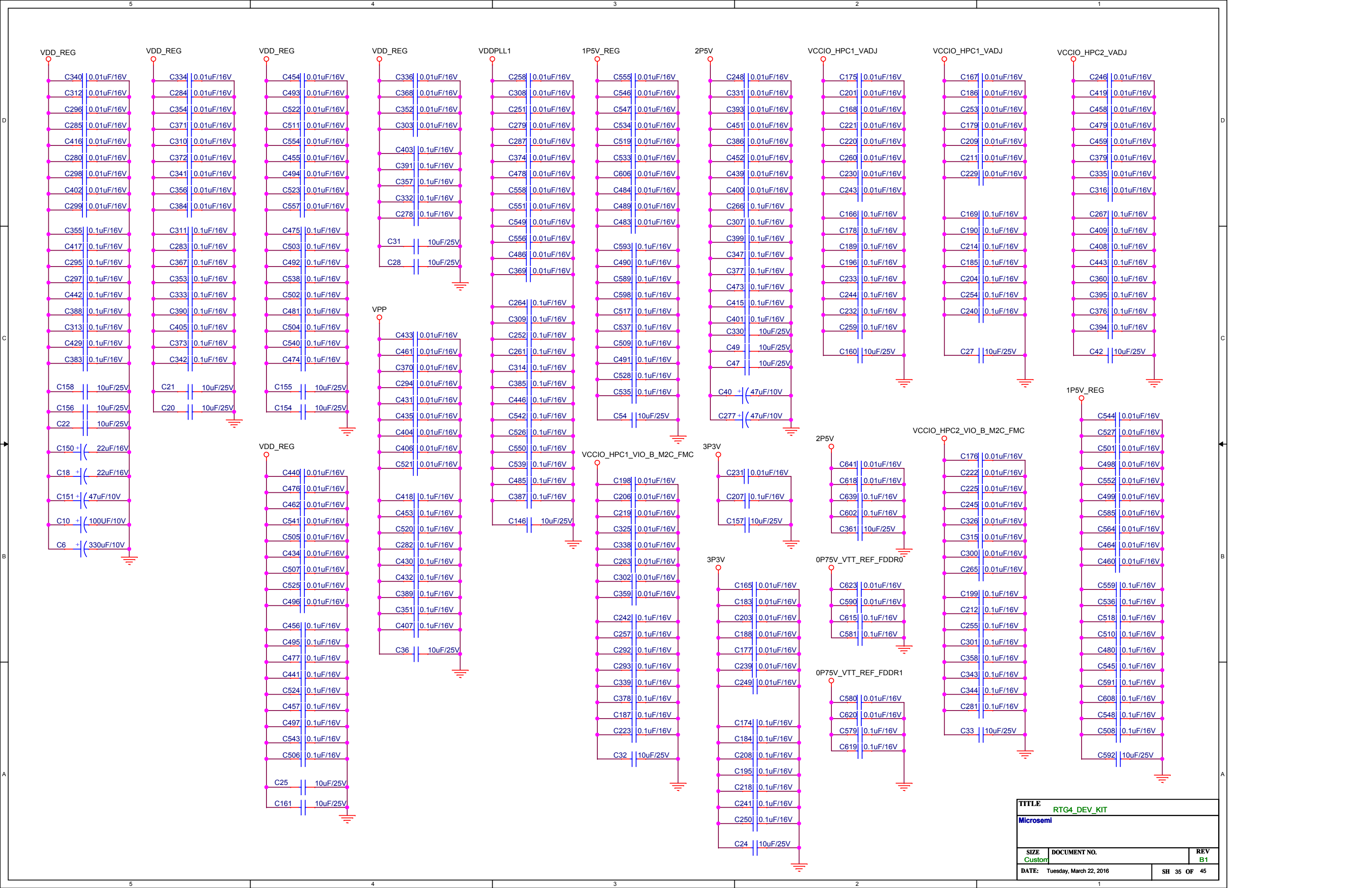
GROUND

GROUND

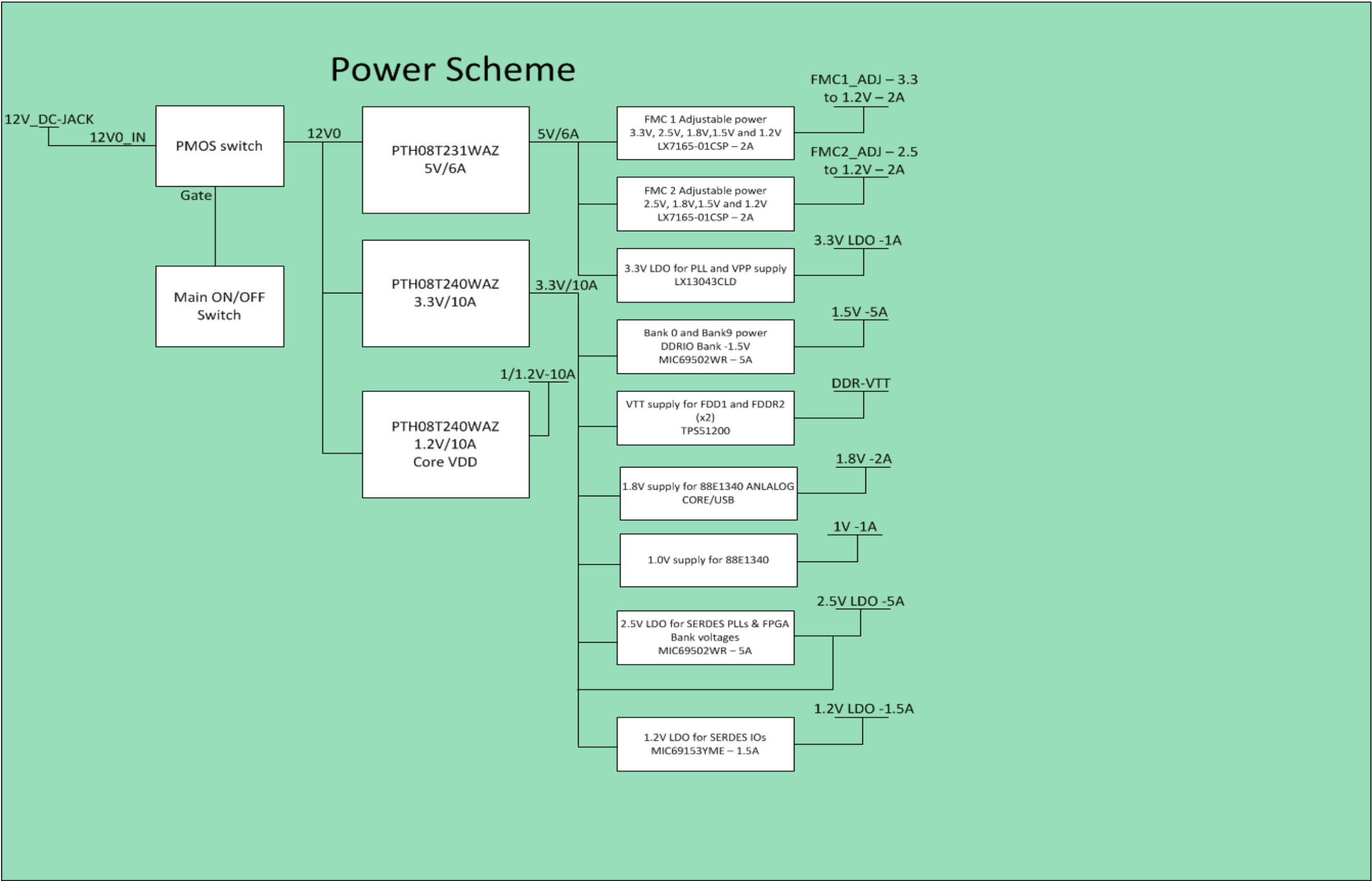
NO CONNECT

<<CORE\_SENSE- {40}>

TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE:	Tuesday, March 22, 2016	SH 34 OF 45

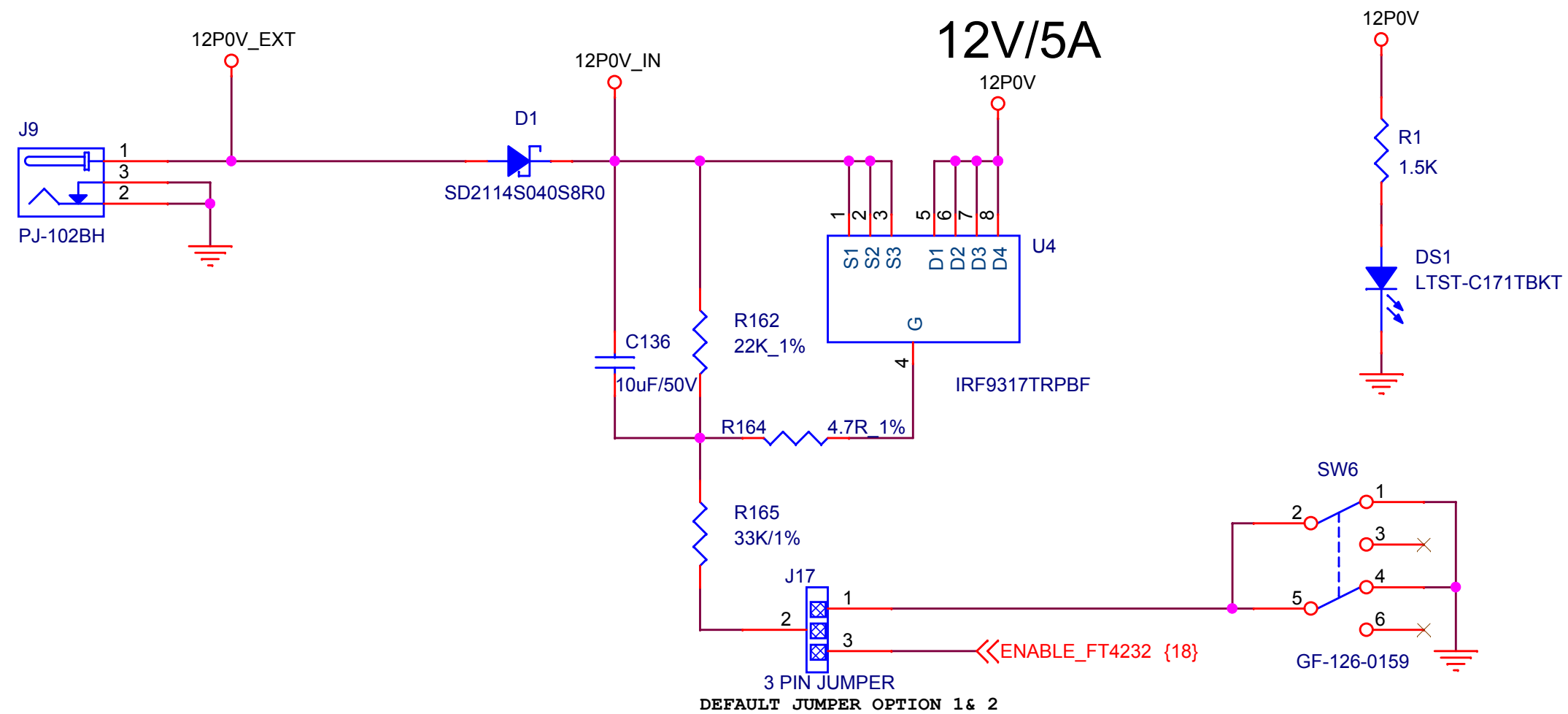


TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE: Tuesday, March 22, 2016		SH 35 OF 45

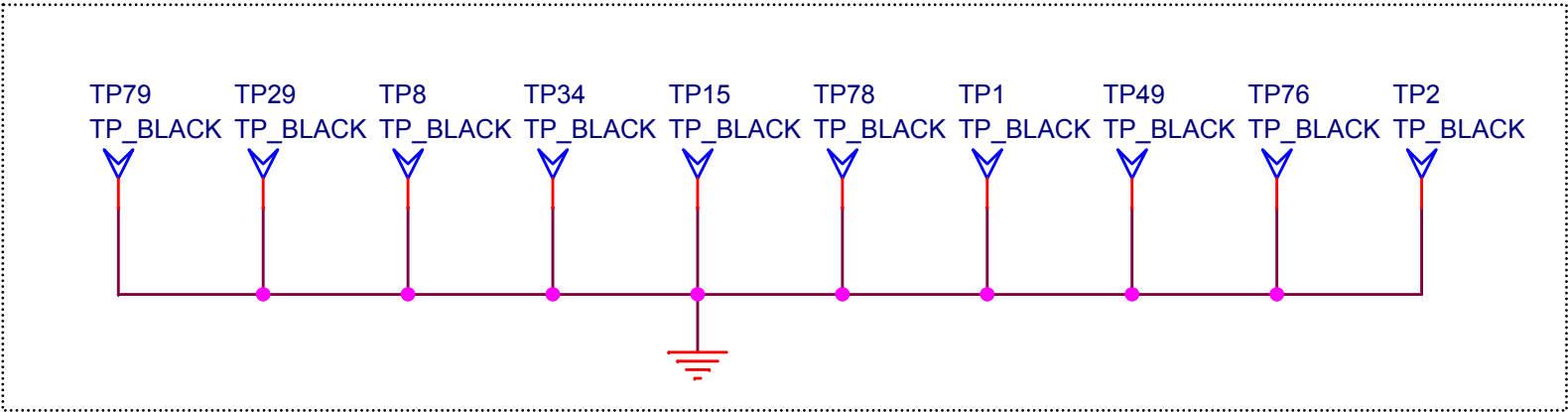
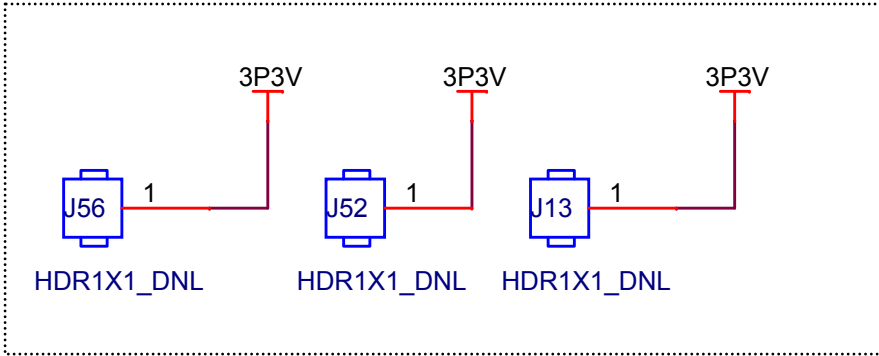
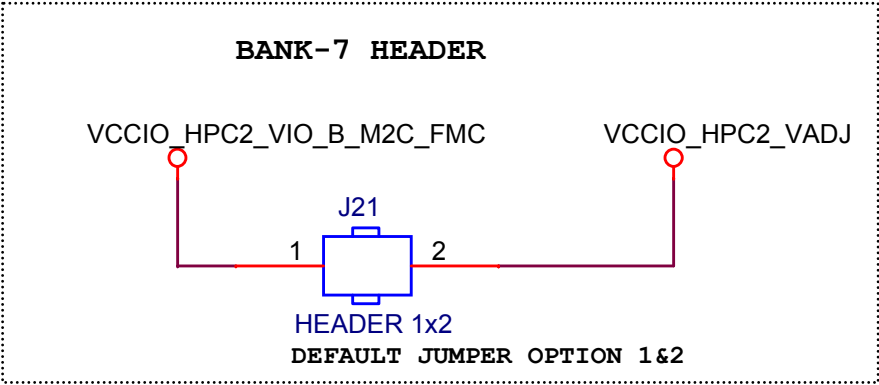
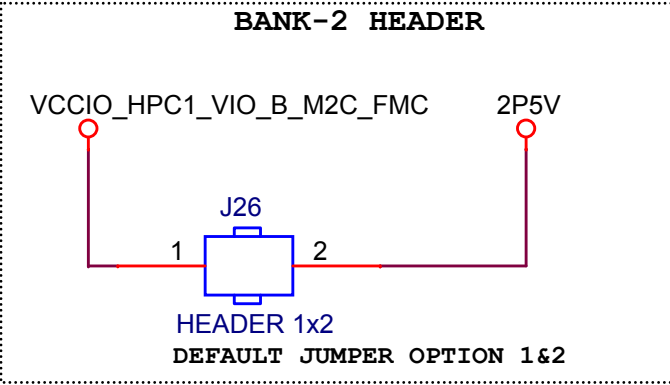


TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
B		B1
DATE:	Tuesday, March 22, 2016	SH 36 OF 45

# 12V EXTERNAL SUPPLY



TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
A		B1
DATE:	Tuesday, March 22, 2016	SH 37 OF 45

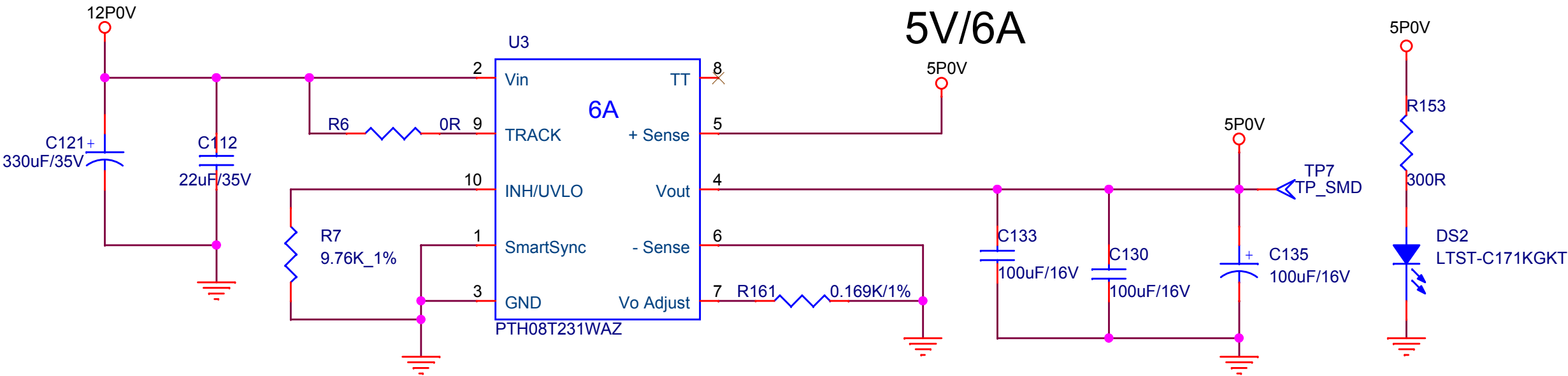


TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
A		B1
DATE:	Tuesday, March 22, 2016	SH 38 OF 45

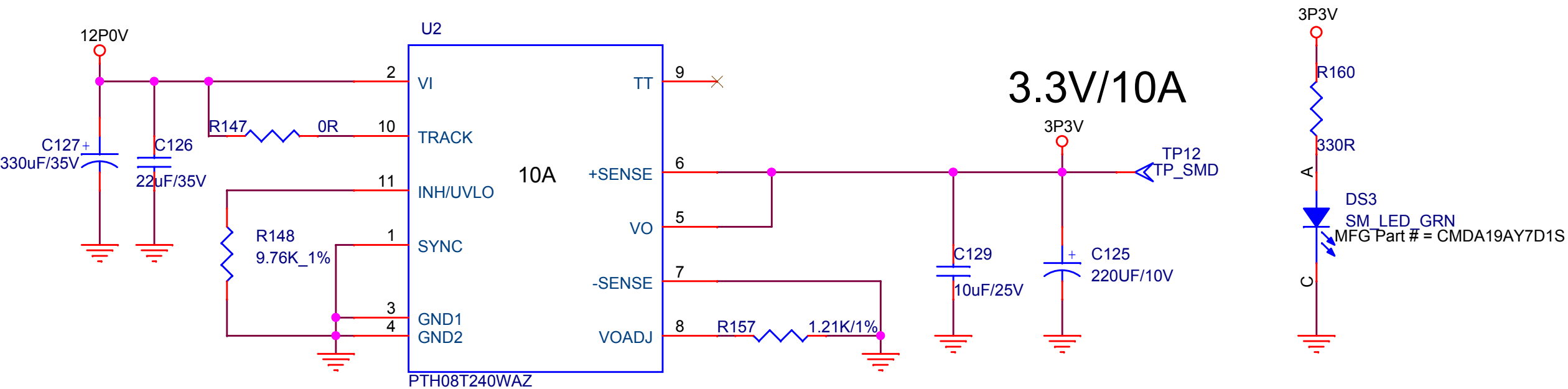


# POWER SUPPLIES - 1

REGULATOR 1: 5V/6A



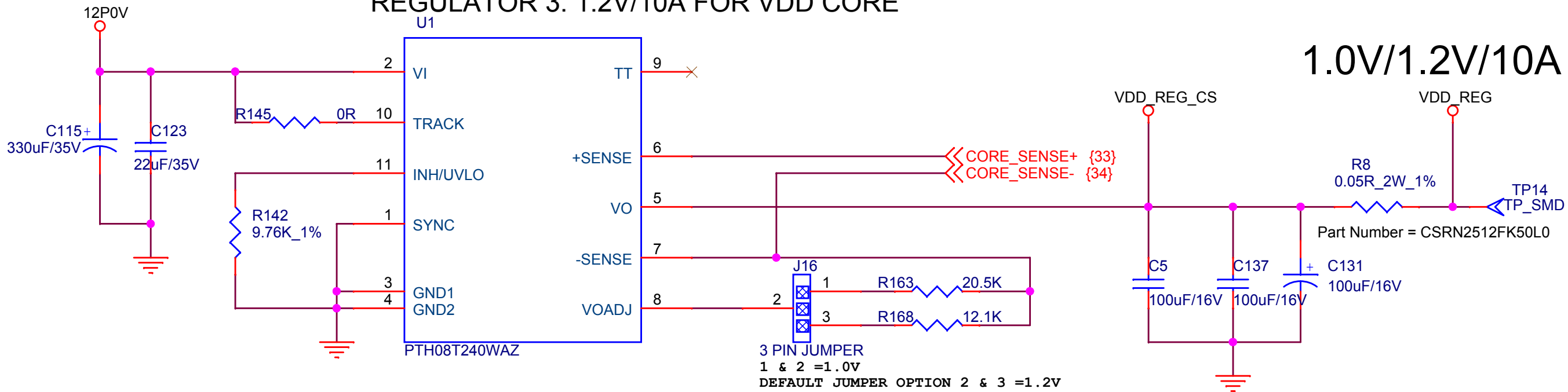
REGULATOR 2: 3.3V/10A



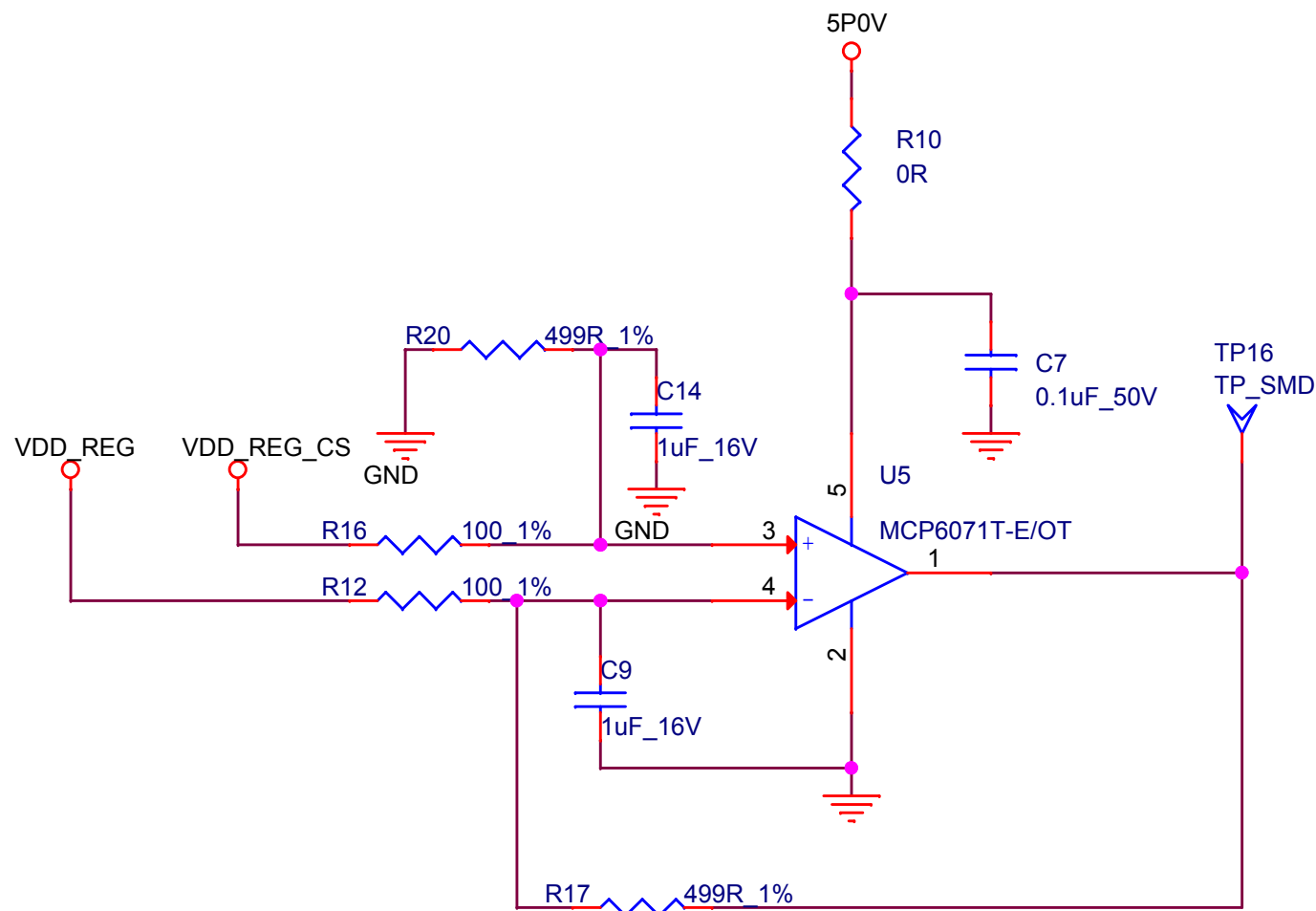
TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE:	Tuesday, March 22, 2016	SH 39 OF 45

# POWER SUPPLIES - 2

## REGULATOR 3: 1.2V/10A FOR VDD CORE



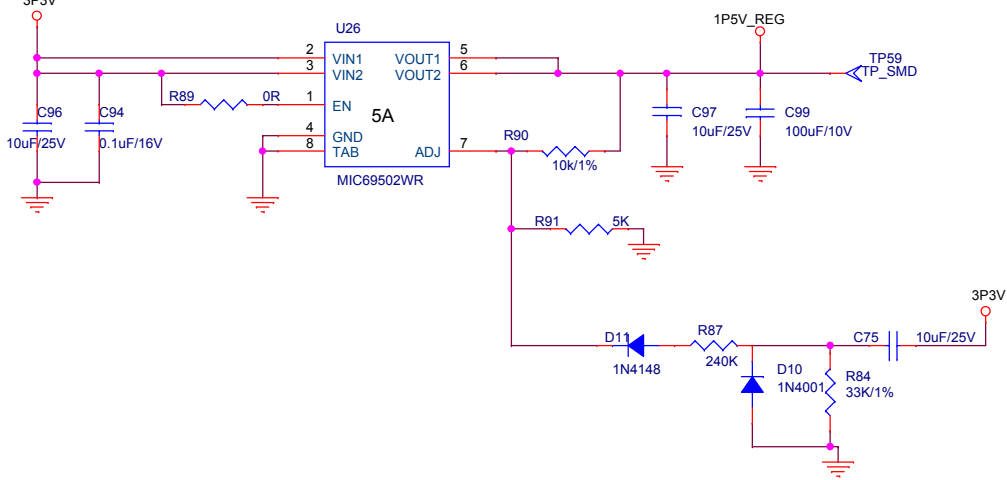
## CORE CURRENT SENSING CIRCUIT



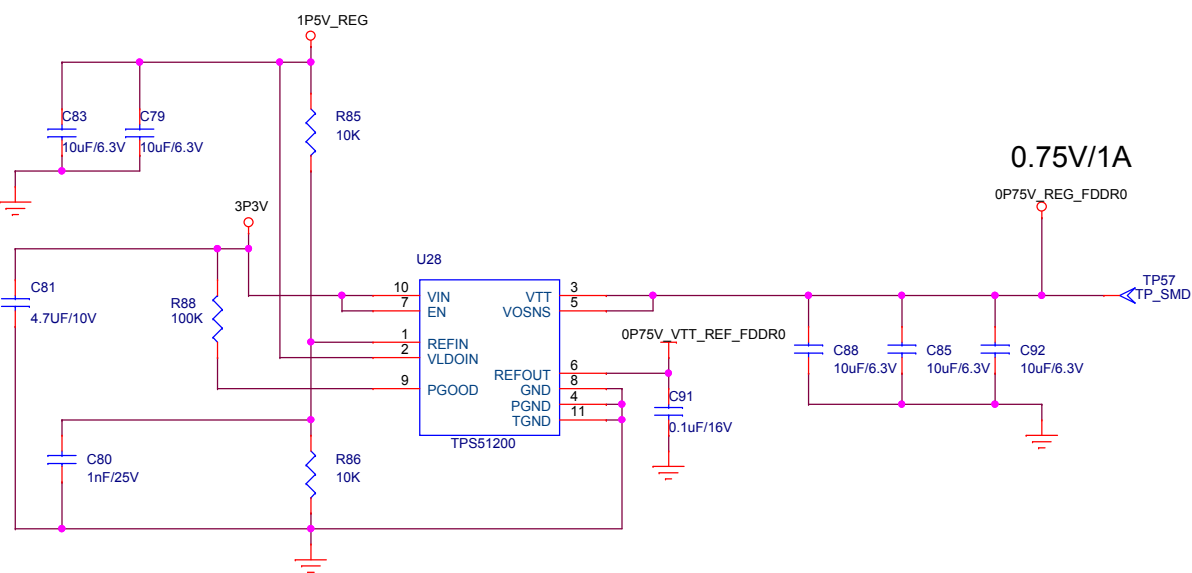
TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
A		B1
DATE:	Tuesday, March 22, 2016	SH 40 OF 45

POWER SUPPLIES 3

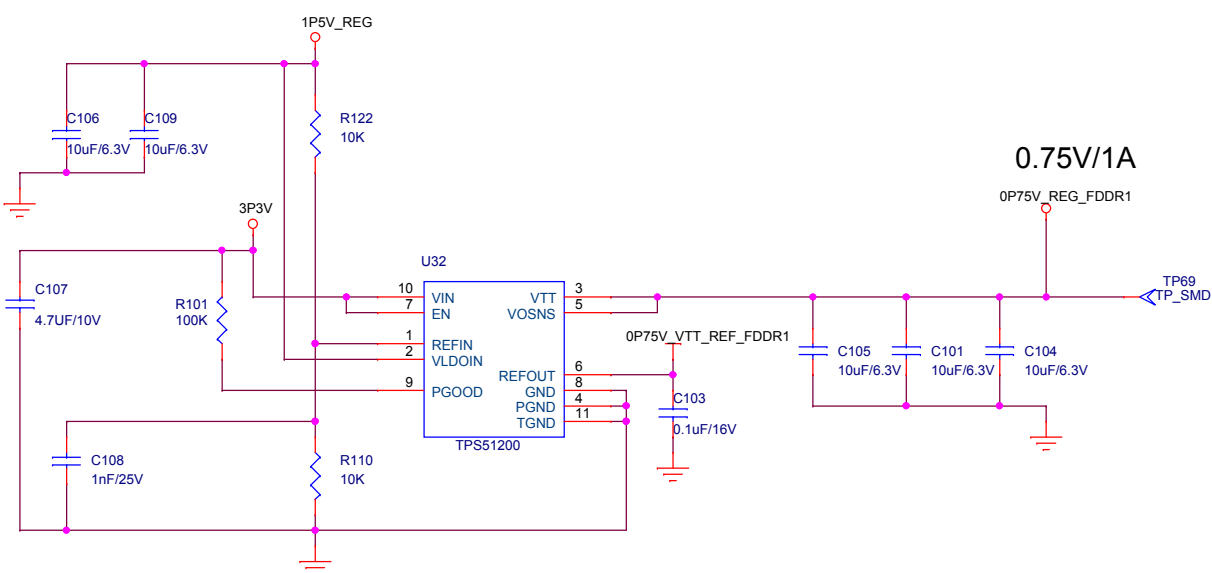
REGULATOR 4 : 3.3V to 1.5V FOR BANK 0 AND BANK 9  
1.5V/5A



REGULATOR 5: 0.75V FOR FDDR-0 -VTT SUPPLY



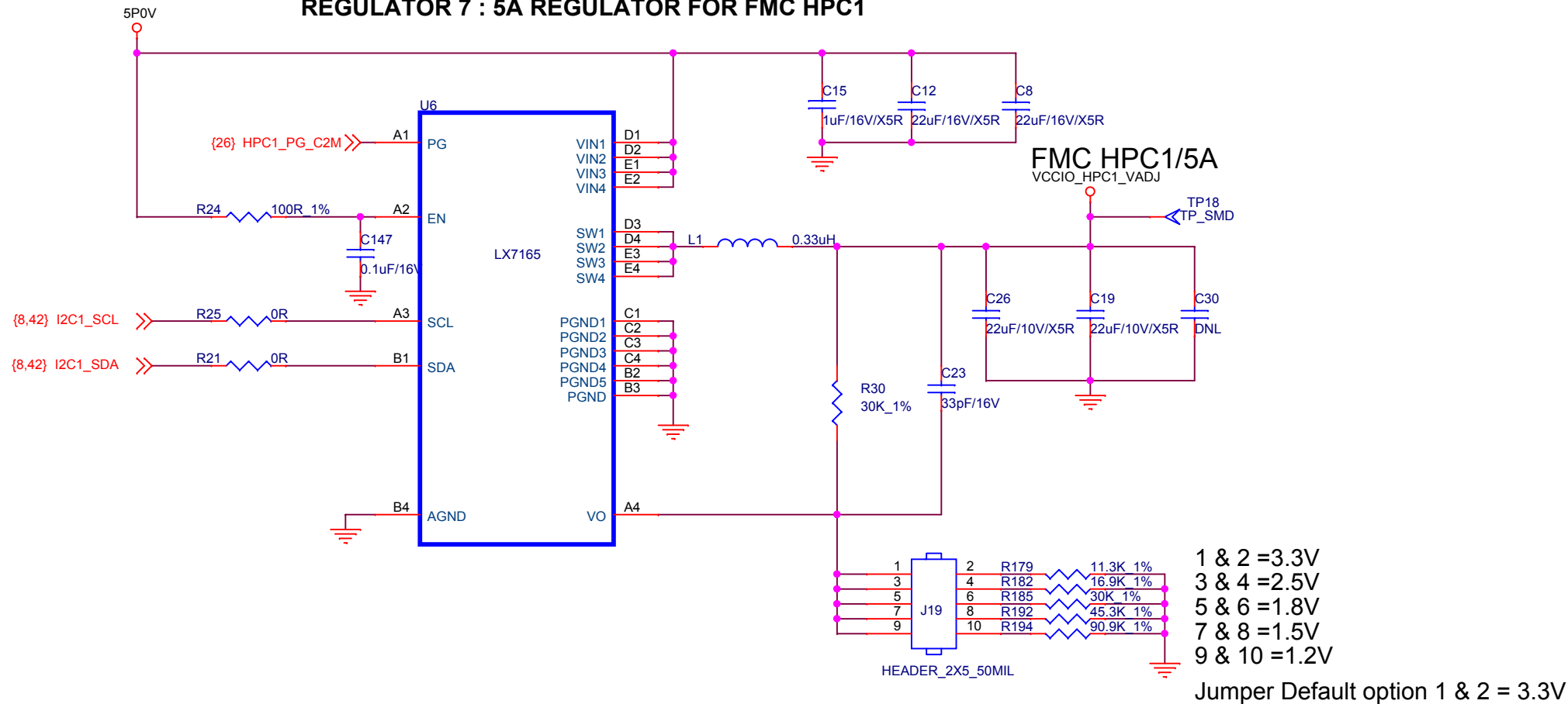
REGULATOR 6: 0.75V FOR FDDR-1 -VTT SUPPLY



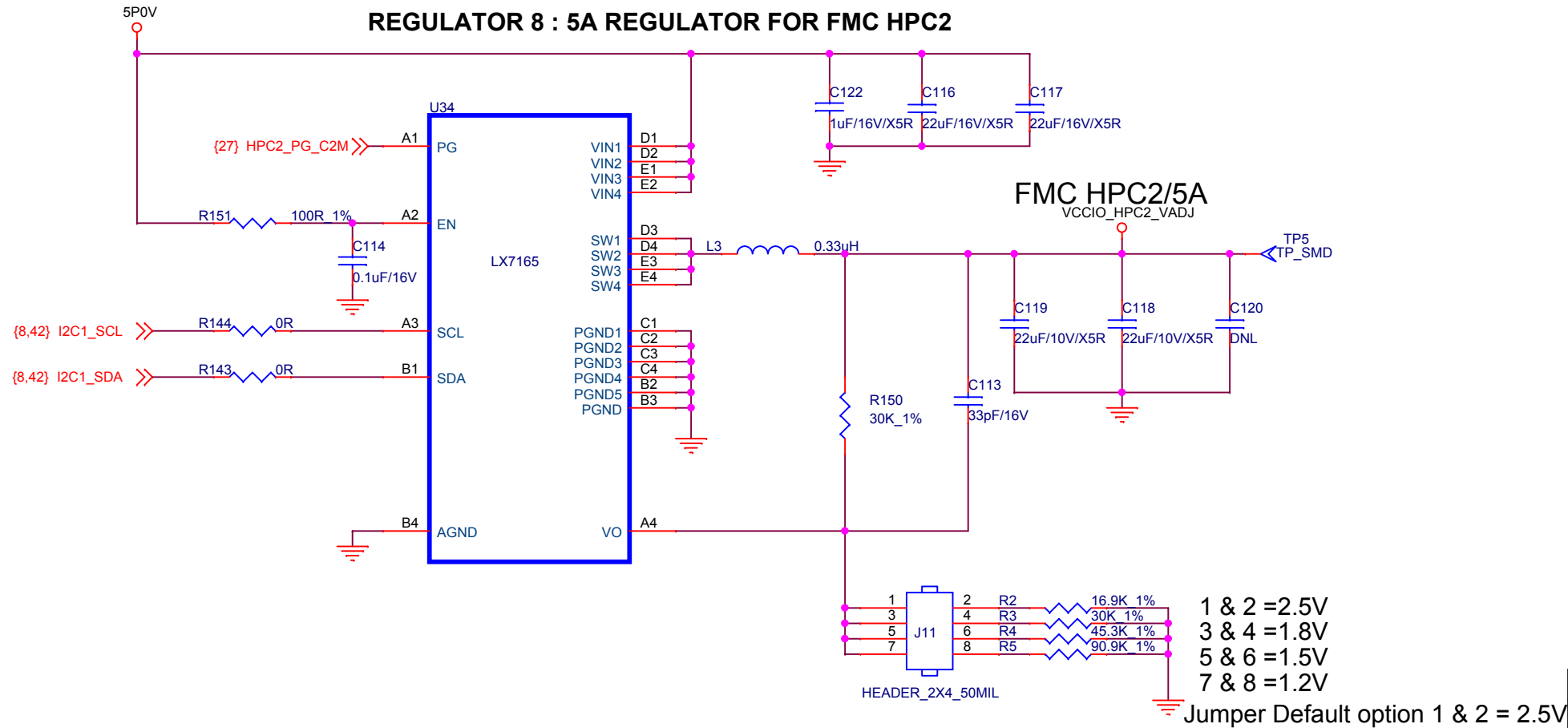
TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE:	Tuesday, March 22, 2016	SH 41 OF 45

POWER SUPPLIES - 4

REGULATOR 7 : 5A REGULATOR FOR FMC HPC1



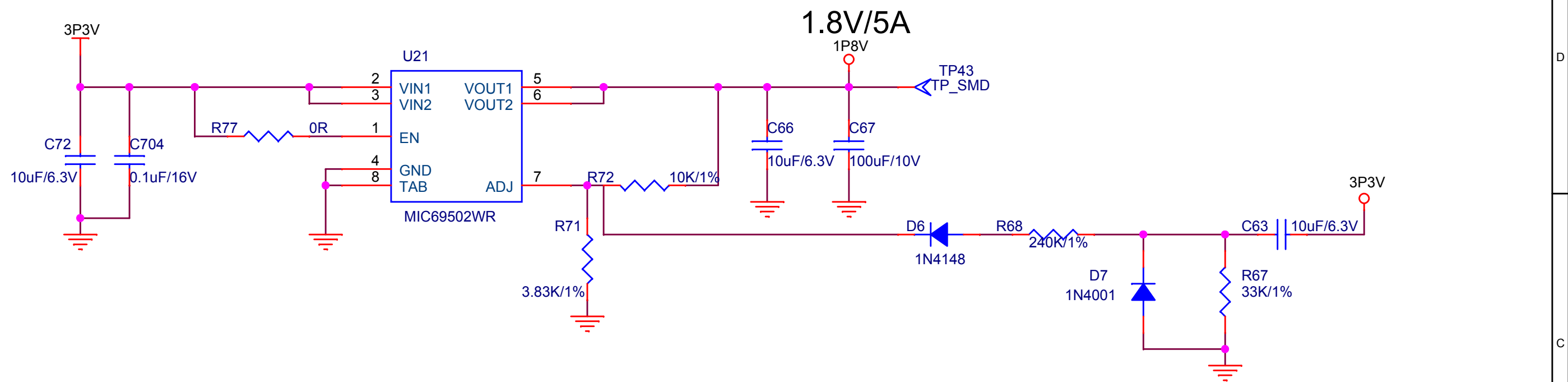
REGULATOR 8 : 5A REGULATOR FOR FMC HPC2



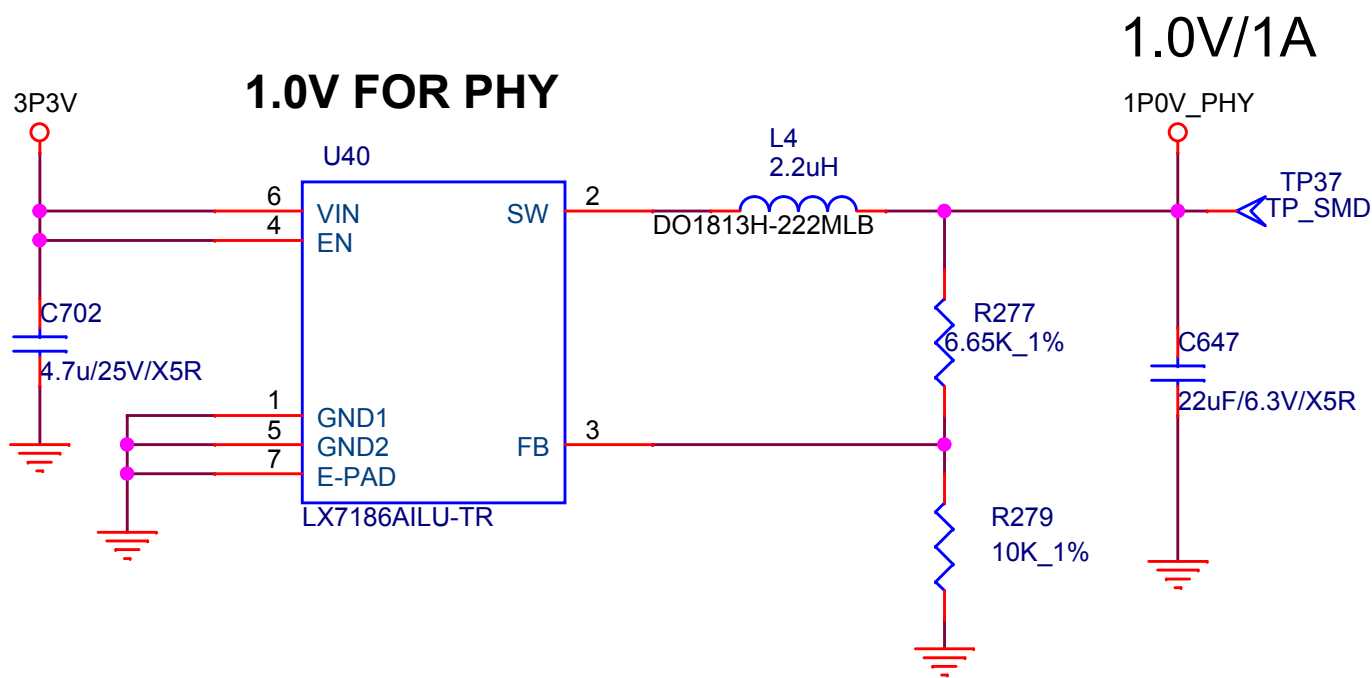
TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE: Tuesday, March 22, 2016		SH 42 OF 45

# POWER SUPPLIES - 5

REGULATOR 9: 1.8V/5A FOR 88E1340 ANLALOG CORE/USB



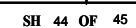
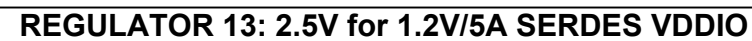
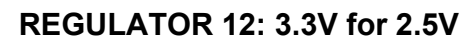
REGULATOR 10: 1V/1A\_FOR PHY 88E1340



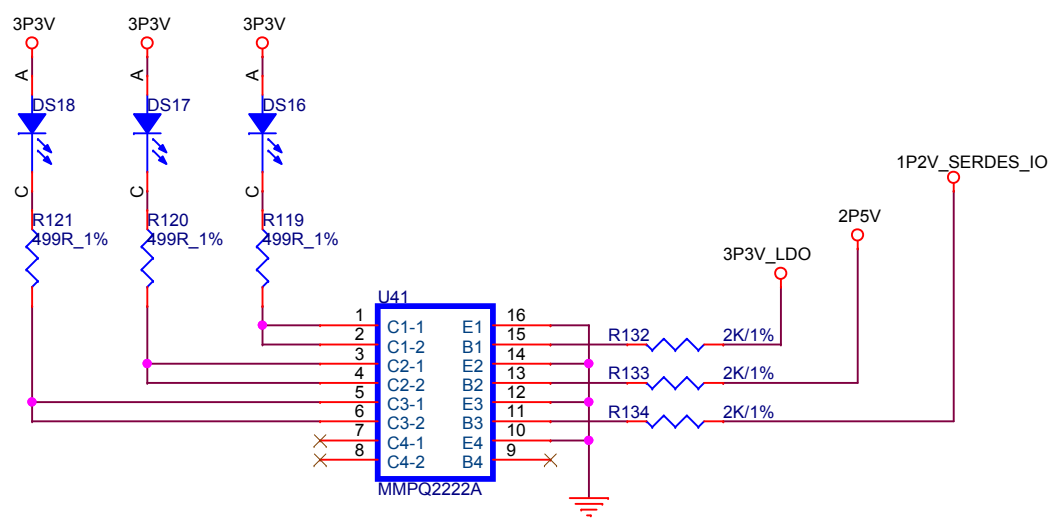
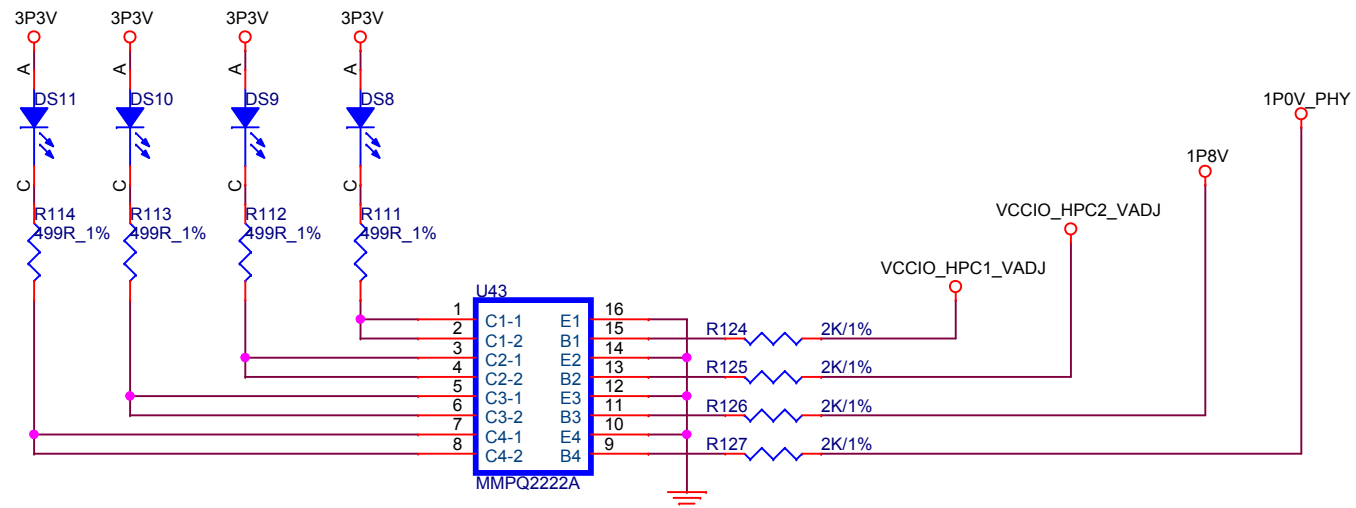
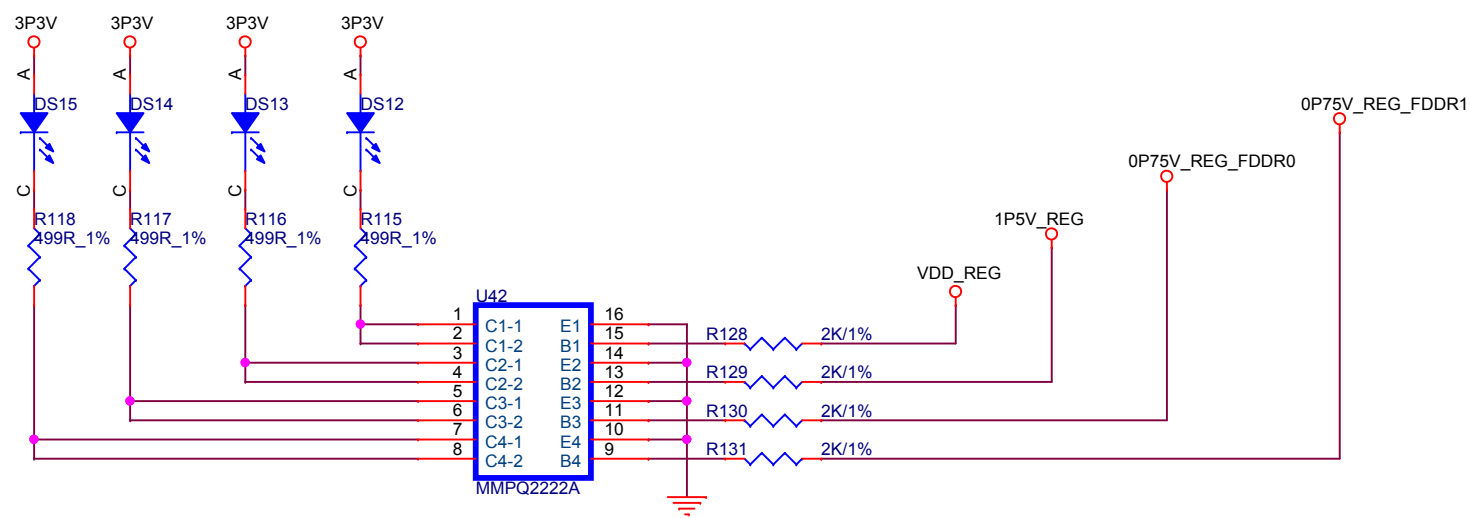
TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
A		B1
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### REGULATOR 11 : 3.3V/1A FOR PLL & VPP



# POWER LEDs



TITLE		
RTG4_DEV_KIT		
Microsemi		
SIZE	DOCUMENT NO.	REV
Custom		B1
DATE:	Tuesday, March 22, 2016	SH 45 OF 45