Total Ionizing Dose Test Report

No. 18T-RTAX4000S-CQ352-DCRNK1

January 10, 2019

Table of Contents

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November 7, 2018

I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 7 days. Every DUT passes the major specifications listed in the table for 300 krad (SiO2) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 300 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or VCCI through a 4.7 kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Part Number	**RTAX4000S**
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	DCRNK1
Quantity Tested	6
Serial Number	300 krad: 7180, 7193 200 krad: 7176, 7179 100 krad: 7168, 7171
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

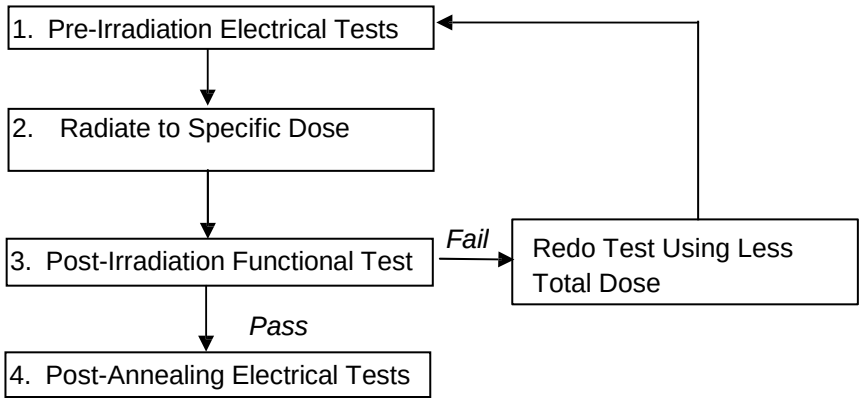


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (RTAX4000S_CQ352_MASTER) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-D Devices

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The delay measurements are taken for both rising and falling edges, the average reading of the two measurements is reported. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-7 show the influx ICCA and ICCI versus total dose for the DUTs.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
7168	100 krad	4.5	4.7	4.1	8.5	11.1	9.4
7171	100 krad	4.6	5.8	5.1	8.4	10.2	9.1
7176	200 krad	9.5	10.6	8.4	8.6	78.5	22.3
7179	200 krad	10.7	18.0	9.5	8.6	77.9	20.1
7180	300 krad	12.2	146	25.3	8.6	130	44.8
7193	300 krad	12.3	86.3	12.9	8.4	164	53.0

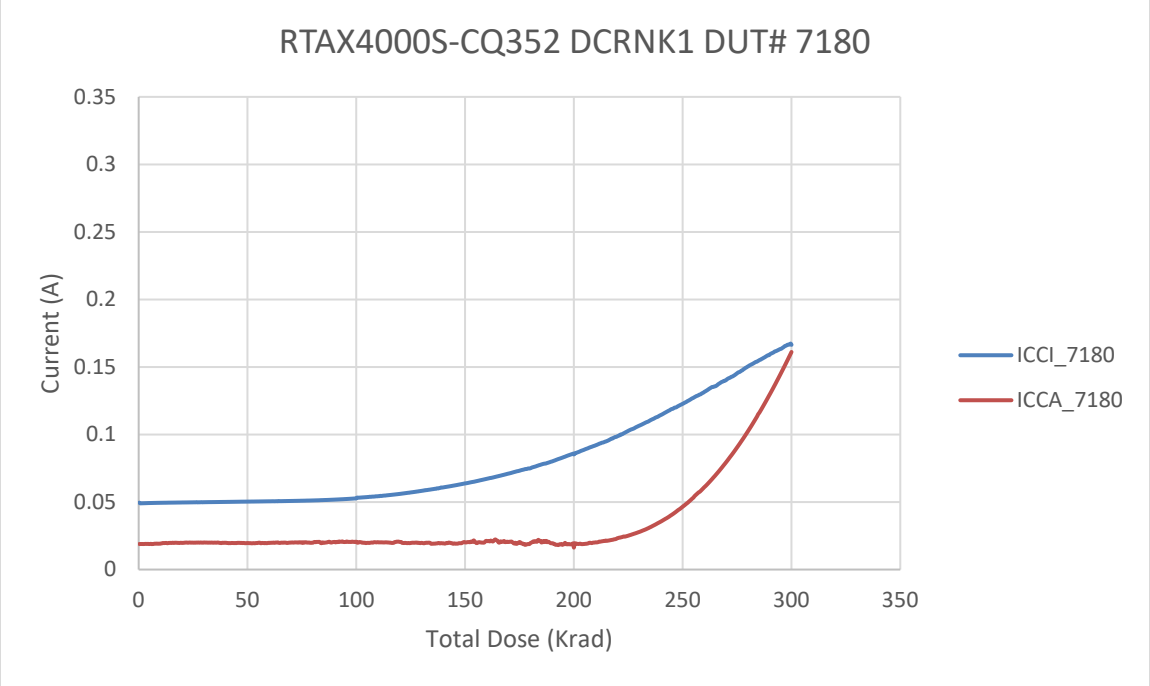


Figure 2 DUT 7180 Influx ICCI and ICCA

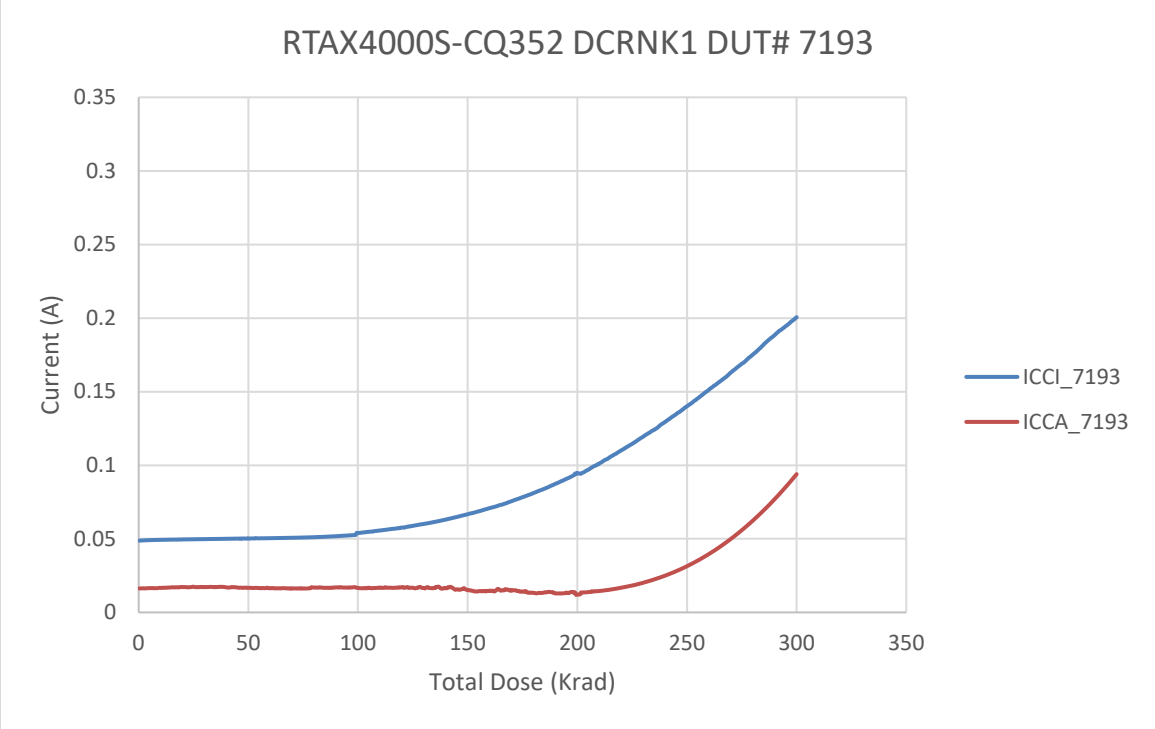


Figure 3 DUT 7193 Influx ICCI and ICCA

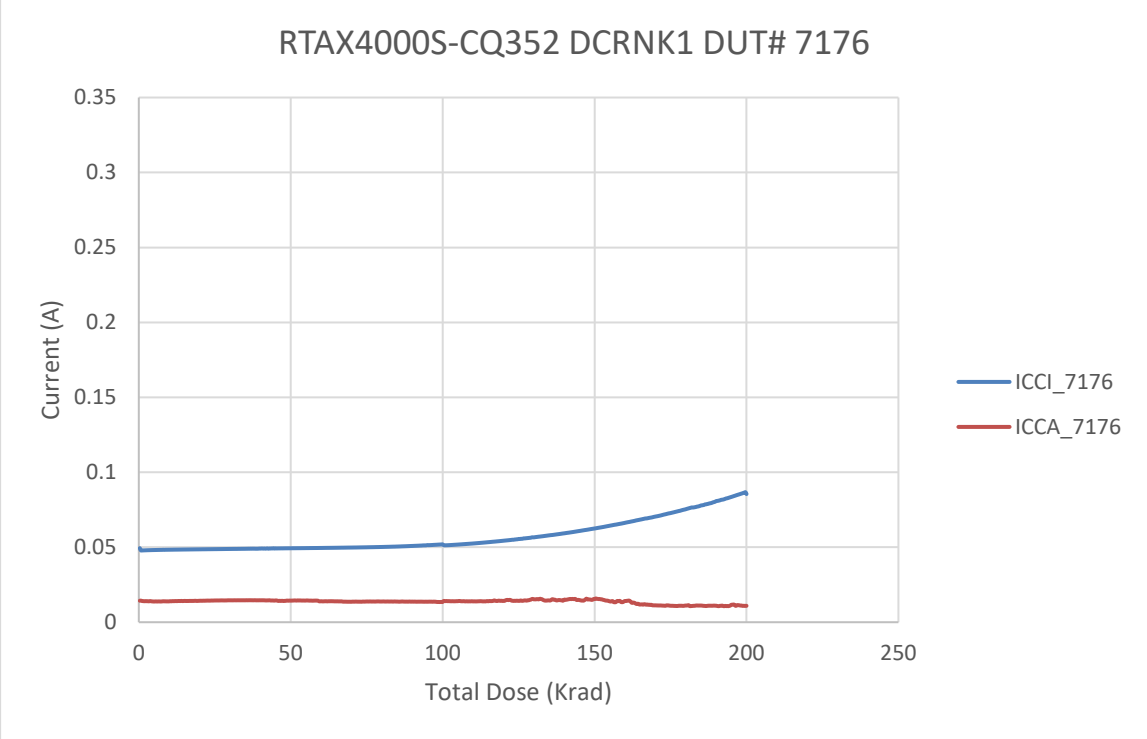


Figure 4 DUT 7176 Influx ICCI and ICCA

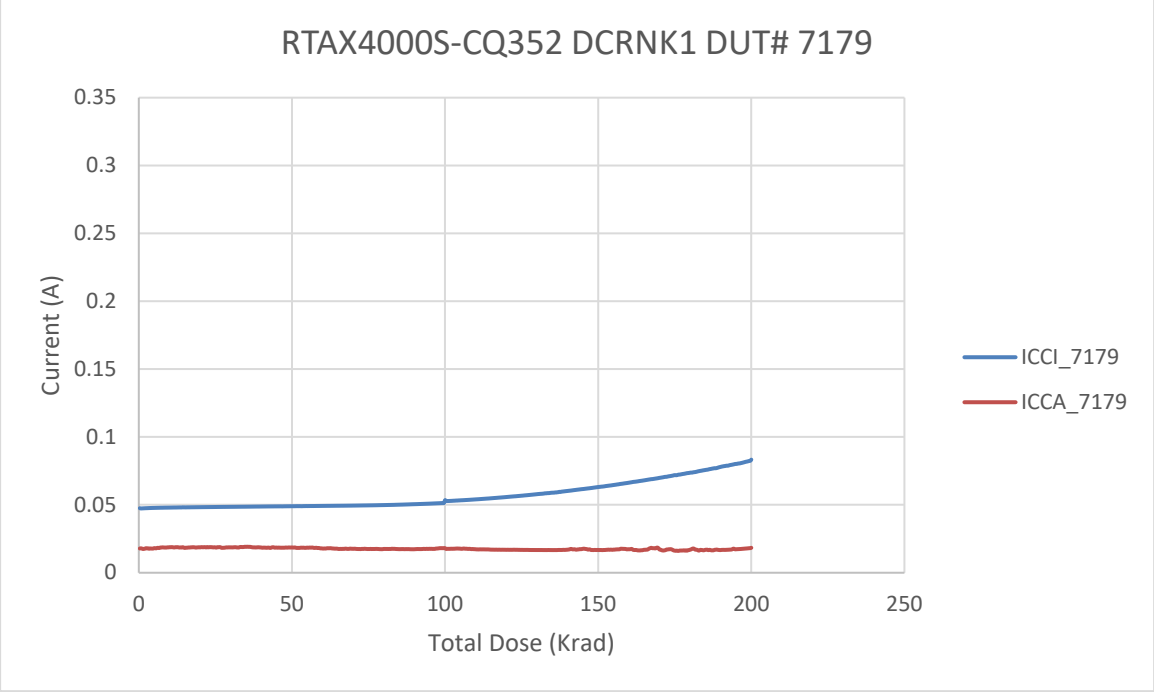


Figure 5 DUT 7179 Influx ICCI and ICCA

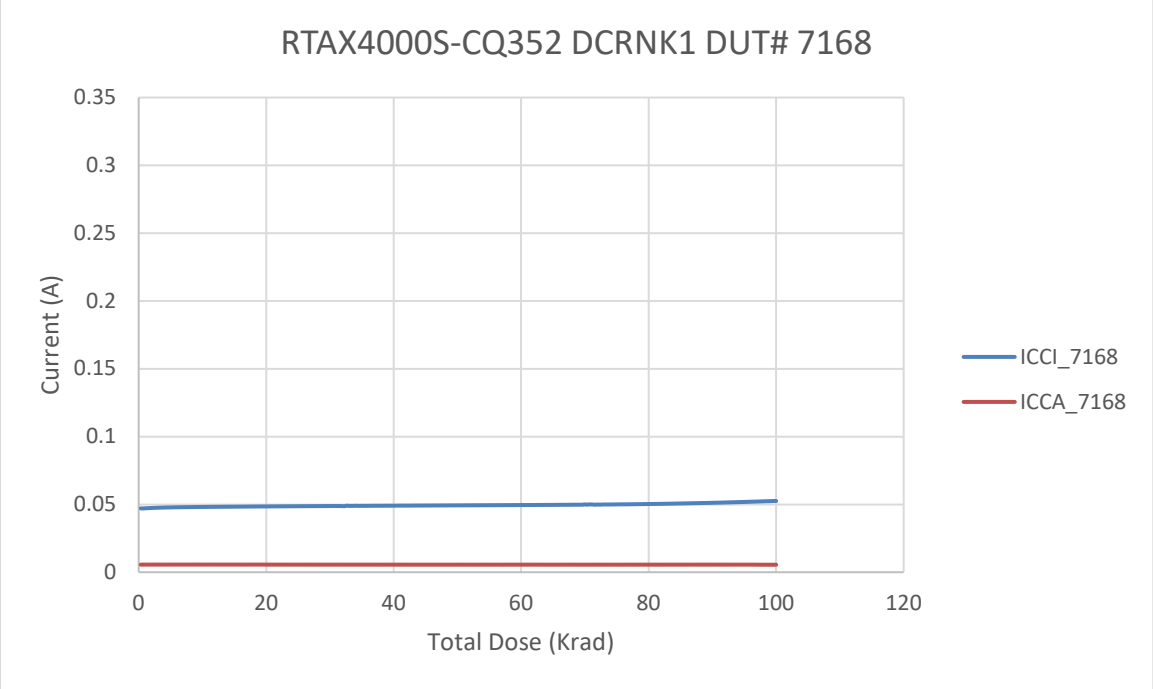


Figure 6 DUT 7168 Influx ICCI and ICCA

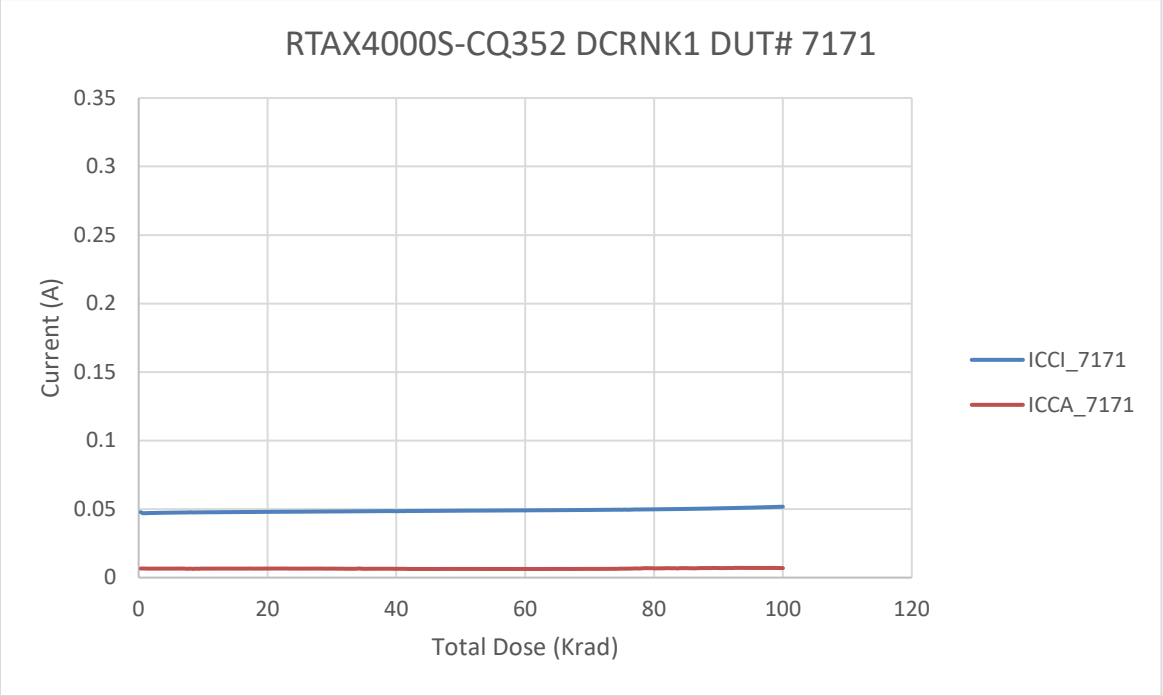


Figure 7 DUT 7171 Influx ICCI and ICCA

C. Single-Ended 3.3 V LVTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design often just input and output buffers starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-annealing data is usually negligibly small. The pre-irradiation and post-annealing single-ended VIL and VIH are tested and recorded as pass or fail. In each case, the pre-irradiation and post-annealing both passed with respect to the specification.

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	7180 (300 krad)		7193 (300 krad)		7176 (200 krad)		7179 (200 krad)		7168 (100 krad)		7171 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	156.6	133.9	159.6	134.6	159.5	141.2	157.6	139.3	164.7	143.9	164.7	146.6
Array_out_EAQ_1	180.0	171.6	183.5	179.4	182.7	188.7	180.1	184.9	184.1	191.7	185.5	191.3
Array_out_EAQ_2	209.1	172.6	210.8	182.8	212.7	180.5	207.5	180.7	213.7	191.0	215.2	191.7
Global_Monitor_EAQ	176.6	168.9	179.4	171.0	178.8	175.9	176.5	174.6	181.3	180.1	183.4	181.4
Shiftout3	184.8	179.9	183.9	179.0	185.1	180.0	186.2	181.0	187.8	183.5	187.7	183.9
Shiftout7	191.9	208.2	190.8	206.5	192.1	186.9	192.7	187.6	194.6	190.3	194	190.5
Shiftout8	199.8	186.2	199.9	187.6	201.4	217.2	199.6	214.2	200.8	212.7	200.2	210.5
RAM_Monitor_EAQ	181.8	181.4	184.7	183.1	184.5	179.7	181.7	177.5	187.6	183.5	189	184.5
RAM_out_EAQ_0	187.9	201.3	189.0	199.4	189.4	183.8	188.0	185.9	189.6	185.1	193.1	188.2
RAM_out_EAQ_4	149.3	145.3	148.5	144.3	150.2	146.4	148.9	144.3	150.4	146.9	149.8	146.7
RAM_out_EAQ_8	182.1	192.8	185.3	185.8	184.8	217.8	183.0	211.5	185.8	223.9	189.7	219.2

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	7180 (300 krad)		7193 (300 krad)		7176 (200 krad)		7179 (200 krad)		7168 (100 krad)		7171 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.753	2.795	2.752	2.766	2.751	2.761	2.754	2.764	2.750	2.762	2.750	2.763
Array_out_EAQ_1	2.728	2.731	2.728	2.720	2.727	2.713	2.730	2.717	2.725	2.713	2.727	2.717
Array_out_EAQ_2	2.708	2.755	2.700	2.727	2.700	2.722	2.702	2.722	2.696	2.714	2.699	2.718
Global_Monitor_EAQ	2.732	2.731	2.733	2.731	2.730	2.725	2.734	2.728	2.726	2.723	2.729	2.725
Shiftout3	2.722	2.717	2.725	2.720	2.723	2.720	2.722	2.719	2.721	2.720	2.722	2.721
Shiftout7	2.714	2.689	2.718	2.692	2.716	2.712	2.716	2.712	2.713	2.713	2.715	2.714
Shiftout8	2.703	2.704	2.706	2.698	2.704	2.681	2.706	2.684	2.704	2.689	2.707	2.693
RAM_Monitor_EAQ	2.728	2.720	2.727	2.719	2.724	2.721	2.729	2.725	2.72	2.720	2.723	2.721
RAM_out_EAQ_0	2.721	2.705	2.722	2.703	2.721	2.718	2.720	2.719	2.718	2.718	2.719	2.719
RAM_out_EAQ_4	2.765	2.762	2.768	2.764	2.766	2.763	2.767	2.764	2.765	2.764	2.767	2.766
RAM_out_EAQ_8	2.726	2.720	2.727	2.721	2.725	2.698	2.727	2.700	2.723	2.703	2.724	2.698

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case, the percentage change is well below 10%.

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	7180	300 krad	6.13	6.11	6.14	6.65	6.11
	7193	300 krad	6.20	6.16	6.19	6.52	6.12
	7176	200 krad	6.18	6.16	6.18	-	6.09
	7179	200 krad	6.32	6.29	6.33	-	6.22
	7168	100 krad	6.35	6.32		-	6.29
	7171	100 krad	6.39	6.36		-	6.32
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	7180	300 krad	-	-0.33%	0.08%	8.48%	-0.41%
	7193	300 krad	-	-0.56%	-0.08%	5.17%	-1.21%
	7176	200 krad	-	-0.40%	0.00%	-	-1.54%
	7179	200 krad	-	-0.40%	0.24%	-	-1.50%
	7168	100 krad	-	-0.55%	-	-	-1.02%
	7171	100 krad	-	-0.55%	-	-	-1.10%

F. Transition Time

Figure 8a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

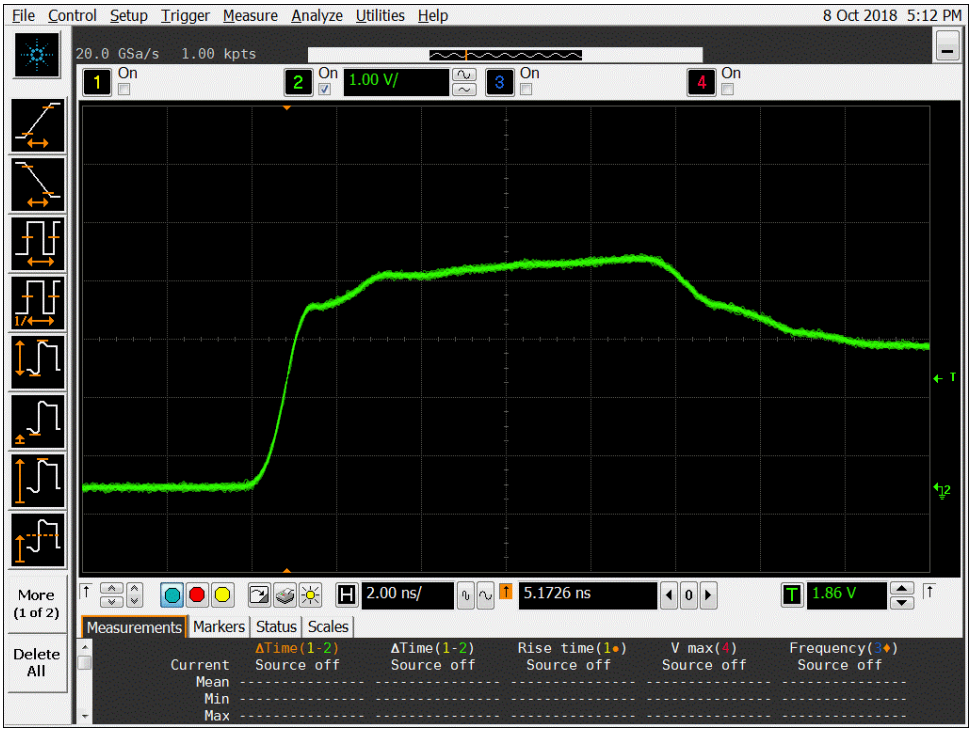


Figure 8a DUT 7180 Pre-Irradiation Rising Edge.

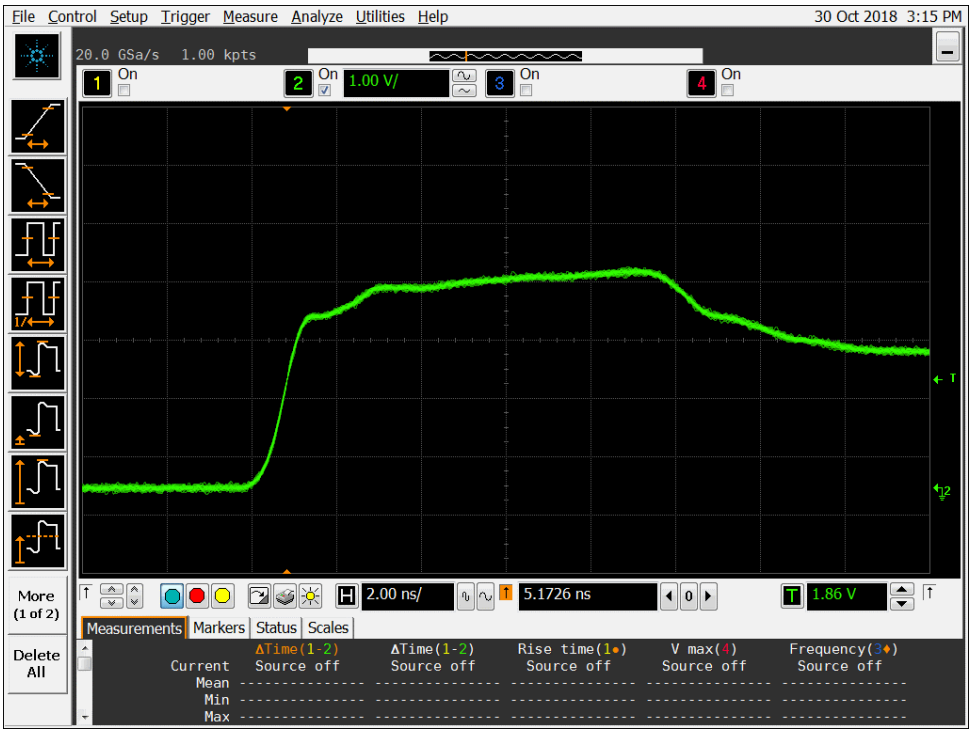


Figure 8b DUT 7180 Post-Annealing Rising Edge.

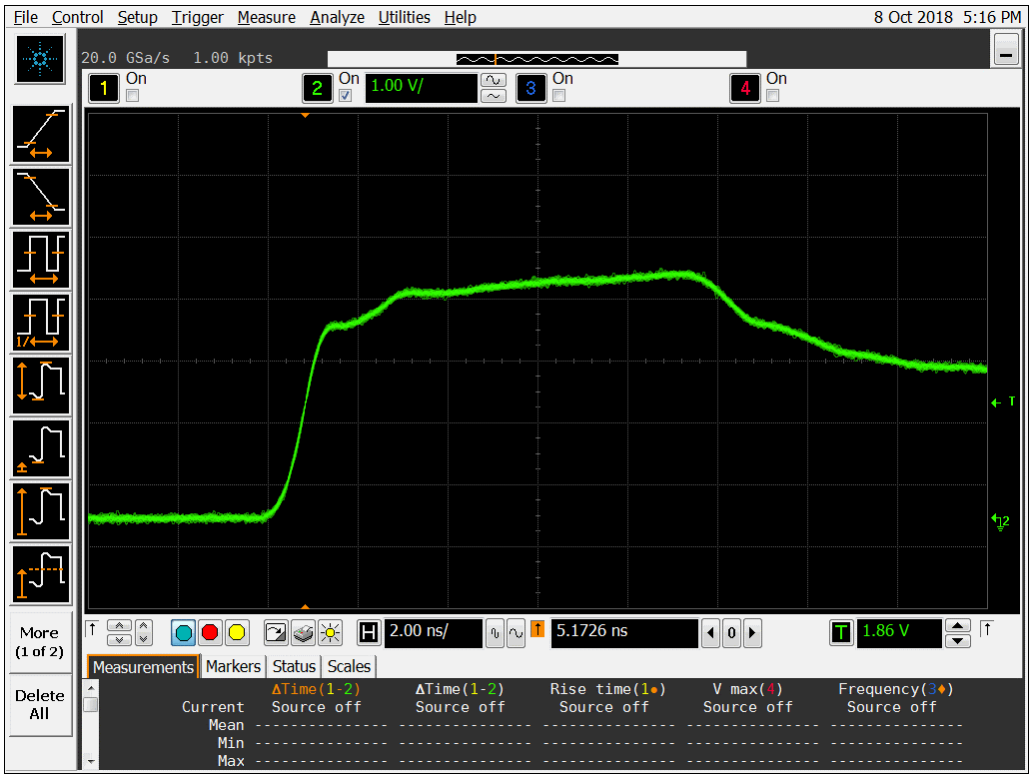


Figure 9a DUT 7193 Pre-irradiation Rising Edge.

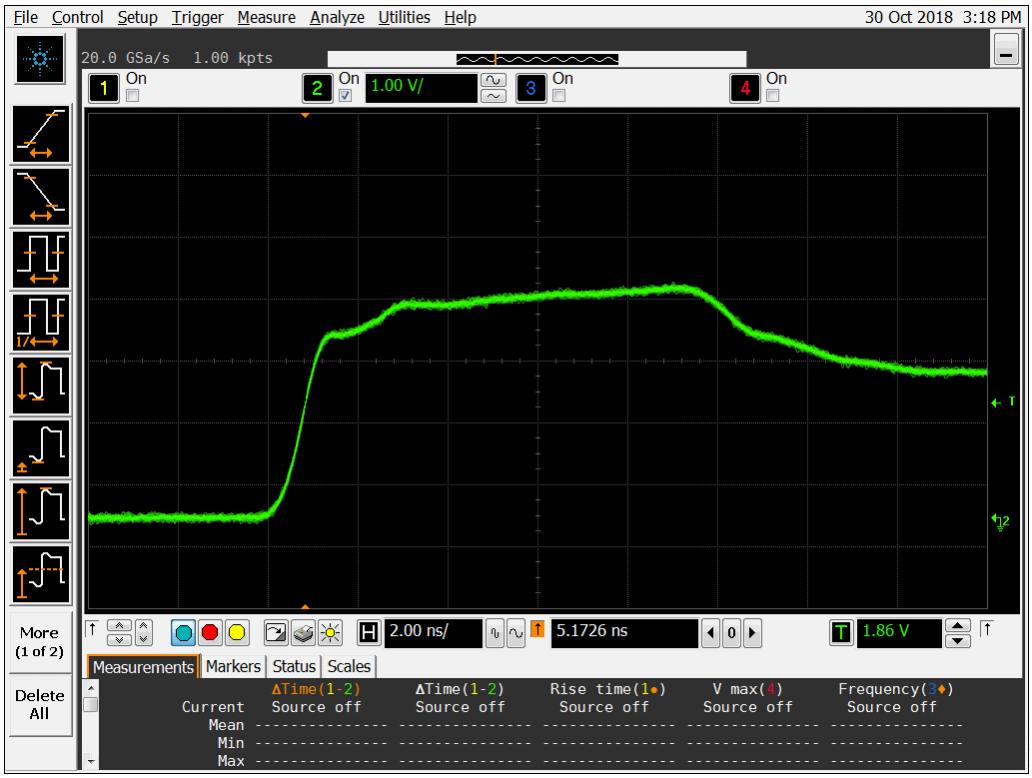


Figure 9b DUT 7193 Post-Annealing Rising Edge.

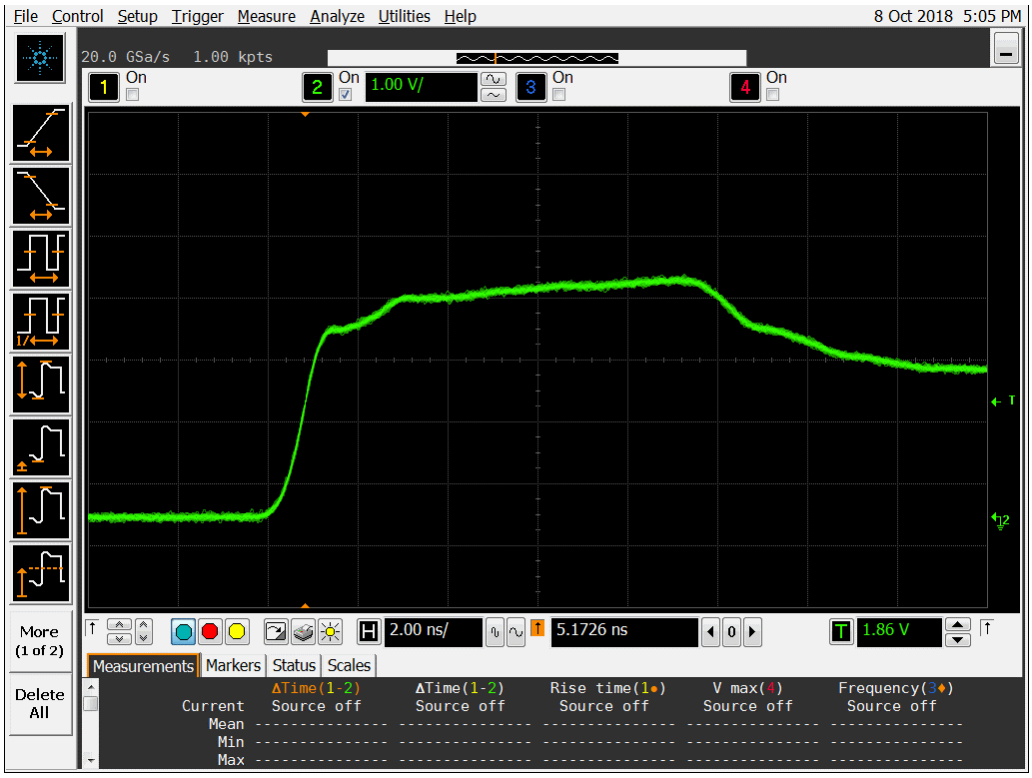


Figure 10a DUT 7176 Pre-Irradiation Rising Edge.

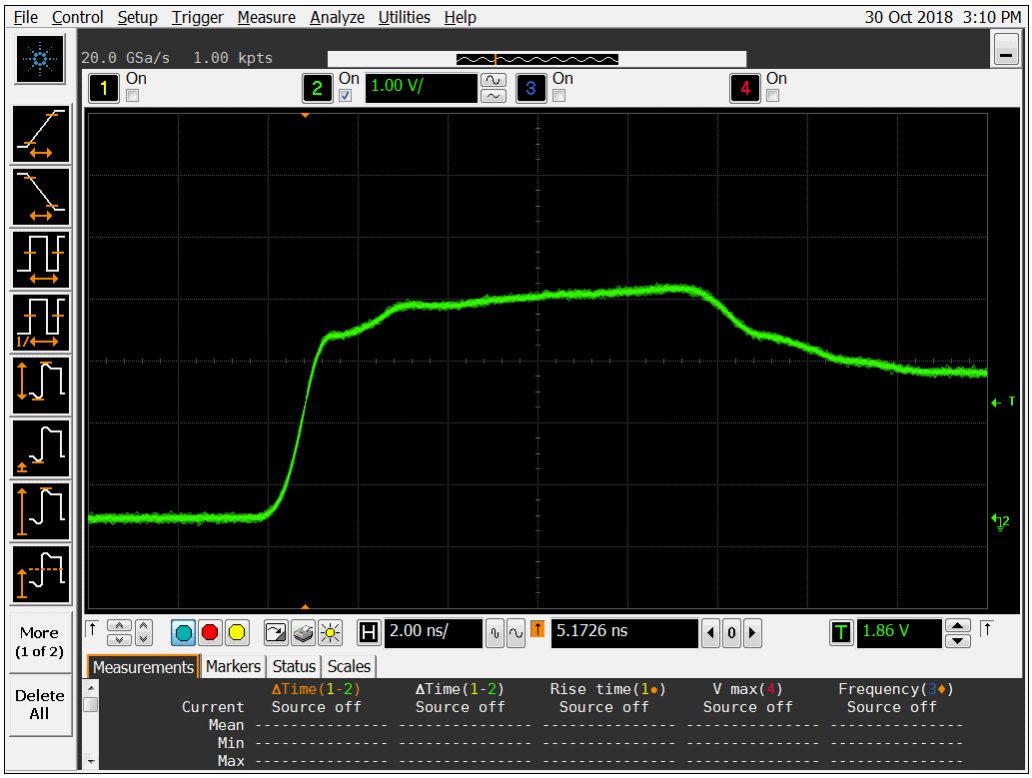


Figure 10b DUT 7176 Post-Annealing Rising Edge.

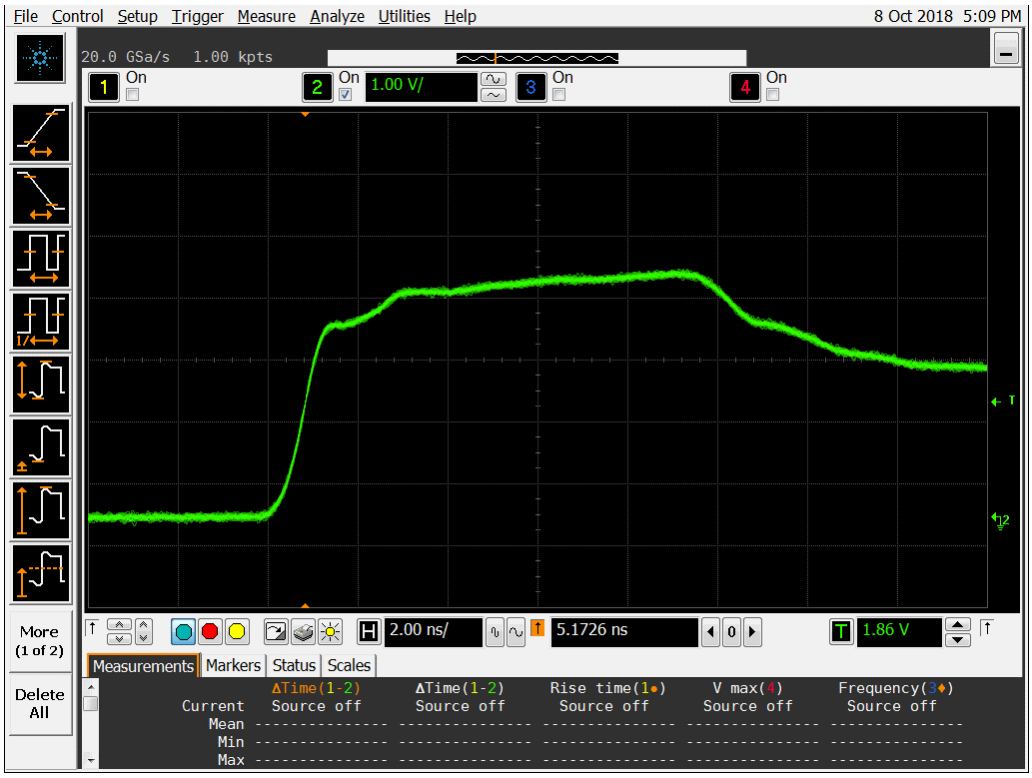


Figure 11a DUT 7179 Pre-Irradiation Rising Edge.

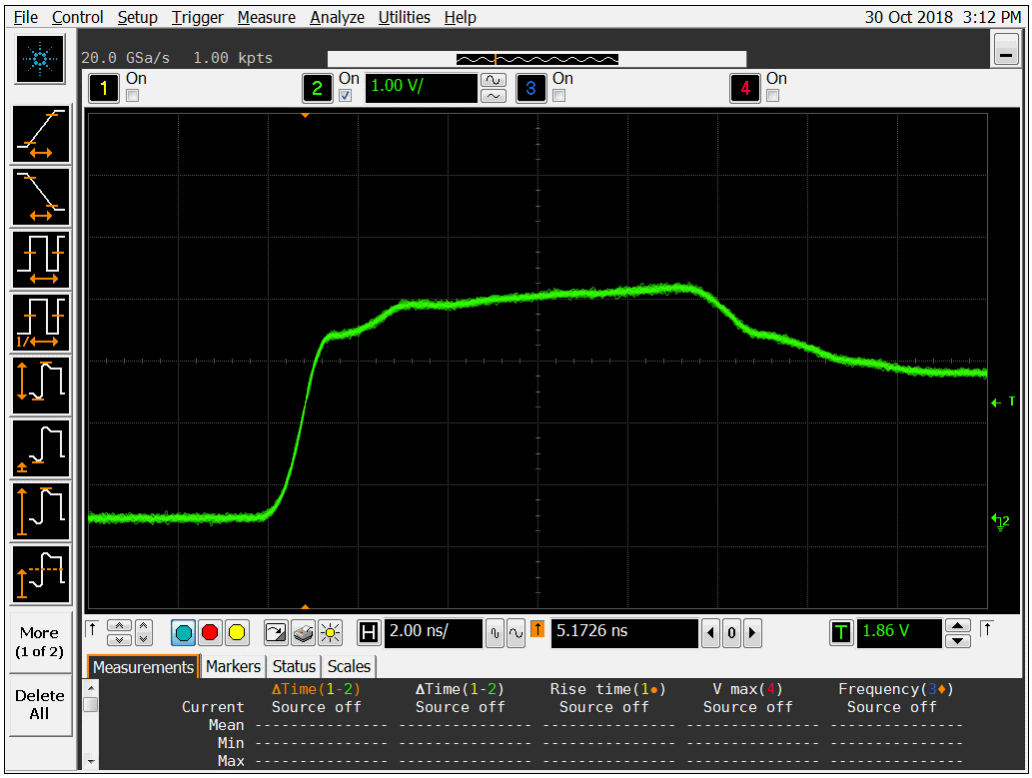


Figure 11b DUT 7179 Post-Annealing Rising Edge.

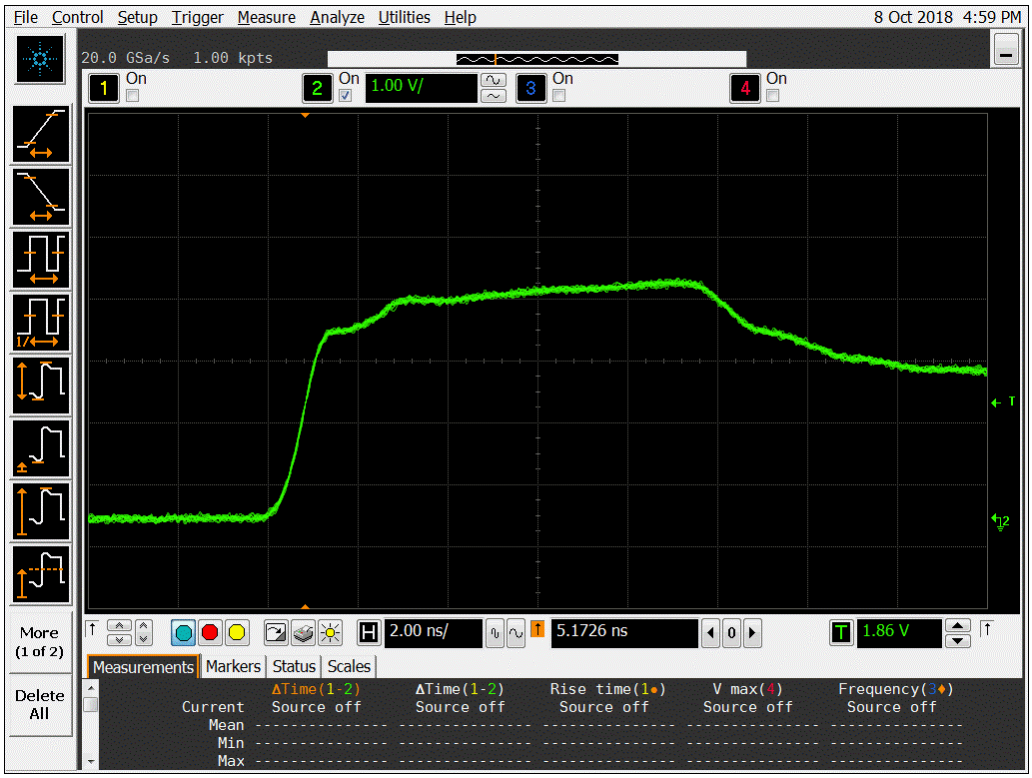


Figure 12a DUT 7168 Pre-Irradiation Rising Edge.

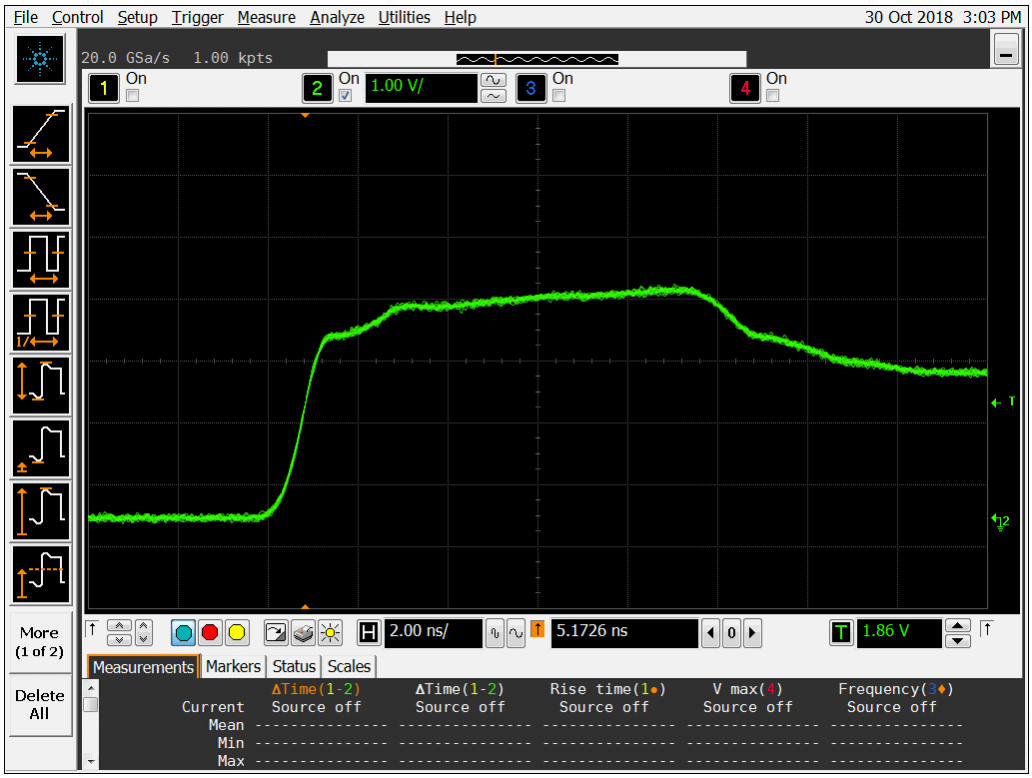


Figure 12b DUT 7168 Post-Annealing Rising Edge.

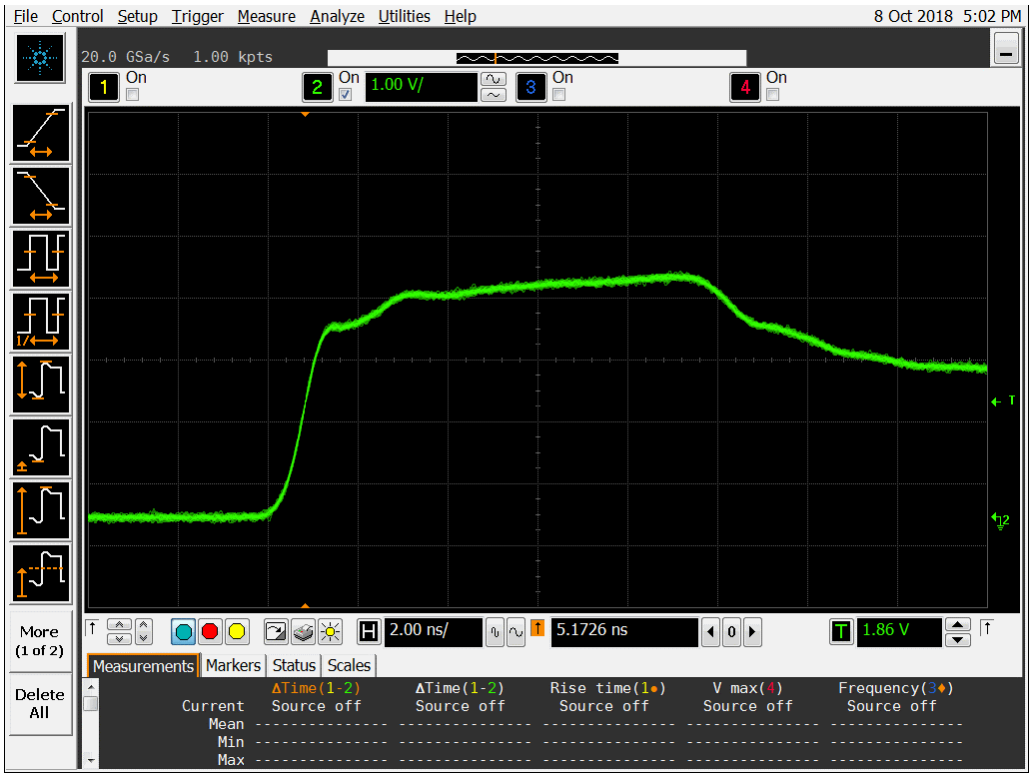


Figure 13a DUT 7171 Pre-Irradiation Rising Edge.

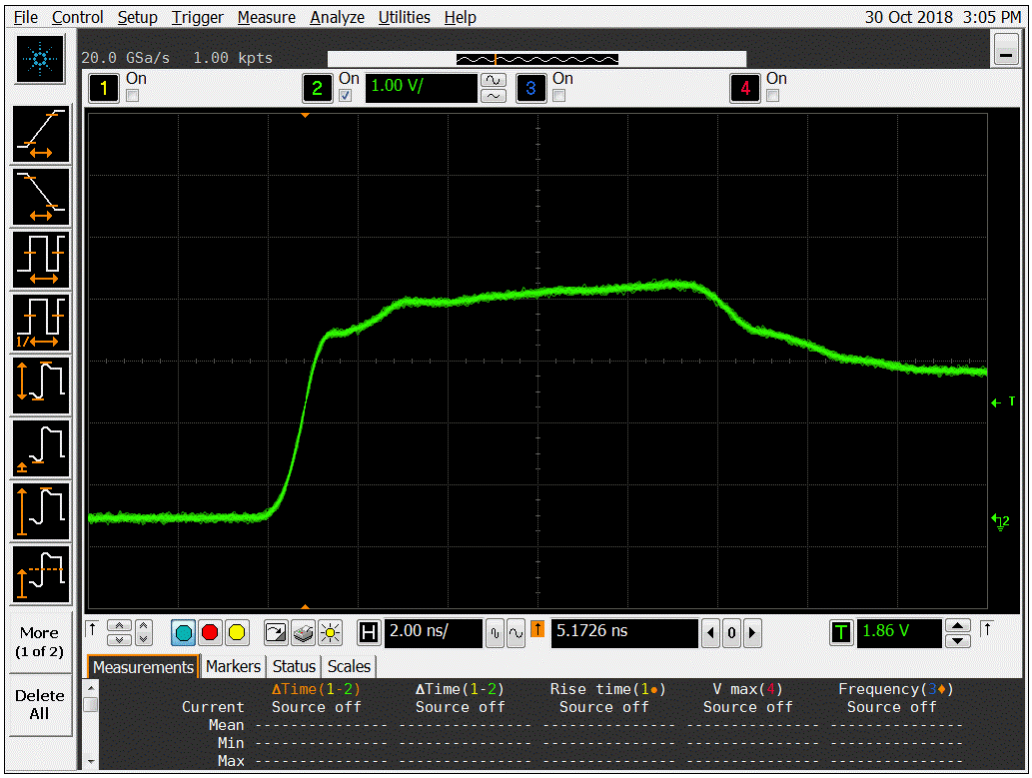


Figure 13b DUT 7171 Post-Annealing Rising Edge.

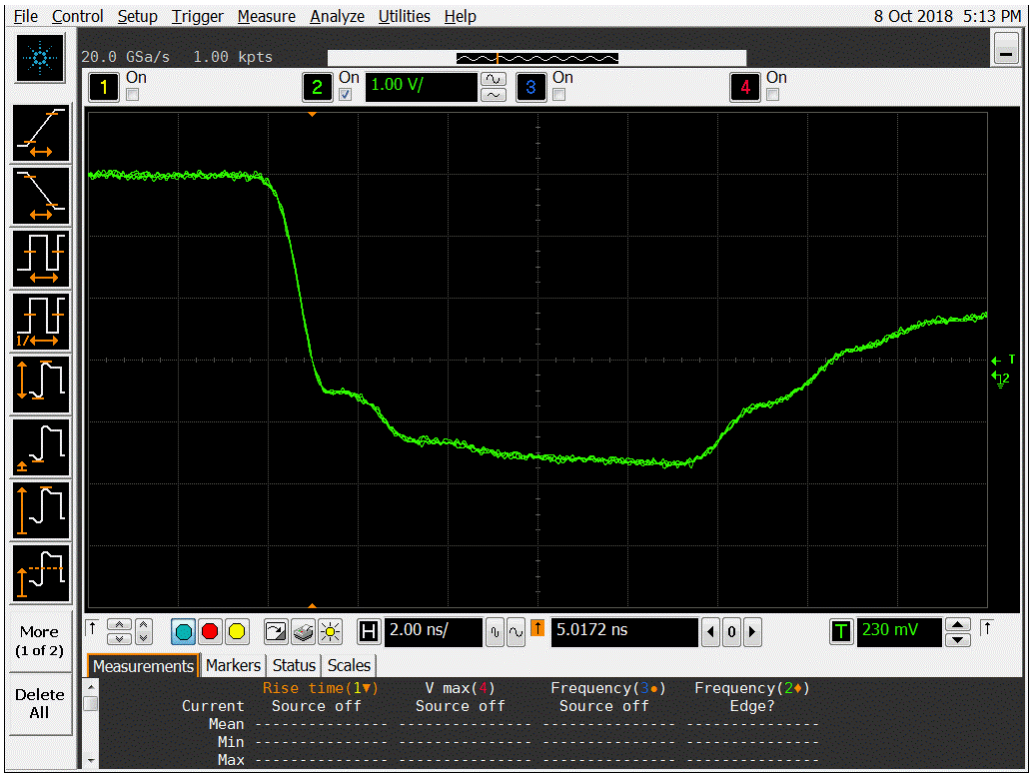


Figure 14a DUT 7180 Pre-Irradiation Falling Edge.

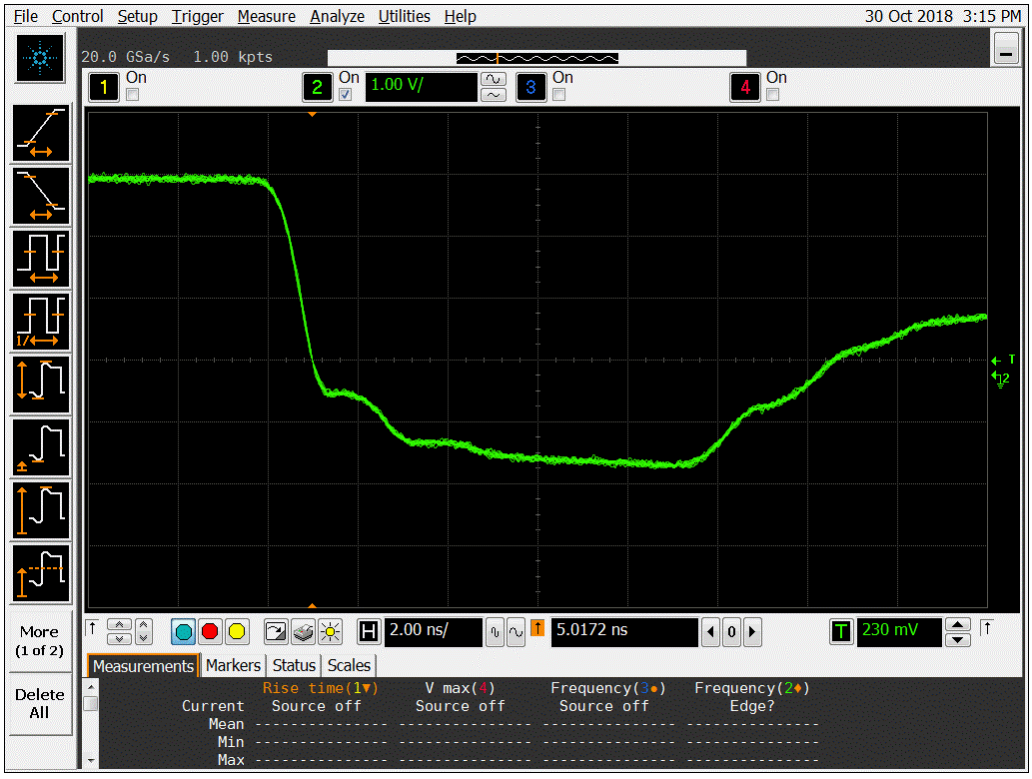


Figure 14b DUT 7180 Post-Annealing Falling Edge.

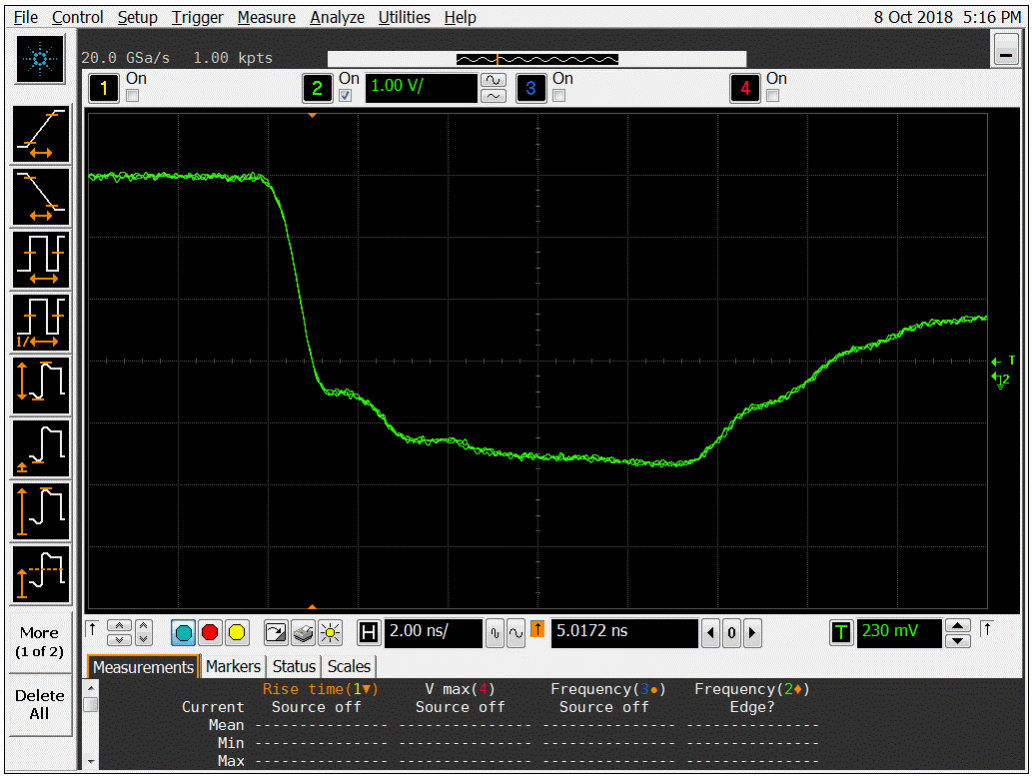


Figure 15a DUT 7193 Pre-Irradiation Falling Edge.

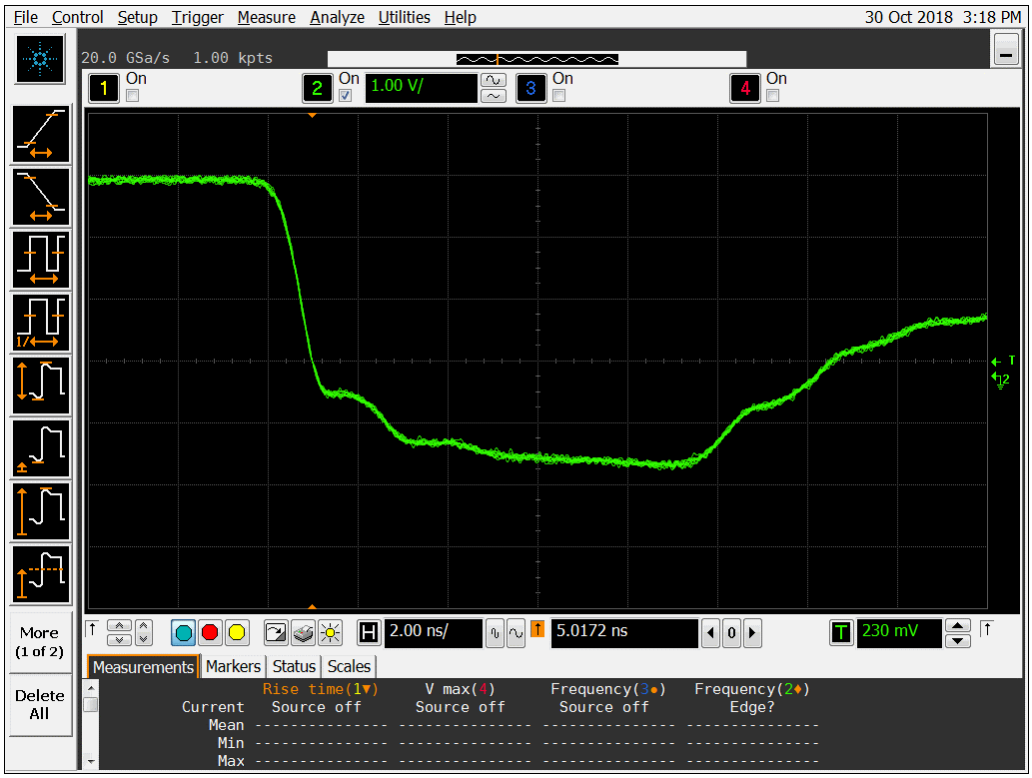


Figure 15b DUT 7193 Post-Annealing Falling Edge.

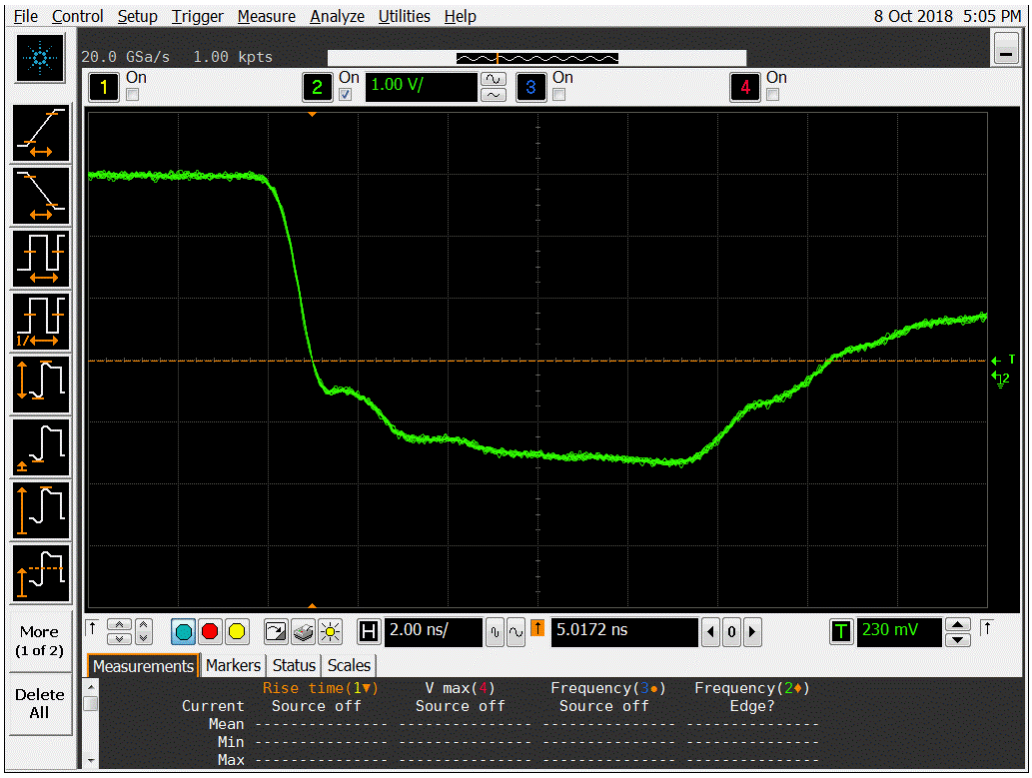


Figure 16a DUT 7176 Pre-Irradiation Falling Edge.

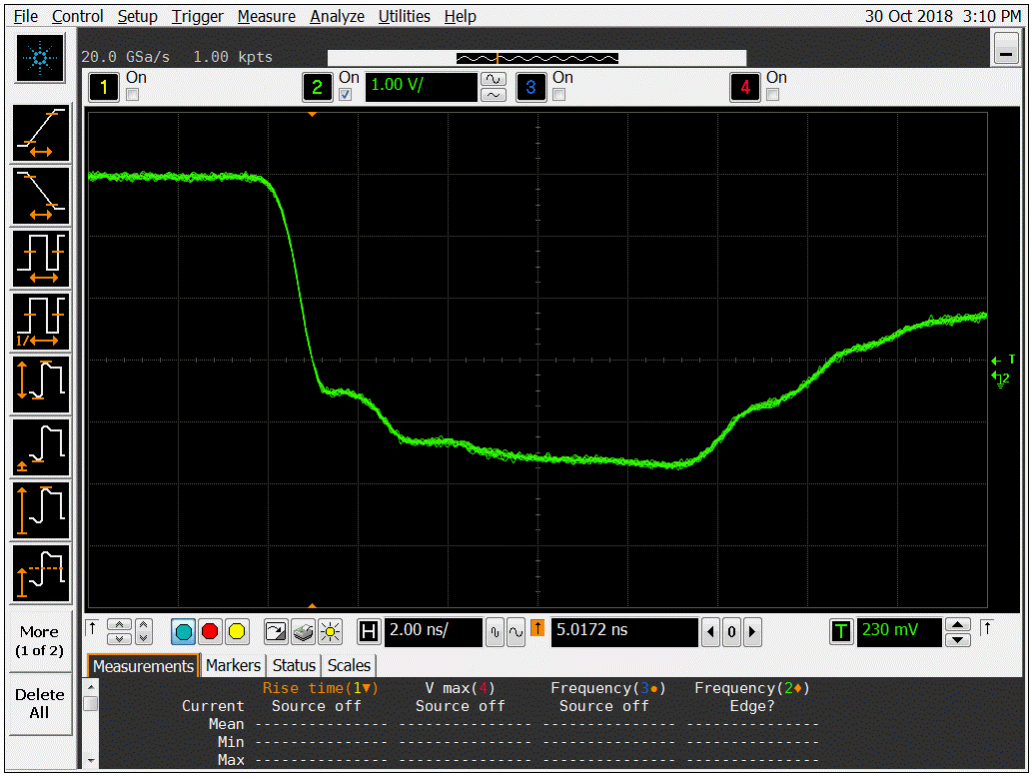


Figure 16b DUT 7176 Post-Annealing Falling Edge.

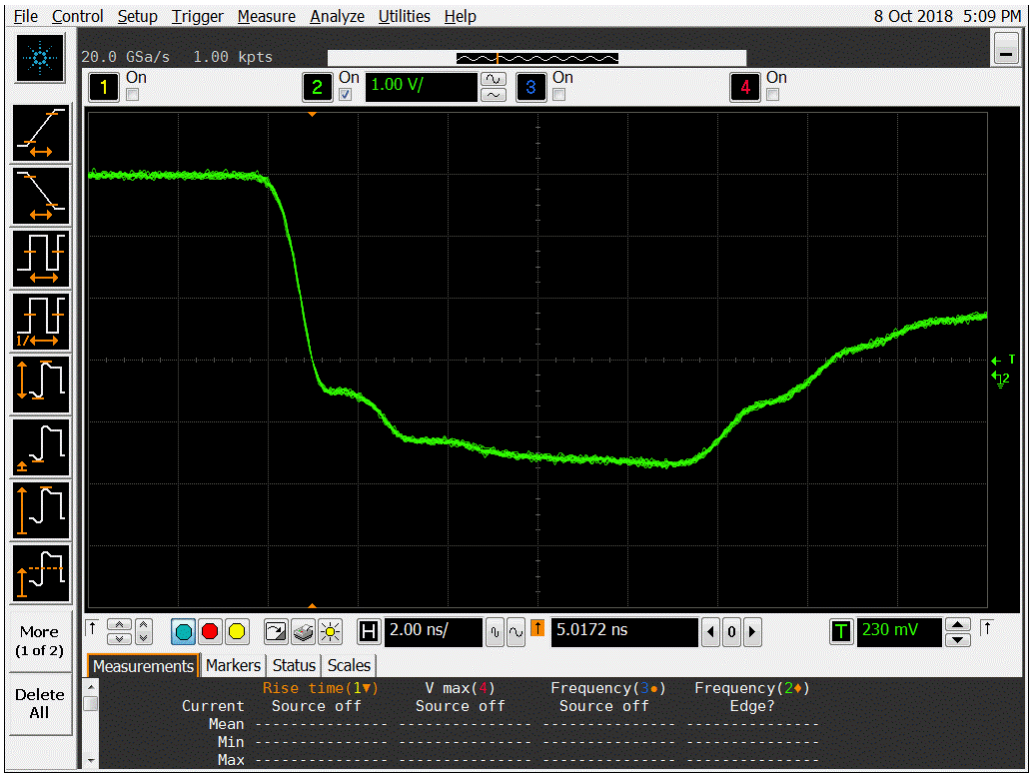


Figure 17a DUT 7179 Pre-Irradiation Falling Edge.

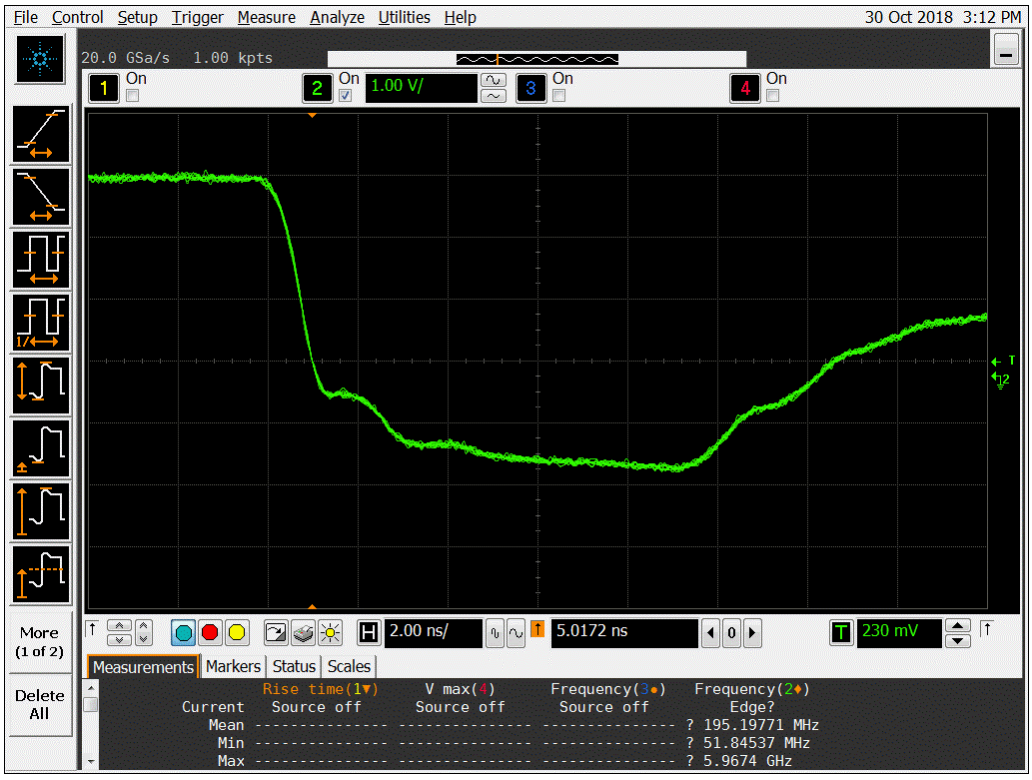


Figure 17b DUT 7179 Post-Annealing Falling Edge.

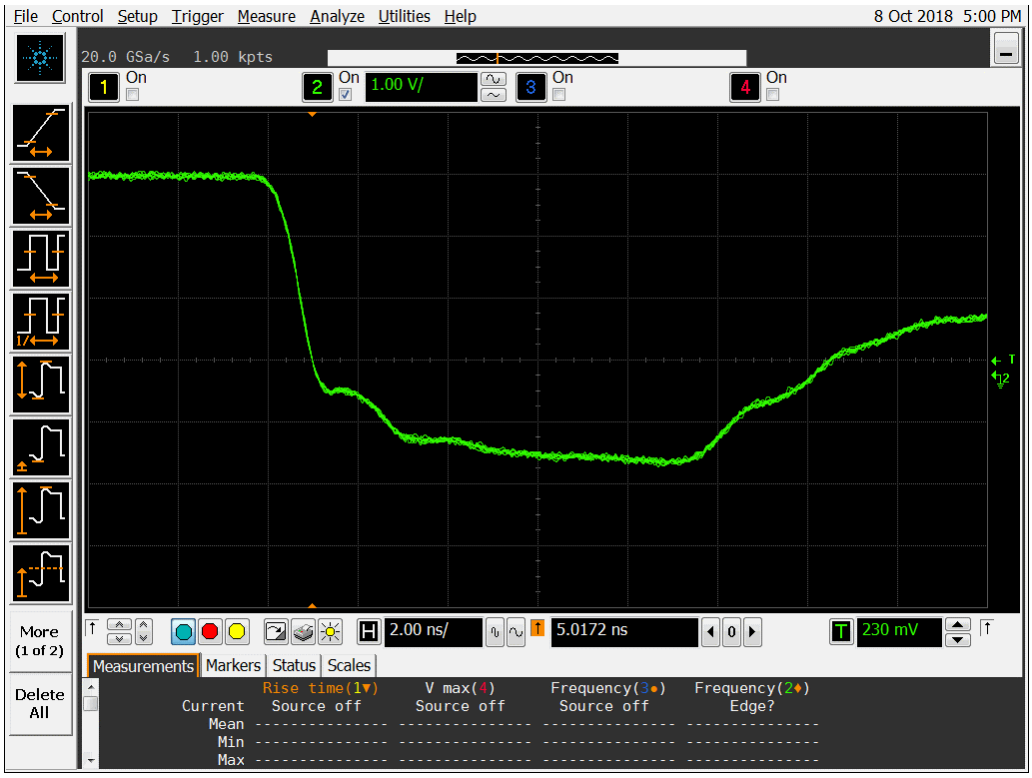


Figure 18a DUT 7168 Pre-Irradiation Falling Edge.

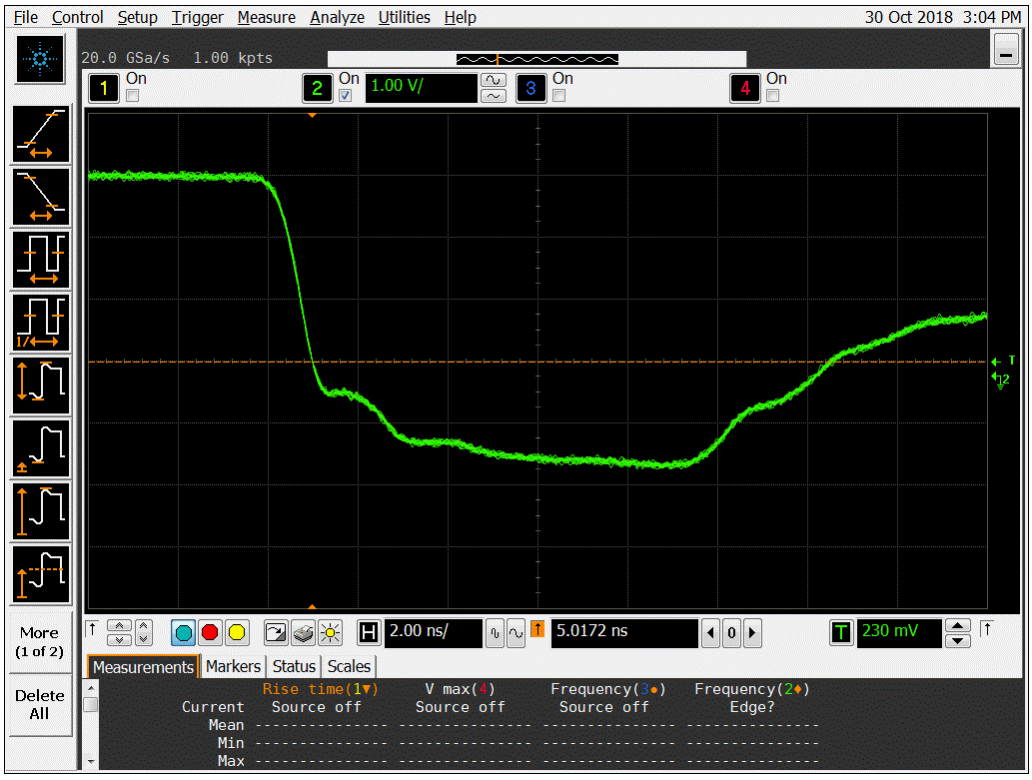


Figure 18b DUT 7168 Post-Annealing Falling Edge.

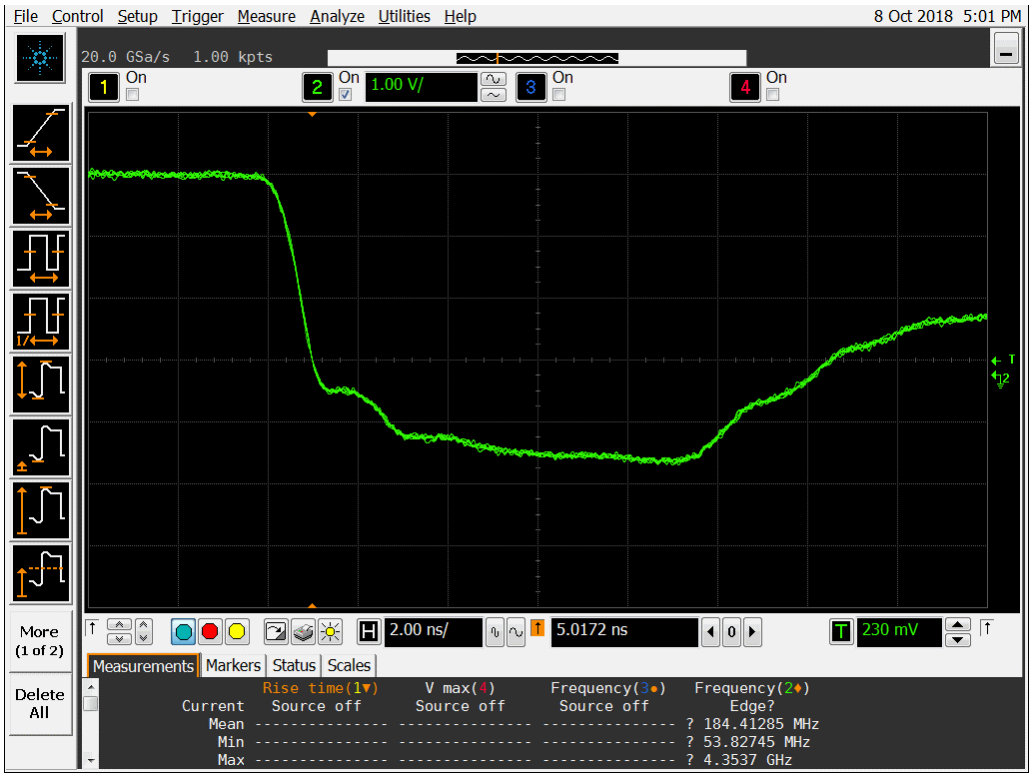


Figure 19a DUT 7171 Pre-Irradiation Falling Edge.

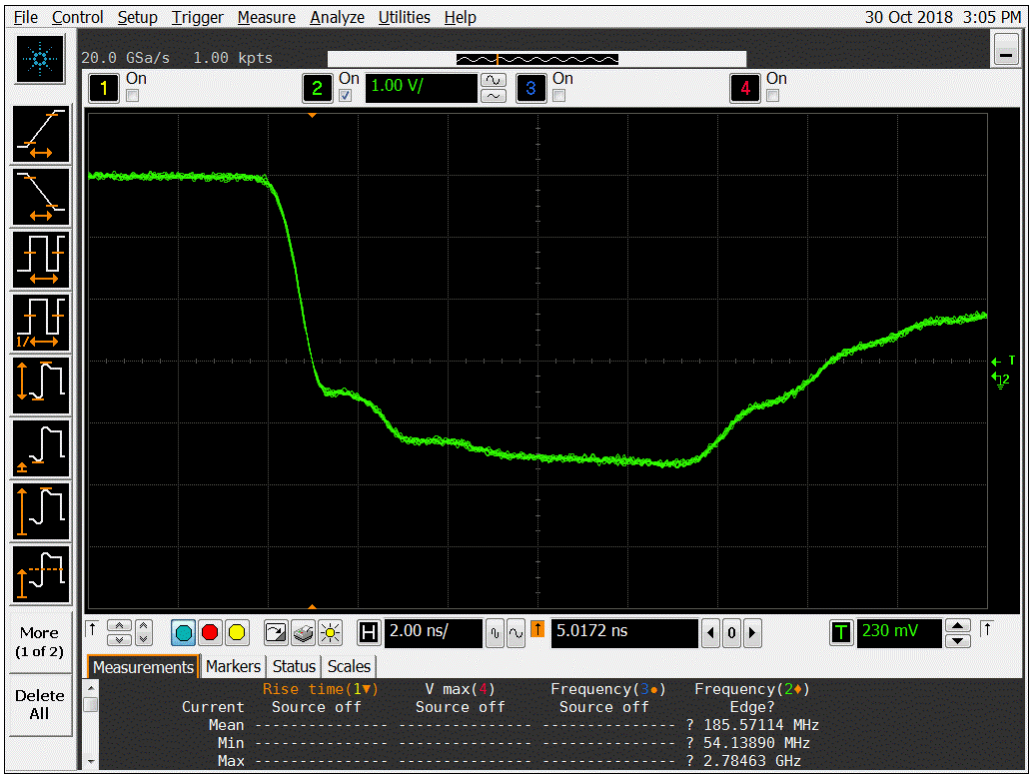


Figure 19b DUT 7171 Post-Annealing Falling Edge.

Appendix A: DUT Bias Diagram

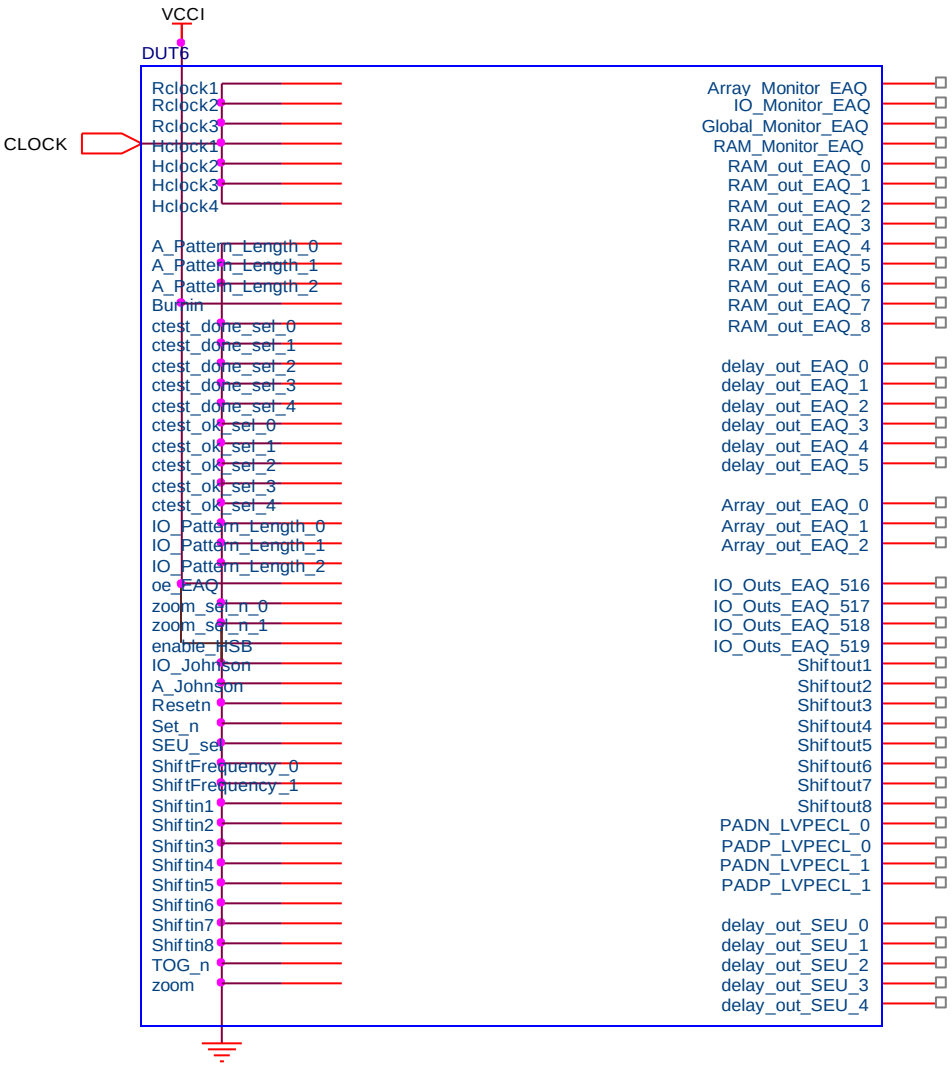


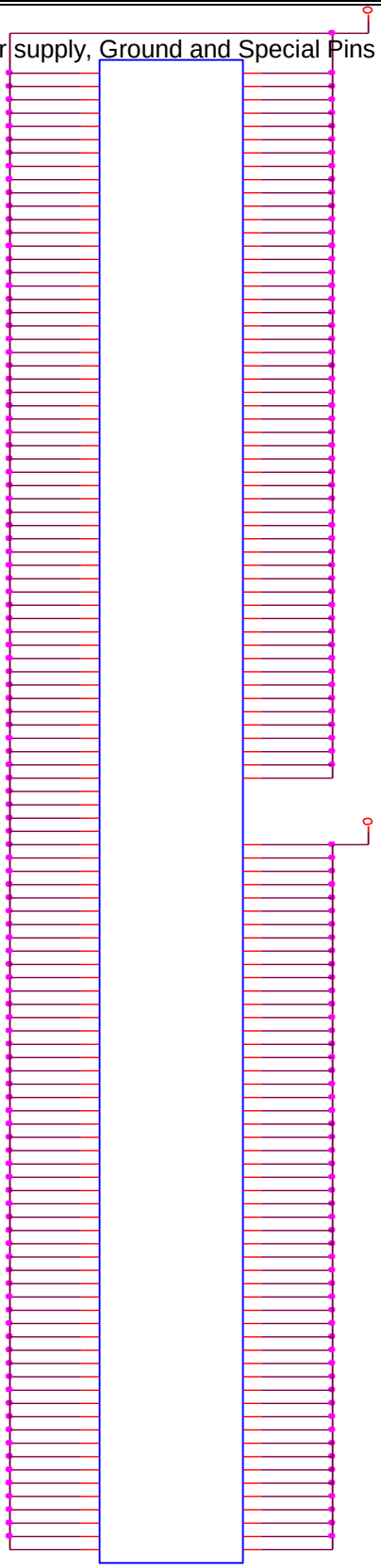
Figure A1 I/O Bias During Irradiation

VCCI_3.3

DUT1D

B11			AB10
B14	VCCI1	VCCR	AB27
B17	VCCI1	VCCR	AF19
B5	VCCI1	VCCR	AH29
B8	VCCI1	VCCR	AJ9
F11	VCCI1	VCCR	AK30
F14	VCCI1	VCCR	AK7
F17	VCCI1	VCCR	AM31
F8	VCCI1	VCCR	F19
K11	VCCI1	VCCR	G31
K14	VCCI1	VCCR	G6
K17	VCCI1	VCCR	H29
N15	VCCI1	VCCR	L18
N17	VCCI1	VCCR	R10
B20	VCCI1	VCCR	V11
B23	VCCI2	VCCR	V26
B26	VCCI2	VCCR	E5
B29	VCCI2	VPP1	F31
B32	VCCI2	VPP10	C21
F20	VCCI2	VPP11	J29
F23	VCCI2	VPP12	G30
F26	VCCI2	VPP13	E24
F29	VCCI2	VPP14	H28
K20	VCCI2	VPP15	AL30
K23	VCCI2	VPP16	AM24
K26	VCCI2	VPP17	AM32
N20	VCCI2	VPP18	AJ28
N22	VCCI2	VPP19	E13
E35	VCCI2	VPP2	AP21
H31	VCCI3	VPP20	AE22
H35	VCCI3	VPP21	AN21
K27	VCCI3	VPP22	AF18
L31	VCCI3	VPP23	AN16
L35	VCCI3	VPP24	AM6
P27	VCCI3	VPP25	AP16
P31	VCCI3	VPP26	AM5
P35	VCCI3	VPP27	AH8
R24	VCCI3	VPP28	AM13
U24	VCCI3	VPP29	E6
U27	VCCI3	VPP3	AL6
U31	VCCI3	VPP30	N13
U35	VCCI3	VPP4	C16
AB24	VCCI4	VPP5	L19
AC27	VCCI4	VPP6	D16
AC31	VCCI4	VPP7	M22
AC35	VCCI4	VPP8	D21
AF31	VCCI4	VPP9	A19
AF35	VCCI4	VSV	AE12
AG27	VCCI4	VSV	AL32
AJ31	VCCI4	VSV	AL5
AJ35	VCCI4	VSV	AT18
AM35	VCCI4	VSV	J30
Y24	VCCI4	VSV	M12
Y27	VCCI4	VSV	W33
Y31	VCCI4		
Y35	VCCI4		
AD20	VCCI5		VCCA_1.5
AD22	VCCI5		
AG20	VCCI5	VCC	AA14
AG23	VCCI5	VCC	AA16
AG26	VCCI5	VCC	AA18
AL20	VCCI5	VCC	AA20
AL23	VCCI5	VCC	AA22
AL26	VCCI5	VCC	AB15
AL29	VCCI5	VCC	AB17
AR20	VCCI5	VCC	AB19
AR23	VCCI5	VCC	AB21
AR26	VCCI5	VCC	AB23
AR29	VCCI5	VCC	AC14
AR32	VCCI5	VCC	AC16
AD15	VCCI6	VCC	AC18
AD17	VCCI6	VCC	AC20
AG11	VCCI6	VCC	AC22
AG14	VCCI6	VCC	AP3
AG17	VCCI6	VCC	AP34
AL11	VCCI6	VCC	C3
AL14	VCCI6	VCC	C34
AL17	VCCI6	VCC	P15
AL8	VCCI6	VCC	P17
AR11	VCCI6	VCC	P19
AR14	VCCI6	VCC	P21
AR17	VCCI6	VCC	P23
AR5	VCCI6	VCC	R14
AR8	VCCI6	VCC	R16
AB13	VCCI7	VCC	R18
AC10	VCCI7	VCC	R20
AC2	VCCI7	VCC	R22
AC6	VCCI7	VCC	T15
AF2	VCCI7	VCC	T17
AF6	VCCI7	VCC	T19
AG10	VCCI7	VCC	T21
AJ2	VCCI7	VCC	T23
AJ6	VCCI7	VCC	U14
AM2	VCCI7	VCC	U16
Y10	VCCI7	VCC	U18
Y13	VCCI7	VCC	U20
Y2	VCCI7	VCC	U22
Y6	VCCI7	VCC	V15
E2	VCCI8	VCC	V17
H2	VCCI8	VCC	V19
H6	VCCI8	VCC	V21
K10	VCCI8	VCC	V23
L2 L6	VCCI8	VCC	W14
P10	VCCI8	VCC	W16
P2	VCCI8	VCC	W18
P6	VCCI8	VCC	W20
R13	VCCI8	VCC	W22
U10	VCCI8	VCC	Y15
U13	VCCI8	VCC	Y17
U2	VCCI8	VCC	Y19
U6	VCCI8	VCC	Y21
	VCCI8	VCC	Y23

Figure A2 Power supply, Ground and Special Pins Bias During Irradiation



Appendix B: Functionality Tests

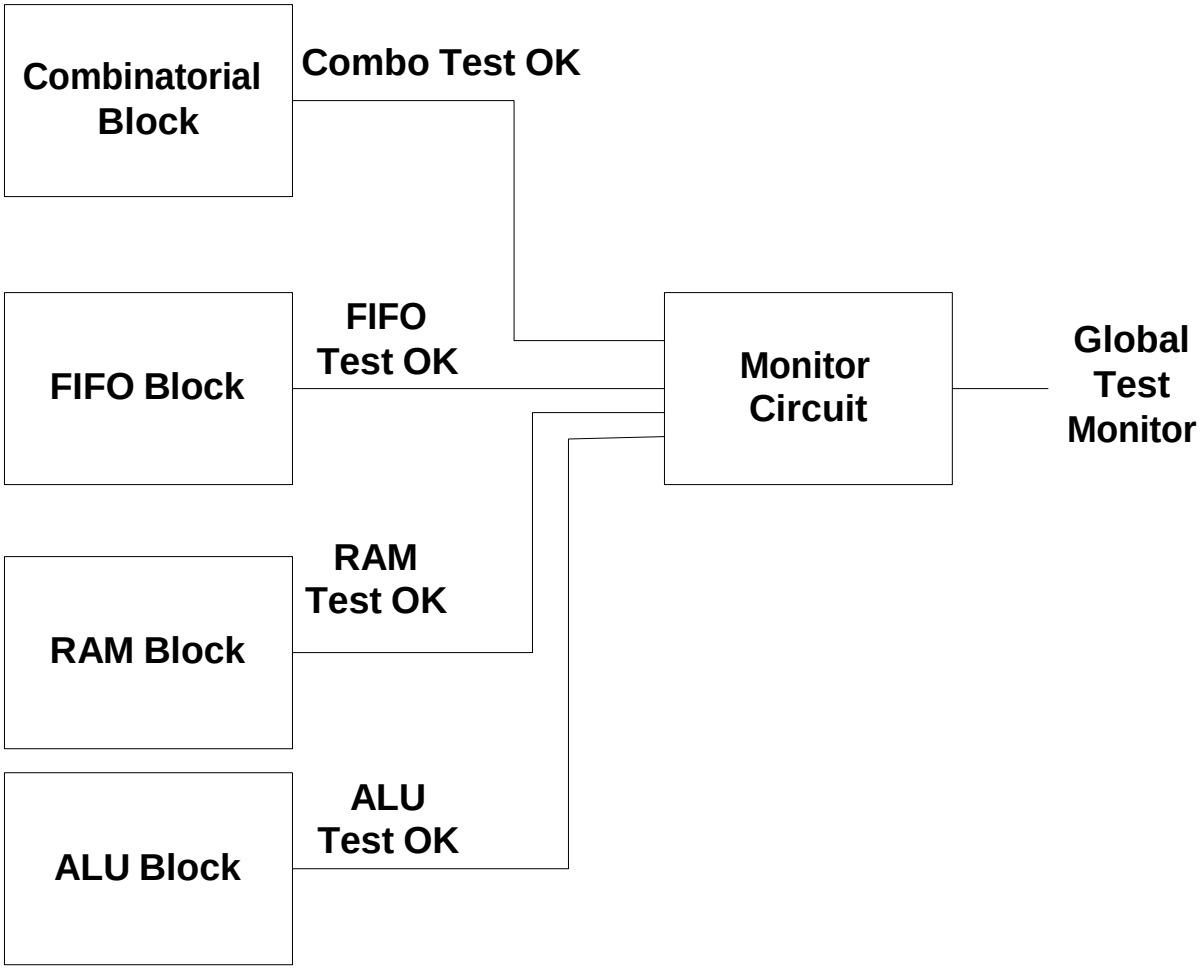


Figure B1 QBI Block – Top-Level Design

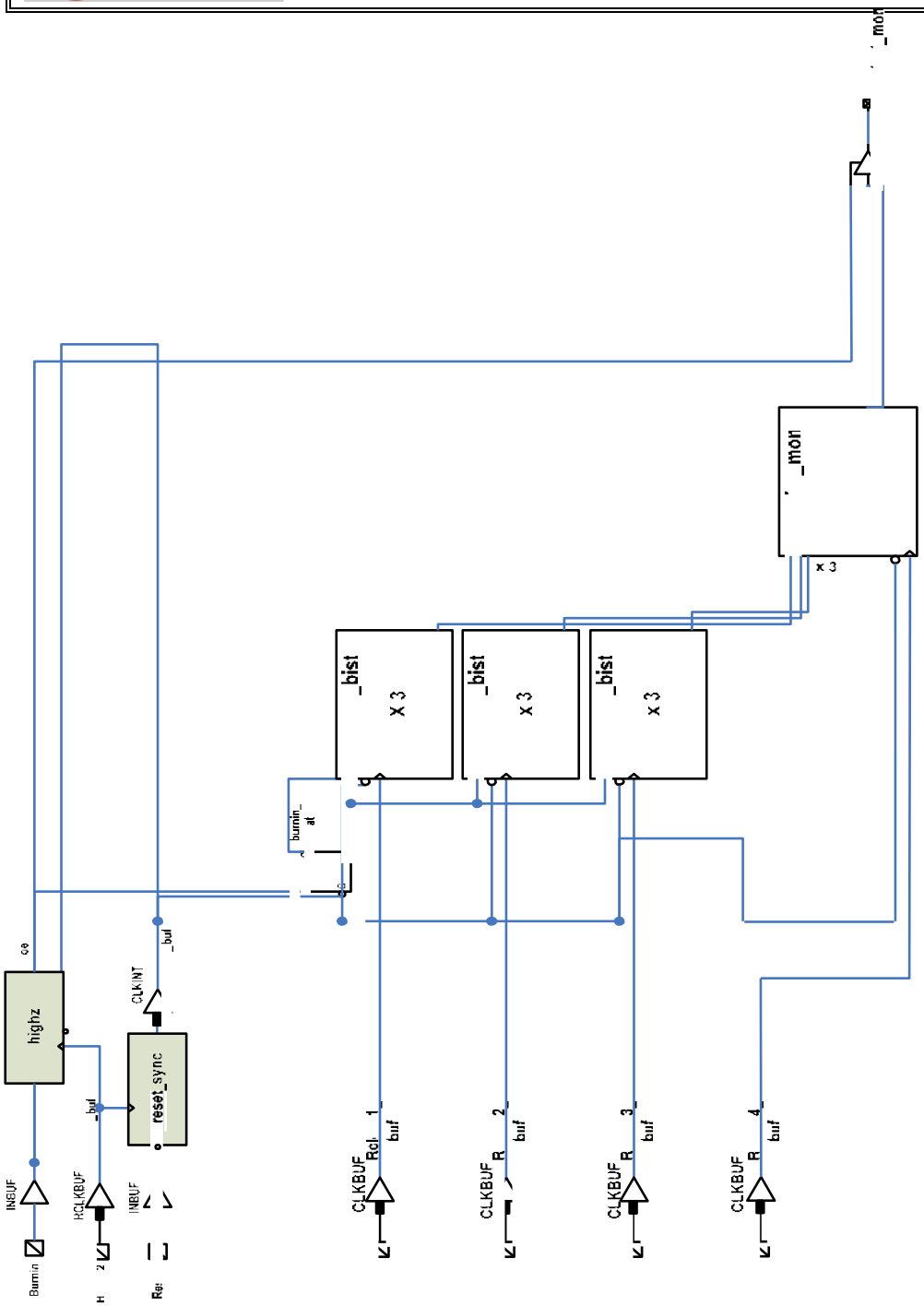

_mon
x 3
_bist
x 3
_bist
x 3
_bist
x 3
burnin_
at
highz
CLKINT
reset_sync
_buf
INBUF
HCLKBUF
INBUF
CLKBUF
CLKBUF
CLKBUF
CLKBUF

Figure B2 QBI Block – Combinatorial Test (Top Level)

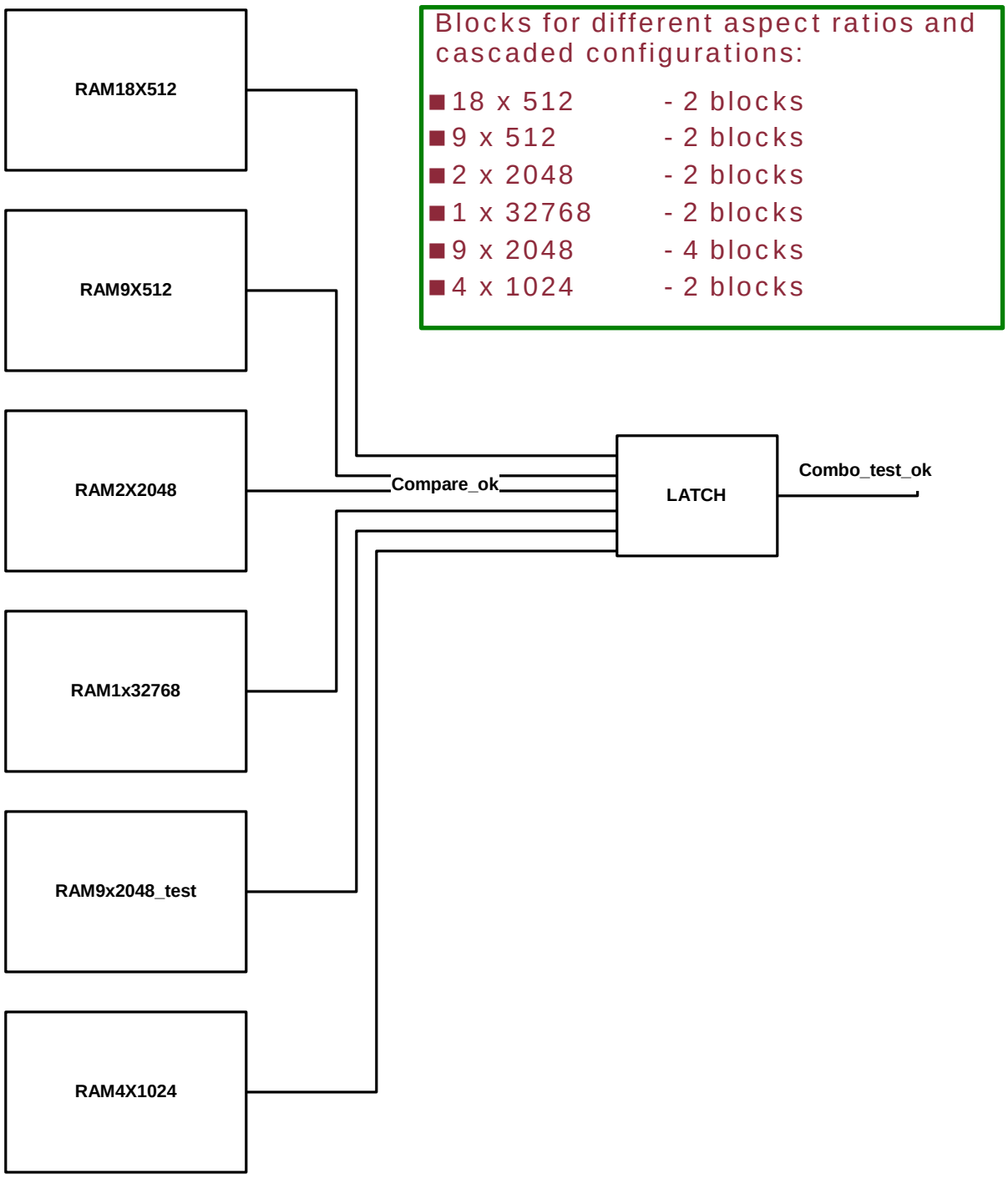


Figure B3 QBI Block – RAM Test (Top Level)

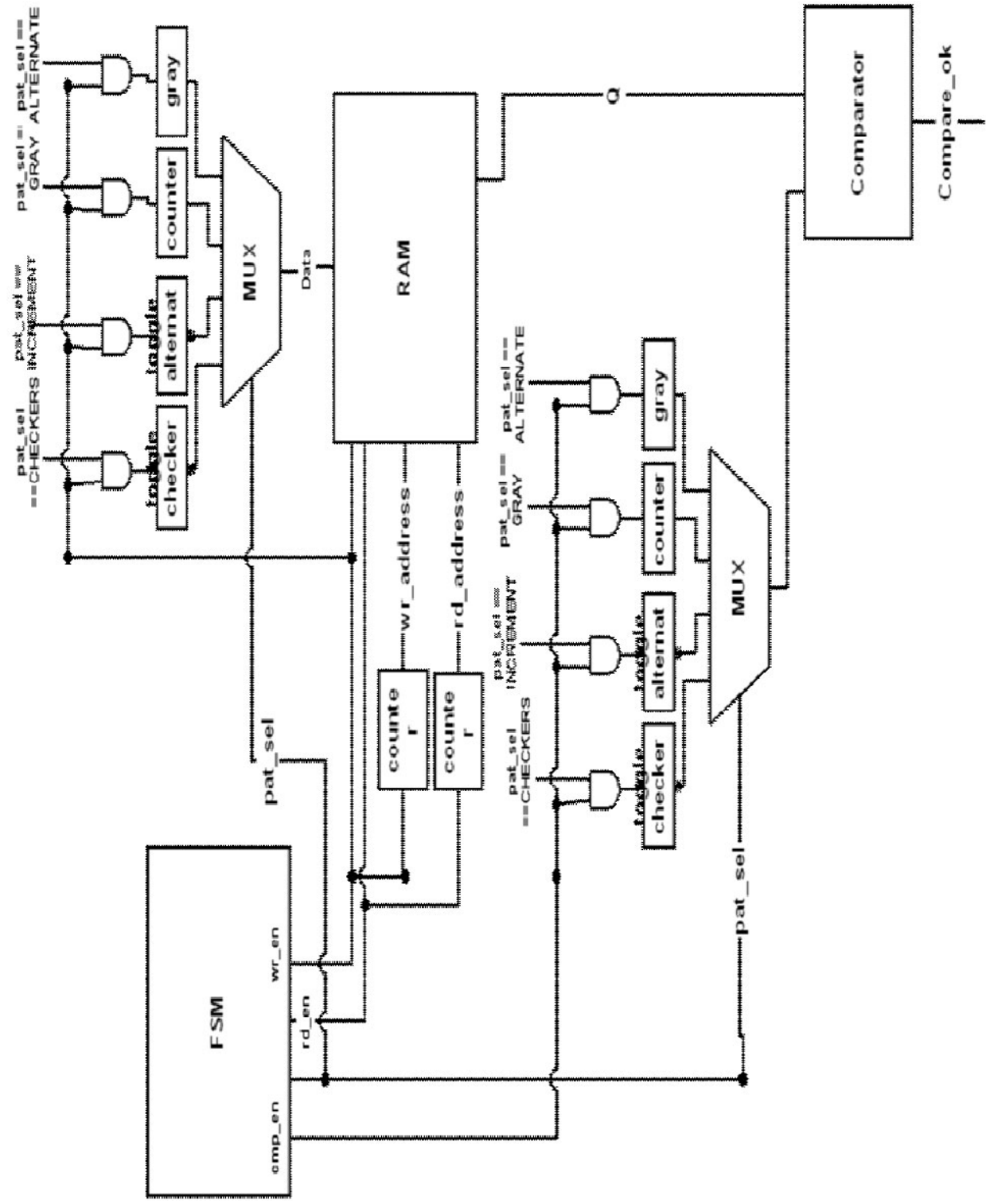


Figure B4 QBI Block – RAM Block

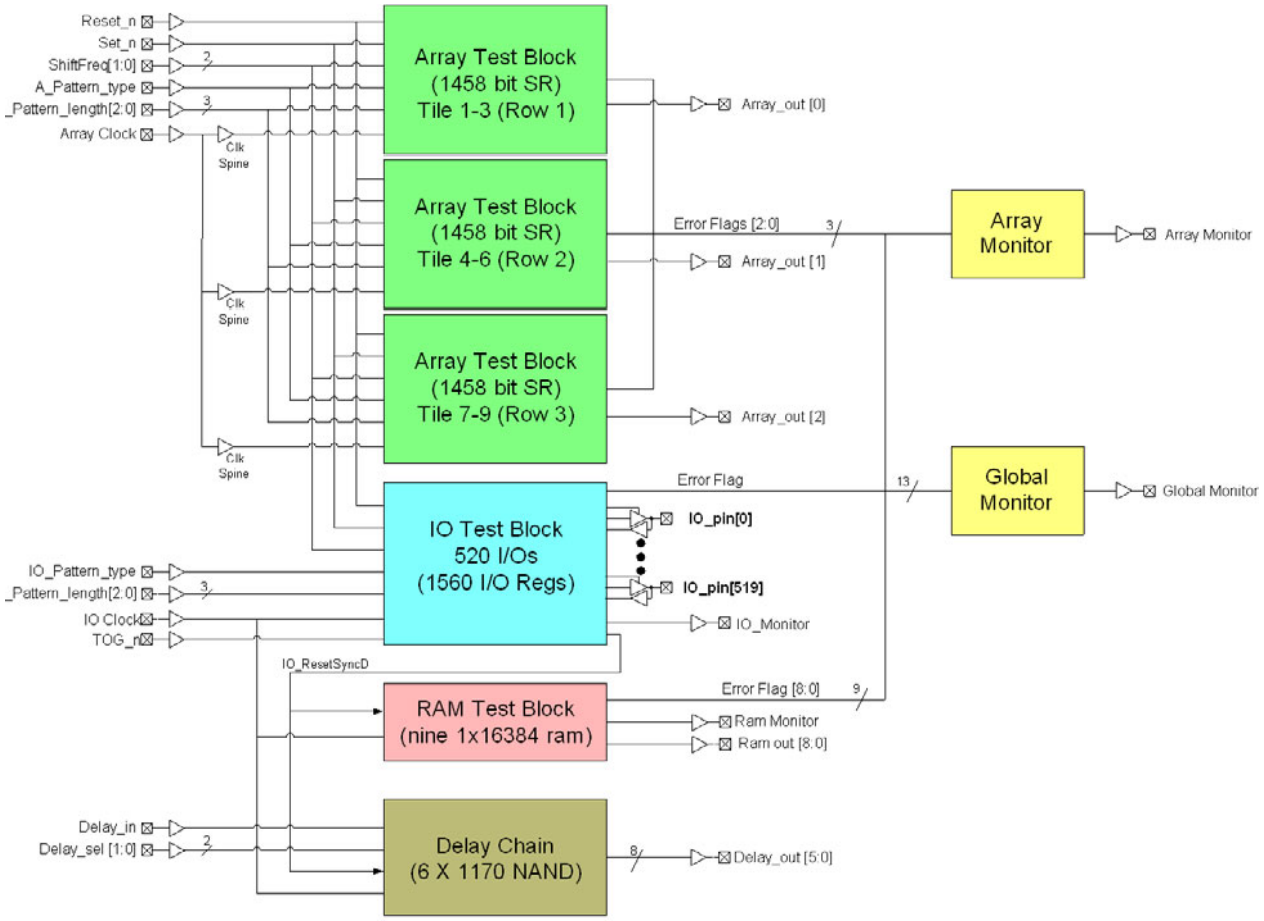


Figure B5 EAQ Block – Top Level

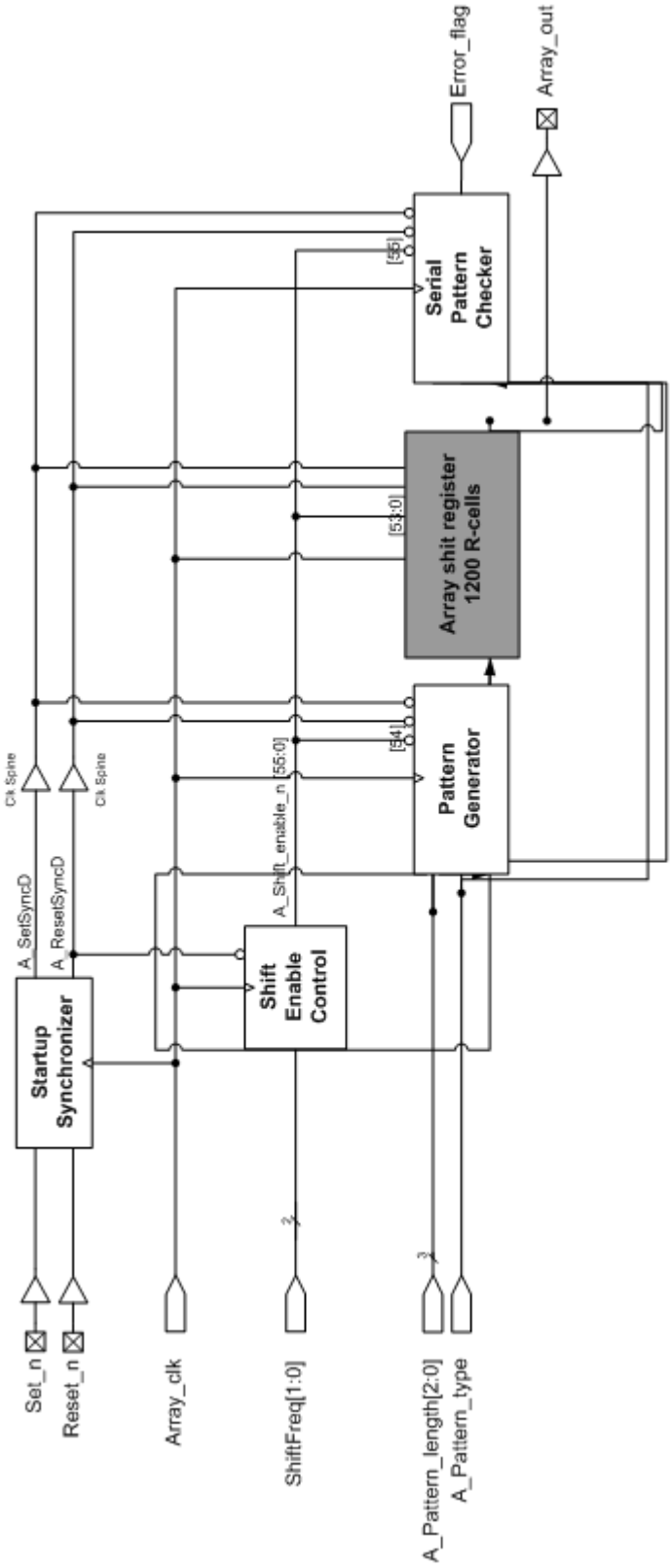


Figure B6 EAQ Block – Array Test (Shift Register)

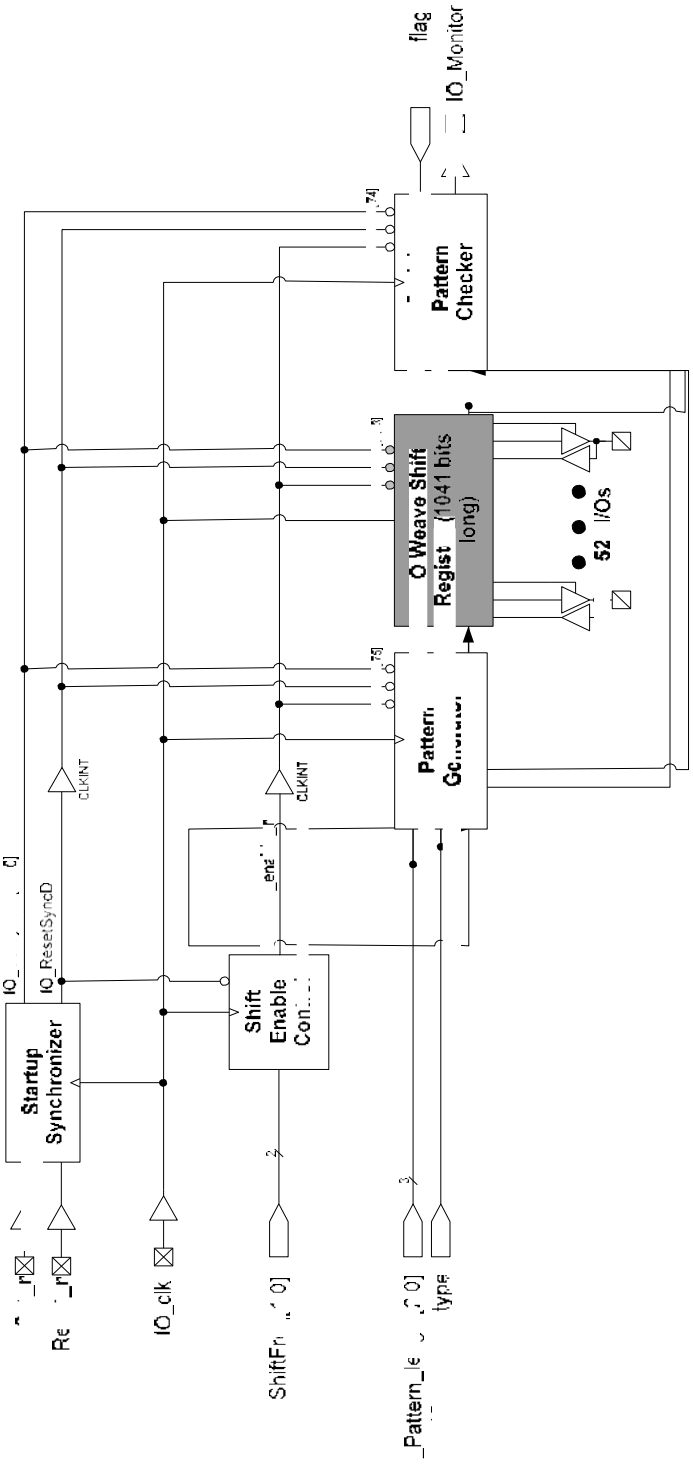


Figure B7 EAQ Block – I/O Test (Top Level)

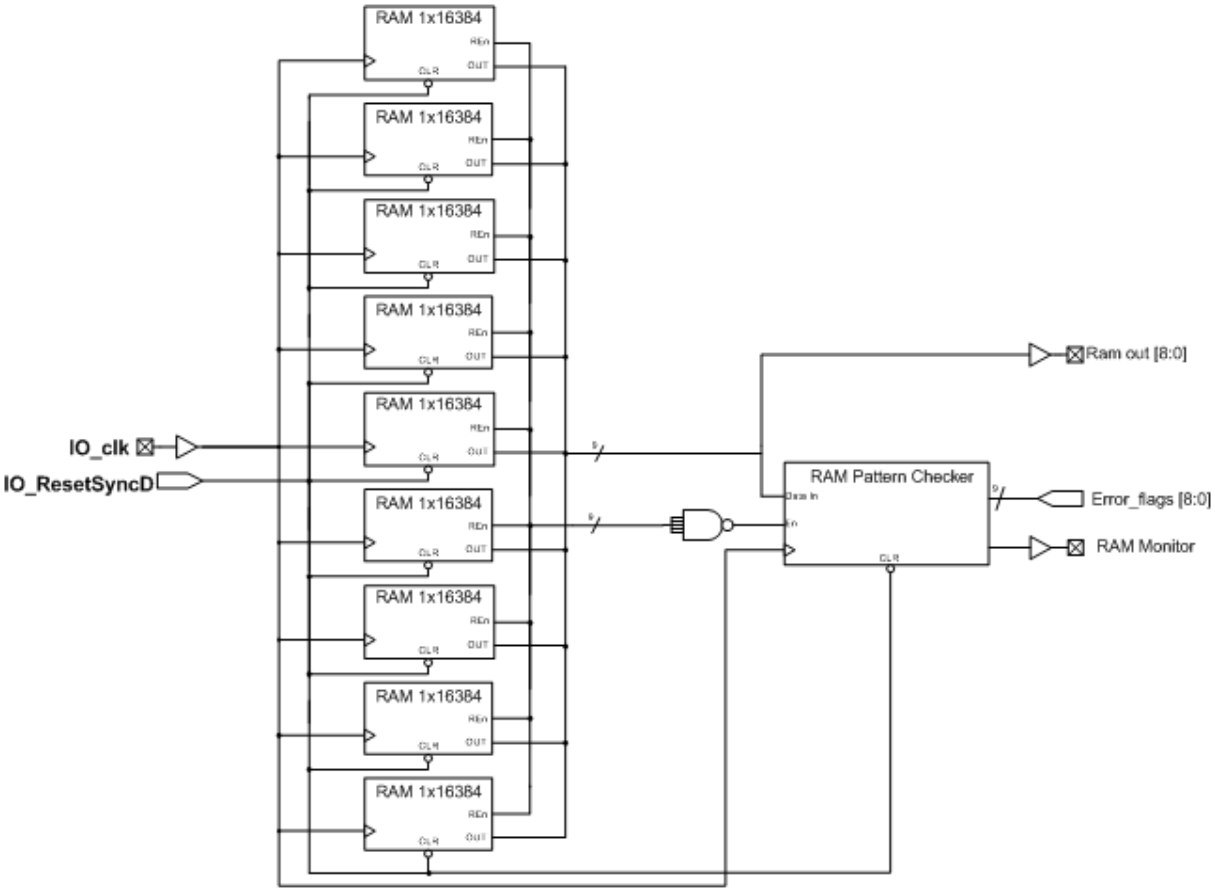


Figure B8 EAQ Block – SRAM Test (Top Level)

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