19-5050; Rev 1; 6/10

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

General Description

The MAX3612 is a high-performance, precision phase-locked loop (PLL) clock generator optimized for next-generation high-speed Ethernet applications that demand low-jitter clock generation and distribution for robust high-speed data transmission. The device features subpicosecond jitter generation, excellent power-supply noise rejection, and pin-programmable LVDS/LVPECL output interfaces. The MAX3612 provides nine differential outputs divided into three banks. The frequency and output interface of each output bank can be individually programmed, making this device an ideal replacement for multiple crystal oscillators and clock distribution ICs on a system board, saving cost and space.

This 3.3V IC is available in a 7mm x 7mm, 48-pin TQFN package and operates from -40°C to +85°C.

Applications

Ethernet Switch/Router

Typical Application Circuits and Pin Configuration appear at end of data sheet.

Features

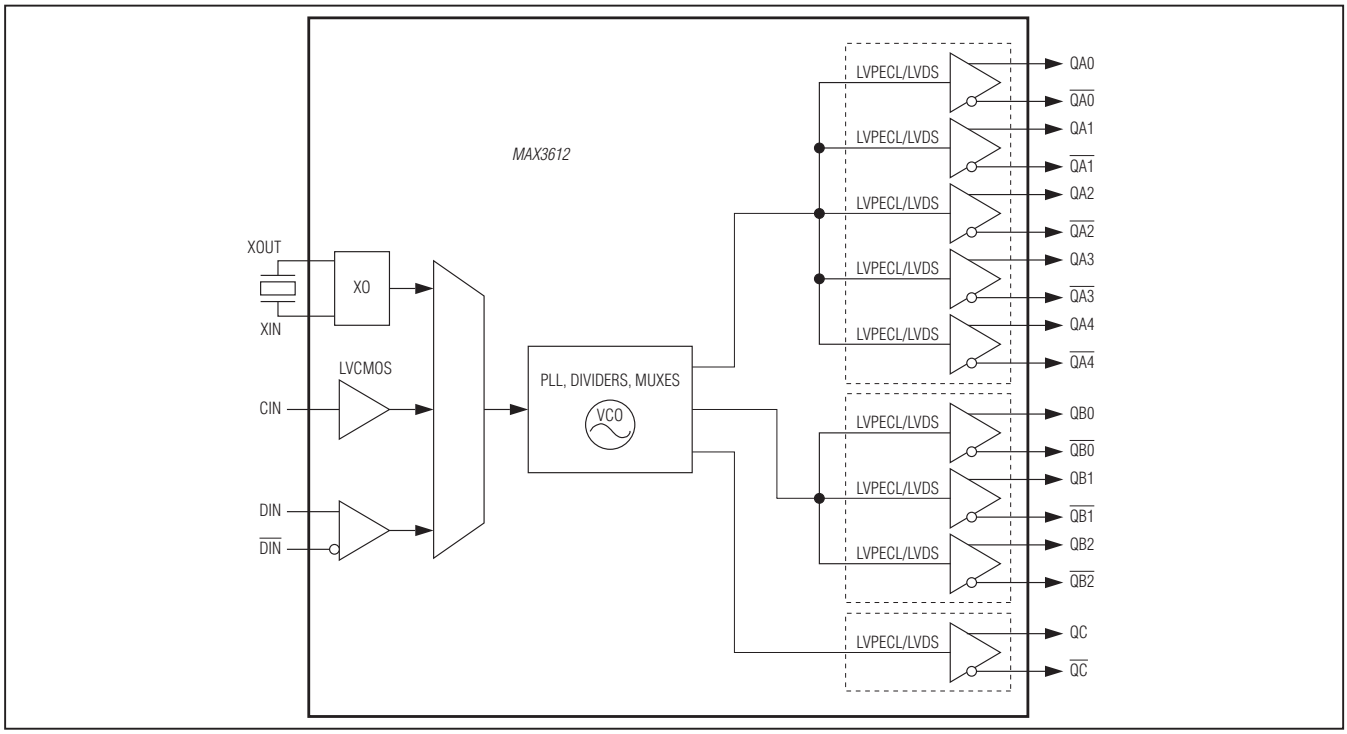
- **Inputs**
  - **Crystal Interface: 25MHz, 31.25MHz**
  - **LVCMOS Input: 25MHz, 31.25MHz, 125MHz, 156.25MHz**
  - **Differential Input: 25MHz, 31.25MHz, 125MHz, 156.25MHz**
- **Outputs**
  - **LVDS/LVPECL Outputs: 125MHz, 156.25MHz, 312.5MHz**
- **Three Individual Output Banks**
  - **Pin-Programmable Dividers**
  - **Pin-Programmable Output Interface**
- **Low Phase Jitter**
  - **0.34ps$_{RMS}$ (12kHz to 20MHz)**
  - **0.14ps$_{RMS}$ (1.875MHz to 20MHz)**
- **Excellent Power-Supply Noise Rejection**
- **Operating Temperature Range: -40°C to +85°C**
- **+3.3V Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3612ETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Functional Diagram



Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}, V_{CCA}, V_{CCQA}, V_{CCQB}, V_{CCQC}) ..... -0.3V to +4.0V
Voltage Range at CIN, IN_SEL, DM, DF, PLL_BP, DA, DB, DC, QA_CTRL1, QA_CTRL2, QB_CTRL, QC_CTRL, RES[6:0] ..... -0.3V to (V_{CC} + 0.3V)
Voltage Range at DIN, $\overline{DIN}$ ..... (V_{CC} - 2.35V) to (V_{CC} - 0.35V)
Voltage Range at QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$ when LVDS Output ... -0.3V to (V_{CC} + 0.3V)
Current into QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$ when LVPECL Output ..... -56mA
Voltage Range at XIN ..... -0.3V to +1.2V
Voltage Range at XOUT ..... -0.3V to (V_{CC} - 0.6V)
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 40mW/°C above +70°C) 3200mW
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current with PLL Enabled (Note 2)	I_{CC}	Configured with LVPECL outputs		150	200	mA
		Configured with LVDS outputs		270	360	
Supply Current with PLL Bypassed (Note 2)		Configured with LVPECL outputs		100		mA
		Configured with LVDS outputs		220		
LVCMOS/LVTTL CONTROL INPUTS (IN_SEL, DM, DF, DA, DB, DC, PLL_BP, QA_CTRL1, QA_CTRL2, QB_CTRL, QC_CTRL)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-80			µA
LVCMOS/LVTTL CLOCK INPUT (CIN)						
Reference Clock Input Frequency	f_{REF}		15		160	MHz
Input Amplitude Range		Internally AC-coupled (Note 3)	1.2		3.6	V_{P-P}
Input High Current	I_{IH}	V_{IN} = V_{CC}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0V	-80			µA
Reference Clock Input Duty-Cycle Distortion			40		60	%
Input Capacitance				1.5		pF
DIFFERENTIAL CLOCK INPUT (DIN, $\overline{DIN}$) (Note 4)						
Differential Input Frequency	f_{REF}		15		350	MHz
Input Bias Voltage	V_{CMI}		V_{CC} - 1.8	V_{CC} - 1.3		V
Input Differential Voltage Swing			150		1800	mV_{P-P}
Single-Ended Voltage Range			V_{CC} - 2.0		V_{CC} - 0.7	V
Input Differential Impedance			80	100	120	Ω
Differential Input Capacitance				1.5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS OUTPUTS (QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$) (Note 5)						
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\lvert V_{OD}\rvert$		250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\lvert V_{OD}\rvert$				25	mV
Output Offset Voltage	V_{OS}		1.125		1.3	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\lvert V_{OS}\rvert$				25	mV
Differential Output Impedance			80	100	140	Ω
Output Current		Short together		3		mA
		Short to ground		6		
Output Current When Disabled		$V_{Q\_}$ = $V_{\overline{Q\_}}$ = 0V to V_{CC}		10		µA
Output Rise/Fall Time		20% to 80%		160	240	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 6)		50		
LVPECL OUTPUTS (QA[4:0], $\overline{QA[4:0]}$, QB[2:0], $\overline{QB[2:0]}$, QC, $\overline{QC}$) (Note 7)						
Output High Voltage	V_{OH}		V_{CC} - 1.13	V_{CC} - 0.98	V_{CC} - 0.83	V
Output Low Voltage	V_{OL}		V_{CC} - 1.85	V_{CC} - 1.70	V_{CC} - 1.55	V
Output-Voltage Swing (Single-Ended)			0.5	0.7	0.9	V_{P-P}
Output Current When Disabled		V_O = 0V to V_{CC}		10		µA
Output Rise/Fall Time		20% to 80%, differential load = 100Ω		140	240	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 6)		50		
PLL SPECIFICATIONS						
VCO Frequency Range	f_{VCO}			625		MHz
PLL Jitter Transfer Bandwidth				130		kHz
Integrated Phase Jitter at 156.25MHz Output	RJ_{RMS}	25MHz crystal input, 12kHz to 20MHz		0.34	1.0	ps_{RMS}
		25MHz crystal input, 1.875MHz to 20MHz		0.14		
		25MHz LVCMOS or differential input (Note 8)		0.34		
Supply-Noise Induced Phase Spur		(Note 9)		-56		dBc
Deterministic Jitter Induced by Power-Supply Noise		(Note 9)		6		ps_{P-P}

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. Signal applied to CIN or DIN/$\overline{DIN}$ only when selected as the reference clock.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nonharmonic and Subharmonic Spurs		(Note 10)		-70		dBc
SSB Phase Noise at 312.5MHz		f_{OFFSET} = 1kHz		-115		dBc/Hz
		f_{OFFSET} = 10kHz		-116		
		f_{OFFSET} = 100kHz		-122		
		f_{OFFSET} = 1MHz		-139		
		$f_{OFFSET} \geq$ 10MHz		-149		
SSB Phase Noise at 156.25MHz		f_{OFFSET} = 1kHz		-122		dBc/Hz
		f_{OFFSET} = 10kHz		-123		
		f_{OFFSET} = 100kHz		-129		
		f_{OFFSET} = 1MHz		-145		
		$f_{OFFSET} \geq$ 10MHz		-152		
SSB Phase Noise at 125MHz		f_{OFFSET} = 1kHz		-123		dBc/Hz
		f_{OFFSET} = 10kHz		-124		
		f_{OFFSET} = 100kHz		-130		
		f_{OFFSET} = 1MHz		-147		
		$f_{OFFSET} \geq$ 10MHz		-153		

Note 1: A series resistor of up to 10.5Ω is allowed between V_{CC} and V_{CCA} for filtering supply noise when system power-supply tolerance is V_{CC} = 3.3V ±5%. See Figure 2.

Note 2: Measured with all outputs enabled and unloaded.

Note 3: CIN can be AC- or DC-coupled. See Figure 7. Input high voltage must be ≤ V_{CC} to +0.3V.

Note 4: DIN can be AC- or DC-coupled. See Figure 9.

Note 5: Measured with 100Ω differential load.

Note 6: Measured with crystal input, or with 50% duty cycle LVCMOS, or differential input.

Note 7: Measured with output termination of 50Ω to V_{CC} - 2V or Thevenin equivalent.

Note 8: Measured using LVCMOS/LVTTL input with slew rate ≥ 1.0V/ns, or differential input with slew rate ≥ 0.5V/ns.

Note 9: Measured at 156.25MHz output with 200kHz, 50mV_{P-P} sinusoidal signal on the supply using the crystal input and the power-supply filter shown in Figure 2. See the *Typical Operating Characteristics* for other supply noise frequencies. Deterministic jitter is calculated from the measured power-supply-induced spurs. For more information, refer to Application Note 4461: *HFAN-04.5.5: Characterizing Power-Supply Noise Rejection in PLL Clock Synthesizers*.

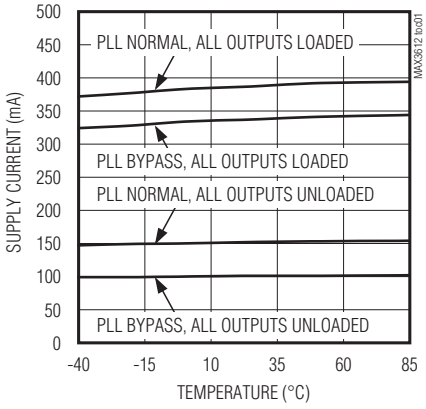
Note 10: Measured with all outputs enabled and all three banks at different frequencies.

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

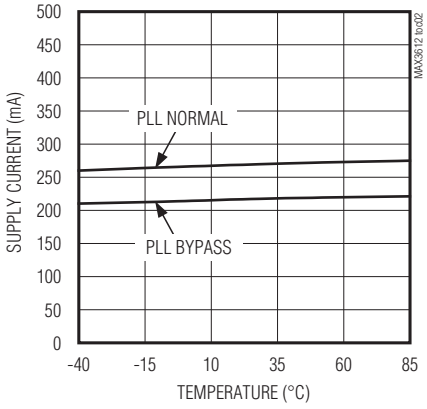
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

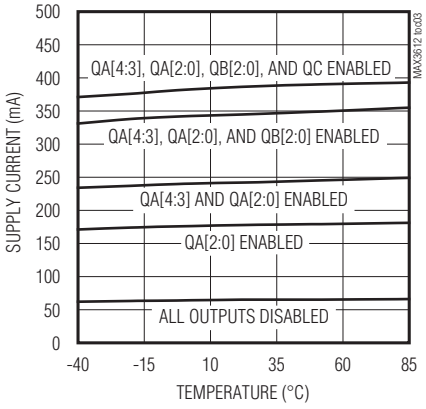
SUPPLY CURRENT vs. TEMPERATURE (LVPECL OUTPUTS, ALL ENABLED)



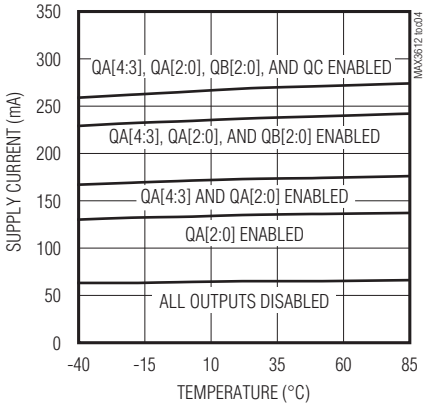
SUPPLY CURRENT vs. TEMPERATURE (LVDS OUTPUTS, ALL ENABLED)



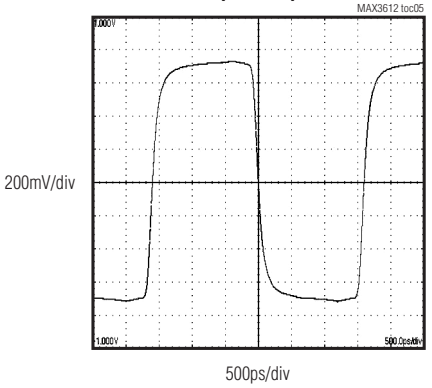
SUPPLY CURRENT vs. TEMPERATURE (LVPECL OUTPUTS, ALL LOADED)



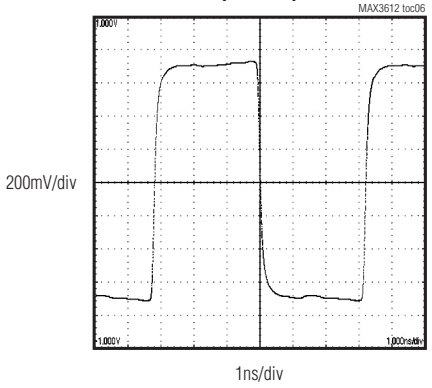
SUPPLY CURRENT vs. TEMPERATURE (LVDS OUTPUTS)



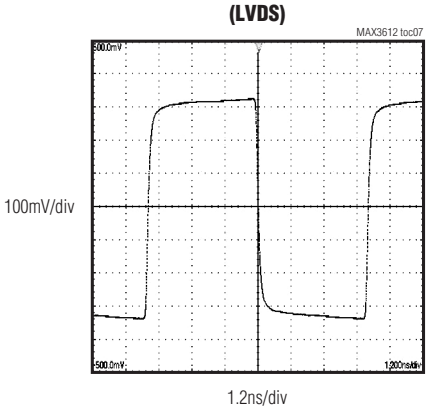
DIFFERENTIAL OUTPUT AT 312.5MHz (LVPECL)



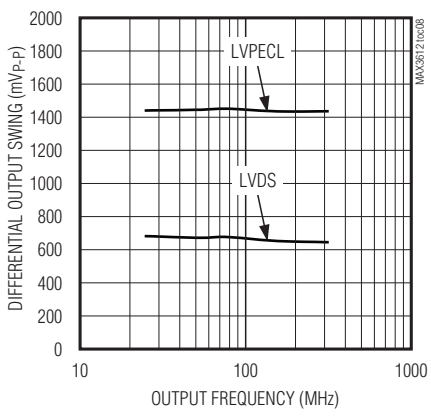
DIFFERENTIAL OUTPUT AT 156.25MHz (LVPECL)



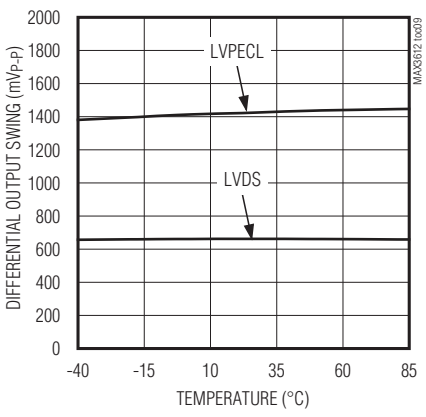
DIFFERENTIAL OUTPUT AT 125MHz (LVDS)



DIFFERENTIAL OUTPUT SWING vs. OUTPUT FREQUENCY



DIFFERENTIAL OUPUT SWING vs. TEMPERATURE

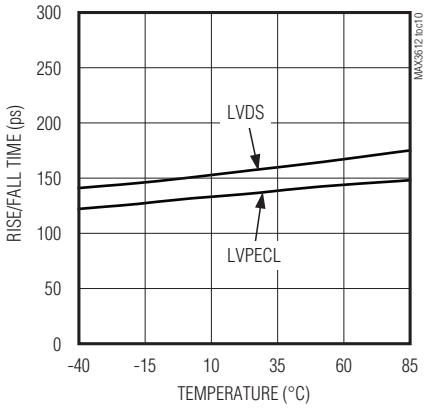


Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

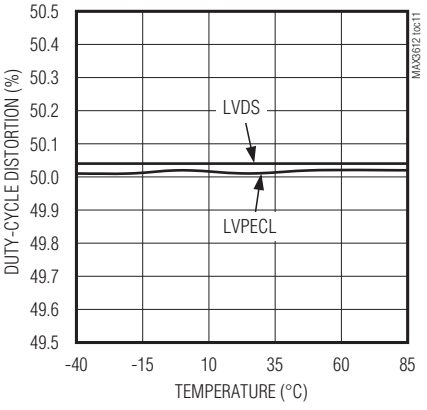
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

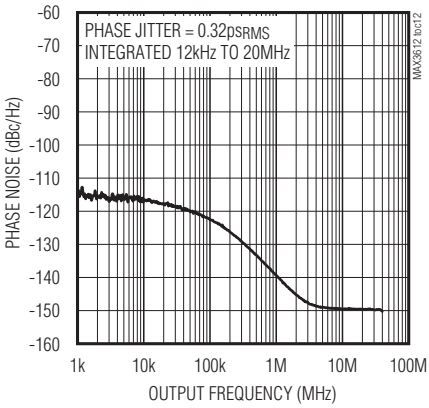
RISE/FALL TIME vs. TEMPERATURE (20% TO 80%)



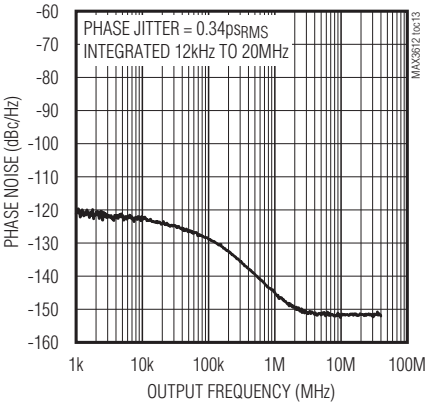
DUTY-CYCLE DISTORTION vs. TEMPERATURE



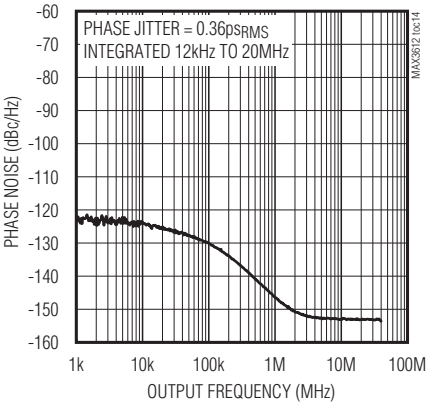
PHASE NOISE AT 312.5MHz



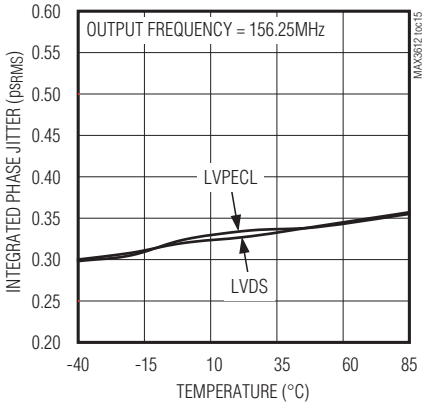
PHASE NOISE AT 156.25MHz



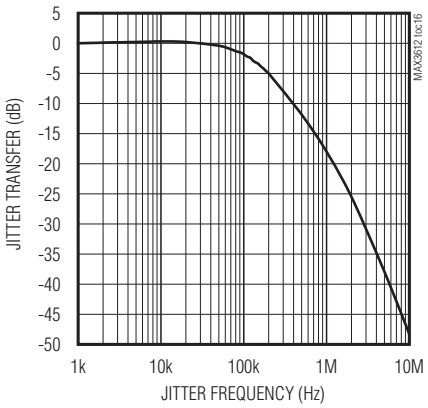
PHASE NOISE AT 125MHz



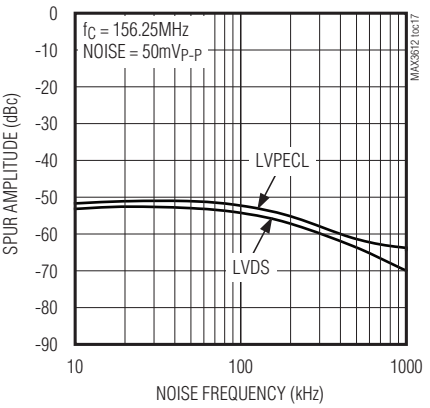
INTEGRATED PHASE JITTER (12kHz TO 20MHz) vs. TEMPERATURE



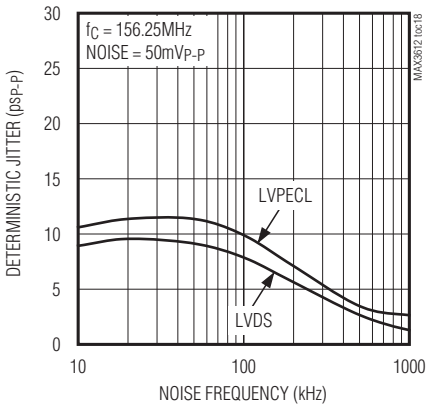
JITTER TRANSFER



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



DETERMINISTIC JITTER INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	DM	LVCMOS/LVTTL Input. Control for input divider M. See Table 3.
2	XIN	Crystal Oscillator Input
3	XOUT	Crystal Oscillator Output
4, 20	V_{CC}	Positive Power Supply. Connect to +3.3V.
5	IN_SEL	LVCMOS/LVTTL Input. Three-level control for input mux. See Table 1.
6	PLL_BP	LVCMOS/LVTTL Input. Three-level control for PLL bypass mode. See Table 2.
7	RES0	Reserved. Connect to GND for normal operation.
8	DF	LVCMOS/LVTTL Input. Control for feedback divider F. See Table 4.
9	QC_CTRL	LVCMOS/LVTTL Input. Three-level control input for C-bank output interface. See Table 8.
10	V_{CCA}	Power Supply for Internal Voltage-Controlled Oscillators (VCOs). See Figure 3.
11	RES1	Reserved. Connect to GND for normal operation.
12	RES2	Reserved. Connect to V_{CC} for normal operation.
13	RES3	Reserved. Connect to GND for normal operation.
14	DB	LVCMOS/LVTTL Input. Three-level controls for output divider B. See Table 5.
15	RES4	Reserved. Connect to GND for normal operation.
16	DA	LVCMOS/LVTTL Input. Three-level controls for output divider A. See Table 5.
17	RES5	Reserved. Connect to GND for normal operation.
18	DC	LVCMOS/LVTTL Input. Three-level controls for output divider C. See Table 5.
19	QA_CTRL2	LVCMOS/LVTTL Input. Three-level control for QA[4:3] output interface. See Table 6.
21	RES6	Reserved. Connect to GND for normal operation.
22, 23	$\overline{QC}$, QC	C-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QC_CTRL pin.
24	V_{CCQC}	Power Supply for C-Bank Differential Output. Connect to +3.3V.
25, 36	V_{CCQA}	Power Supply for A-Bank Differential Outputs. Connect to +3.3V.
26, 27	$\overline{QA4}$, QA4	A-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QA_CTRL2 pin.
28, 29	$\overline{QA3}$, QA3	A-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QA_CTRL2 pin.
30, 31	$\overline{QA2}$, QA2	A-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QA_CTRL1 pin.
32, 33	$\overline{QA1}$, QA1	A-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QA_CTRL1 pin.
34, 35	$\overline{QA0}$, QA0	A-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QA_CTRL1 pin.
37	V_{CCQB}	Power Supply for B-Bank Differential Outputs. Connect to +3.3V.
38, 39	$\overline{QB0}$, QB0	B-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QB_CTRL pin.
40, 41	$\overline{QB1}$, QB1	B-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QB_CTRL pin.
42, 43	$\overline{QB2}$, QB2	B-Bank Differential Output. Configured as LVPECL, LVDS, or high-Z with the QB_CTRL pin.
44	QA_CTRL1	LVCMOS/LVTTL Input. Three-level control for QA[2:0] output interface. See Table 6.
45	QB_CTRL	LVCMOS/LVTTL Input. Three-level control for B-bank output interface. See Table 7.
46, 47	$\overline{DIN}$, DIN	Differential Clock Input. Operates up to 350MHz. This input can accept DC-coupled LVPECL signals, and is internally biased to accept AC-coupled LVDS, CML, and LVPECL signals.
48	CIN	LVCMOS Clock Input. Operates up to 160MHz.
—	EP	Exposed Pad. Connect to supply ground for proper electrical and thermal performance.

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

Detailed Description

The MAX3612 is a low-jitter clock generator optimized for Ethernet applications. It consists of a selectable reference clock (on-chip crystal oscillator, LVCMOS input, or differential input), PLL with on-chip VCO, pin-programmable dividers and muxes, and three banks of clock outputs. See Figure 1. The output banks include nine pin-programmable LVDS/LVPECL output buffers. The frequency and output interface of each output bank can be individually programmed. A PLL bypass mode is also available for system testing or clock distribution.

Crystal Oscillator

The on-chip crystal oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between XIN and XOUT. See the *Crystal Selection and Layout* section for more

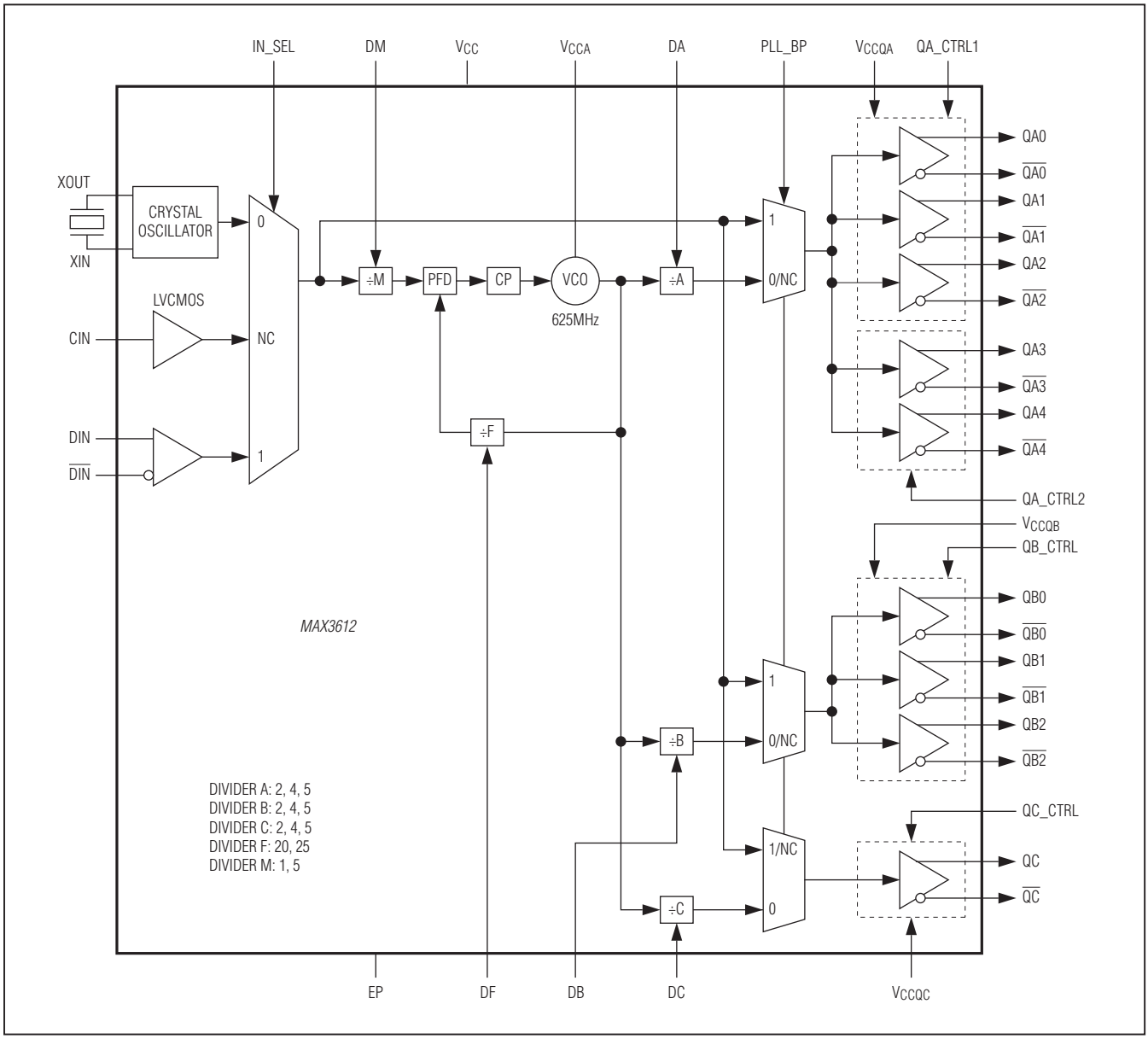


Figure 1. Detailed Functional Diagram

information. The XIN and XOUT pins can be left open if not used.

LVCMOS Clock Input

An LVCMOS-compatible clock source can be connected to CIN to serve as the PLL reference clock. The input is internally biased to allow AC- or DC-coupling (see the *Applications Information* section). It is designed to operate from 15MHz to 160MHz. No signal should be applied to CIN if not used.

Differential Clock Input

A differential clock source can be connected to DIN to serve as the PLL reference clock. This input operates from 15MHz to 350MHz and contains an internal 100Ω differential termination. This input can accept DC-coupled LVPECL signals, and is internally biased to accept AC-coupled LVDS, CML, and LVPECL signals (see the *Applications Information* section). No signal should be applied to DIN if not used.

Phase-Locked Loop (PLL)

The PLL takes the signal from the crystal oscillator, LVCMOS clock input, or differential clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a charge pump (CP), and a low-phase noise VCO. The VCO output is connected to the PFD input through a feedback divider. The PFD compares the reference frequency to the divided-down VCO output and generates a control signal that keeps the VCO locked to the reference clock. The high-frequency VCO output clock is sent to the output dividers. To minimize noise-induced jitter, the VCO supply (V_{CCA}) is isolated from the core logic and output buffer supplies.

Dividers and Muxes

The dividers and muxes are set with three-level control inputs. Divider settings and routing information are given in Tables 1 to 9.

Table 1. PLL Input

IN_SEL	INPUT
0	Crystal Input. XO circuit is disabled when not selected.
1	Differential Input. No signal should be applied to DIN if not selected.
NC	LVCMOS Input. No signal should be applied to CIN if not selected.

Table 2. PLL Bypass

PLL_BP	PLL OPERATION
0	PLL Enabled for Normal Operation. All outputs from the A-, B-, and C-banks are derived from the VCO.
1	PLL Bypassed. Selected input passes directly to the outputs. The VCO is disabled to minimize power consumption and intermodulation spurs. Used for system testing or clock distribution.
NC	The outputs from A-bank and B-bank are derived from the VCO, but the C-bank output is directly driven from the input signal for purposes of daisy chaining.

Table 3. Input Divider M

DM	M DIVIDER RATIO
0	÷1
1	÷5
NC	Not allowed

Note: *When the on-chip XO is selected (IN_SEL = 0), the setting DM = 0 is required.*

Table 4. PLL Feedback Divider F

DF	F DIVIDER RATIO
0	÷25
1	÷20
NC	Not allowed

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

Table 5. Output Divider A, B, C

DA/DB/DC	A, B, C DIVIDER RATIO
0	÷4
1	÷5
NC	÷2

Table 6. A-Bank Output Interface

QA_CTRL1	QA[2:0] OUTPUT
0	QA[2:0] = LVDS
1	QA[2:0] = LVPECL
NC	QA[2:0] disabled to high impedance
QA_CTRL2	**QA[4:3] OUTPUT**
0	QA[4:3] = LVDS
1	QA[4:3] = LVPECL
NC	QA[4:3] disabled to high impedance

Table 7. B-Bank Output Interface

QB_CTRL	QB[2:0] OUTPUT
0	QB[2:0] = LVDS
1	QB[2:0] = LVPECL
NC	QB[2:0] disabled to high impedance

Table 8. C-Bank Output Interface

QC_CTRL	QC OUTPUT
0	QC = LVDS
1	QC = LVPECL
NC	QC disabled to high impedance

LVDS/LVPECL Clock Outputs

The differential clock outputs (QA[4:0], QB[2:0], QC) operate up to 350MHz and have a pin-programmable LVDS/LVPECL output interface. See Tables 6 to 8. When configured as LVDS, the buffers are designed to drive transmission lines with a 100Ω differential termination. When configured as LVPECL, the buffers are designed to drive transmission lines terminated with 50Ω to V_{CC} - 2V. Unused output banks can be disabled to high impedance and unused outputs can be left open.

Internal Reset

During power-on, a power-on reset (POR) signal is generated to synchronize all dividers. A reset signal is also generated if any control pin is changed. Outputs within a bank are phase aligned, but outputs bank-to-bank may not be phase aligned.

Applications Information

Output Frequency Configuration

Table 9 provides the divider ratios for typical configurations.

Power-Supply Filtering

The MAX3612 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. To take full advantage of on-board filtering and noise attenuation, in addition to excellent on-chip power-supply rejection, this part provides a separate power-supply pin, V_{CCA}, for the VCO circuitry. Figure 2 illustrates the recommended power-supply filter network for V_{CCA}. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve

Table 9. Divider Configurations

INPUT FREQUENCY (MHz)	INPUT DIVIDER M	FEEDBACK DIVIDER F	VCO FREQUENCY (MHz)		OUTPUT DIVIDERS A, B, C	OUTPUT FREQUENCY (MHz)
25	÷1	÷25	625		÷2	312.5
31.25		÷20				
125	÷5	÷25			÷4	156.25
156.25		÷20			÷5	125

the overall immunity to power-supply noise. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins for best performance. All supply connections should be driven from the same source.

Ground Connection

The 48-pin TQFN package features an exposed pad (EP), which provides a low resistance thermal path for heat removal from the IC and also the electrical ground. For proper operation, the EP must be connected to the circuit board ground plane with multiple vias.

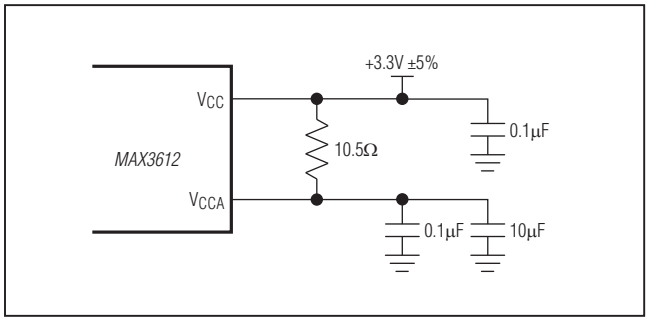


Figure 2. Power-Supply Filter

Crystal Selection and Layout

The MAX3612 features an integrated on-chip crystal oscillator to minimize system implementation cost.

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 10 for recommended crystal specifications. See Figure 3 for the crystal equivalent circuit and Figure 4 for the recommended external capacitor connections. The crystal, trace, and two external capacitors should be placed on the board as close as possible to the XIN and XOUT pins to reduce crosstalk of active signals into the oscillator.

The total load capacitance for the crystal is a combination of external and on-chip capacitance. The layout shown in Figure 5 gives approximately 1.7pF of trace plus footprint capacitance per side of the crystal. Note the ground plane is removed under the crystal to minimize capacitance. There is approximately 2.5pF of on-chip capacitance between XIN and XOUT. With an external 27pF capacitor connected to XIN and a 33pF external capacitor connected to XOUT, the total load capacitance for the crystal is approximately 18pF. The XIN and XOUT pins can be left open if not used.

Table 10. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	f_{OSC}		25		MHz
Shunt Capacitance	C_0		2.0	7.0	pF
Load Capacitance	C_L		18		pF
Equivalent Series Resistance (ESR)	R_S		10	50	Ω
Maximum Crystal Drive Level				200	µW

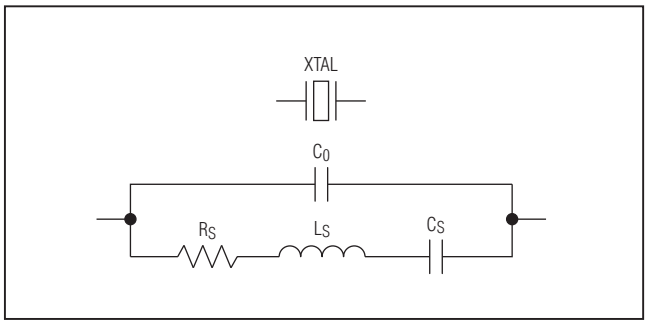


Figure 3. Crystal Equivalent Circuit

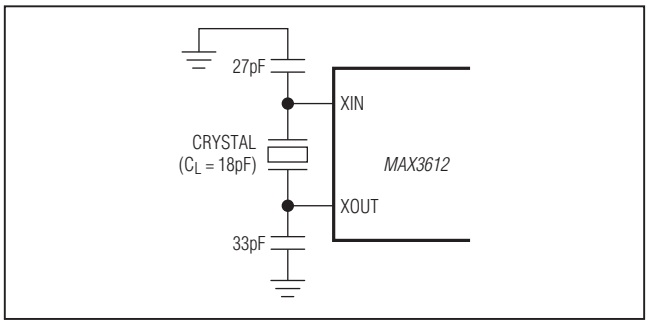


Figure 4. Crystal, Capacitor Connections

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

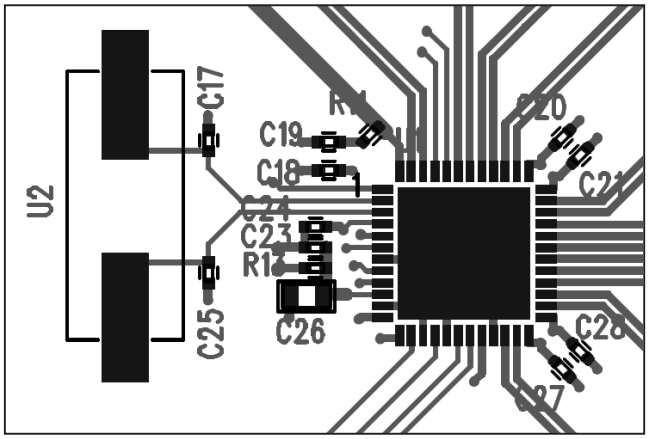


Figure 5. Crystal Layout

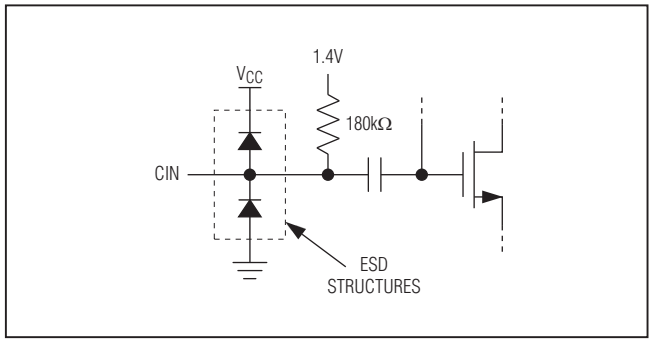


Figure 6. Equivalent CIN Circuit

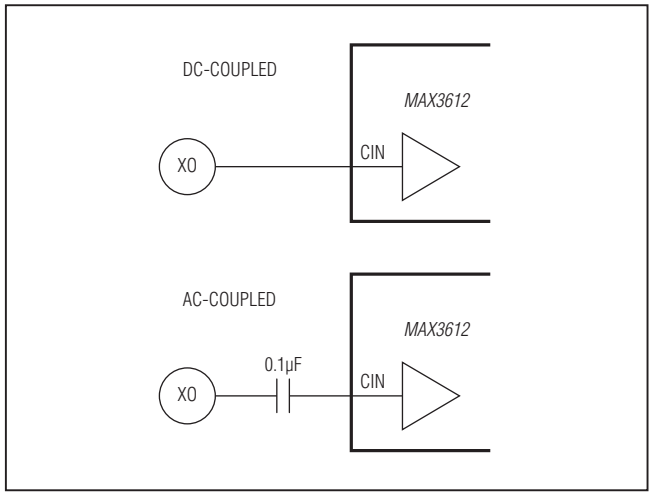


Figure 7. Interface to CIN

Interfacing with LVCMOS Input

The equivalent LVCMOS input circuit for CIN is given in Figure 6. This input is internally biased to allow AC- or DC-coupling, and has 180kΩ input impedance. See Figure 7 for the interface circuit. No signal should be applied to CIN if not used.

Interfacing with Differential Input

The equivalent input circuit for DIN is given in Figure 8. This input operates up to 350MHz and contains an internal 100Ω differential termination as well as a 35Ω common-mode termination. The common-mode termination ensures good signal integrity when connected to a source with large common-mode signals. The input can accept DC-coupled LVPECL signals, and is internally biased to accept AC-coupled LVDS, CML, and LVPECL signals (Figure 9). No signal should be applied to DIN if not used.

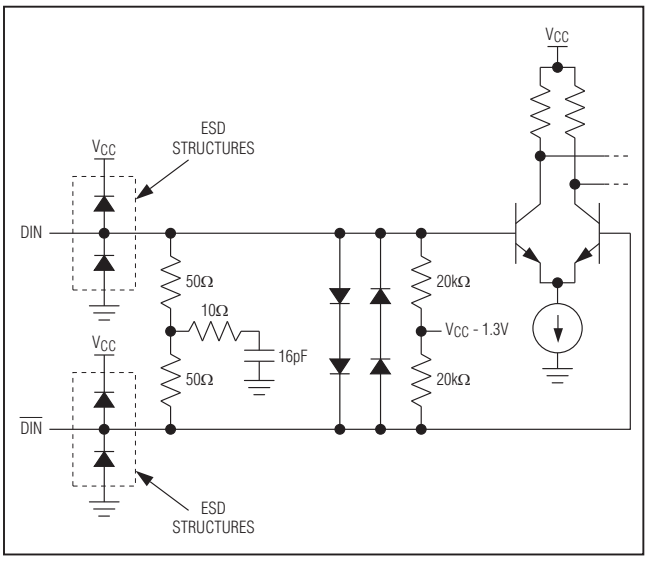


Figure 8. Equivalent DIN Circuit

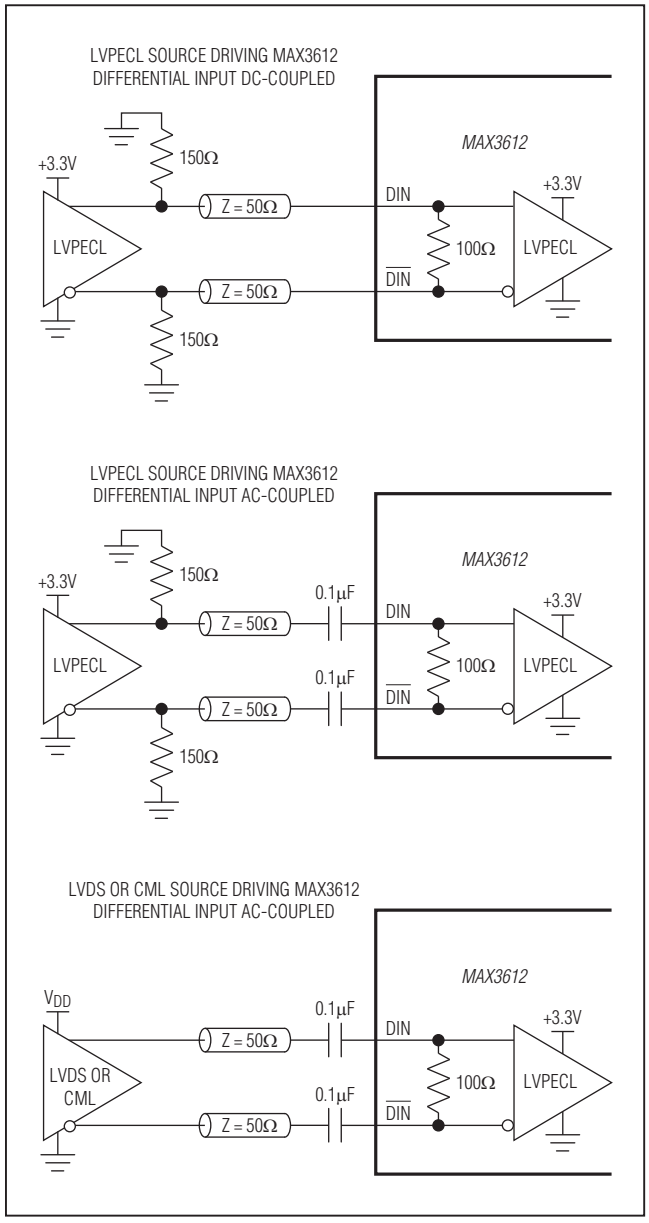


Figure 9. Interfacing to DIN

Interfacing with LVPECL Outputs

The equivalent LVPECL output circuit is given in Figure 10. These outputs are designed to drive a pair of 50Ω transmission lines terminated with 50Ω to $V_{TT} = V_{CC}$ - 2V. If a separate termination voltage (V_{TT}) is not available, other terminations methods can be used such as those shown in Figure 11. For more information on LVPECL terminations and how to interface with other logic families, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

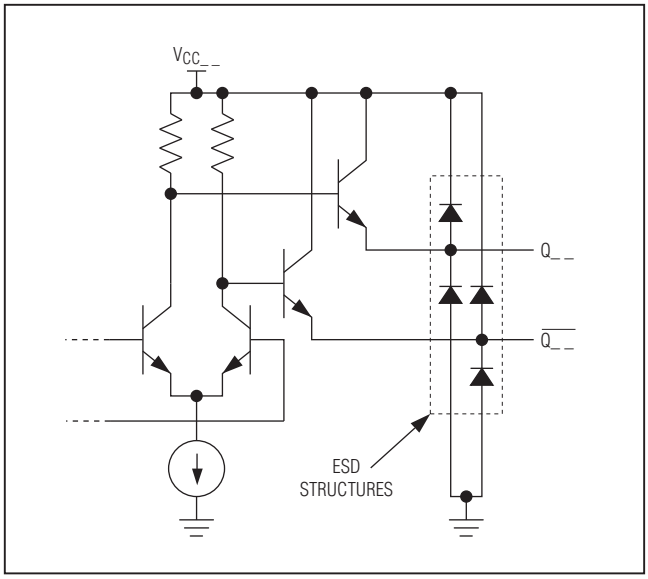


Figure 10. Equivalent LVPECL Output Circuit

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

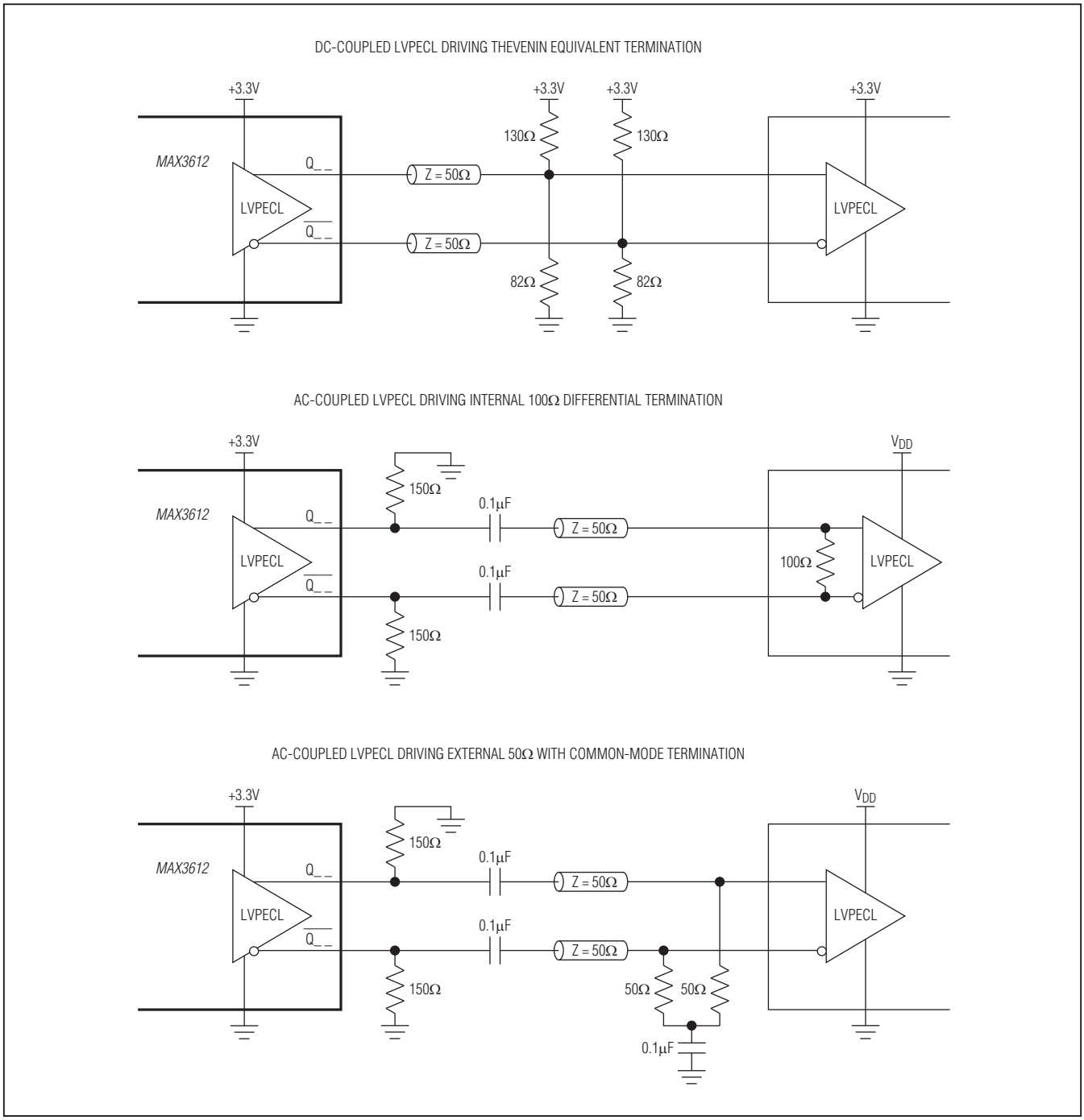


Figure 11. Interface to LVPECL Outputs

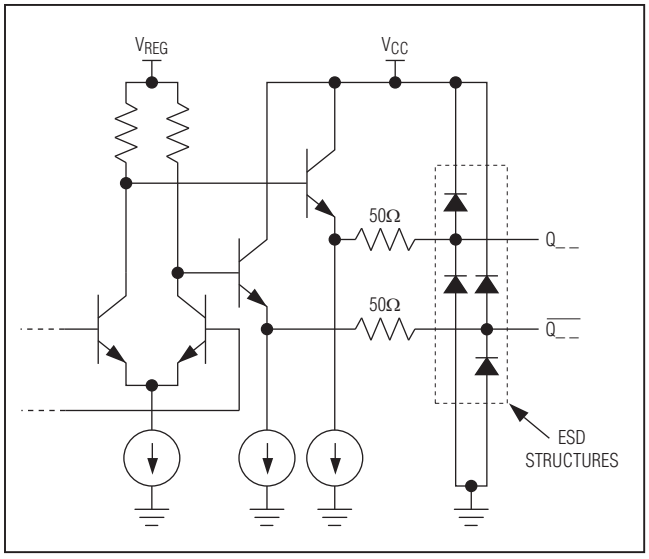


Figure 12. Equivalent LVDS Output Circuit

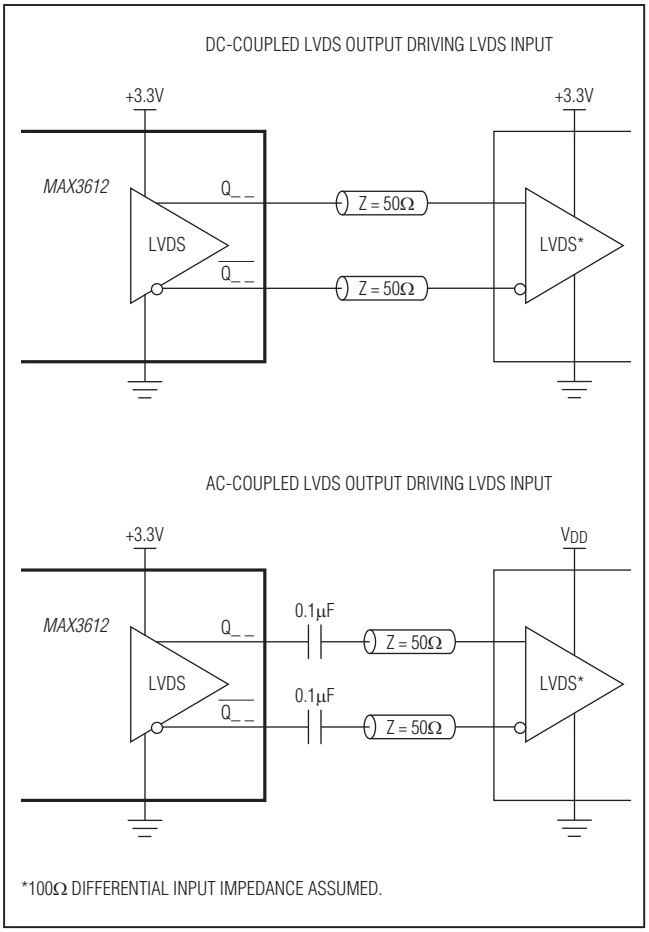


Figure 13. Interface to LVDS Outputs

Interfacing with LVDS Outputs

The equivalent LVDS output circuit is given in Figure 12. These outputs provide 100Ω differential output impedance designed to drive a 100Ω differential transmission line terminated with a 100Ω differential load. Example interface circuits are shown in Figure 13. For more information on LVDS terminations and how to interface with other logic families, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Layout Considerations

The inputs and outputs are the most critical paths for the MAX3612; great care should be taken to minimize discontinuities on the transmission lines. Here are some suggestions for maximizing the performance of the MAX3612:

- An uninterrupted ground plane should be positioned beneath the clock outputs. The ground plane under the crystal should be removed to minimize capacitance.
- Supply decoupling capacitors should be placed close to the supply pins, preferably on the same side of the board as the MAX3612.
- Take care to isolate input traces from the MAX3612 outputs.
- The crystal, trace, and two external capacitors should be placed on the board as close as possible to the XIN and XOUT pins to reduce crosstalk of active signals into the oscillator.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance into and out of the part.
- Provide space between differential output pairs to reduce crosstalk, especially if the outputs are operating at different frequencies.
- Use multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

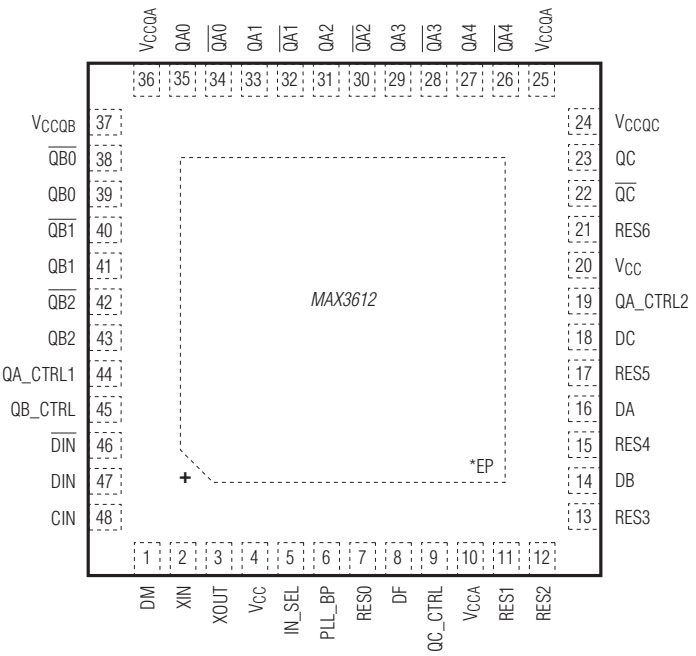
Refer to the MAX3612 evaluation kit for more information.

Chip Information

PROCESS: BiCMOS

Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

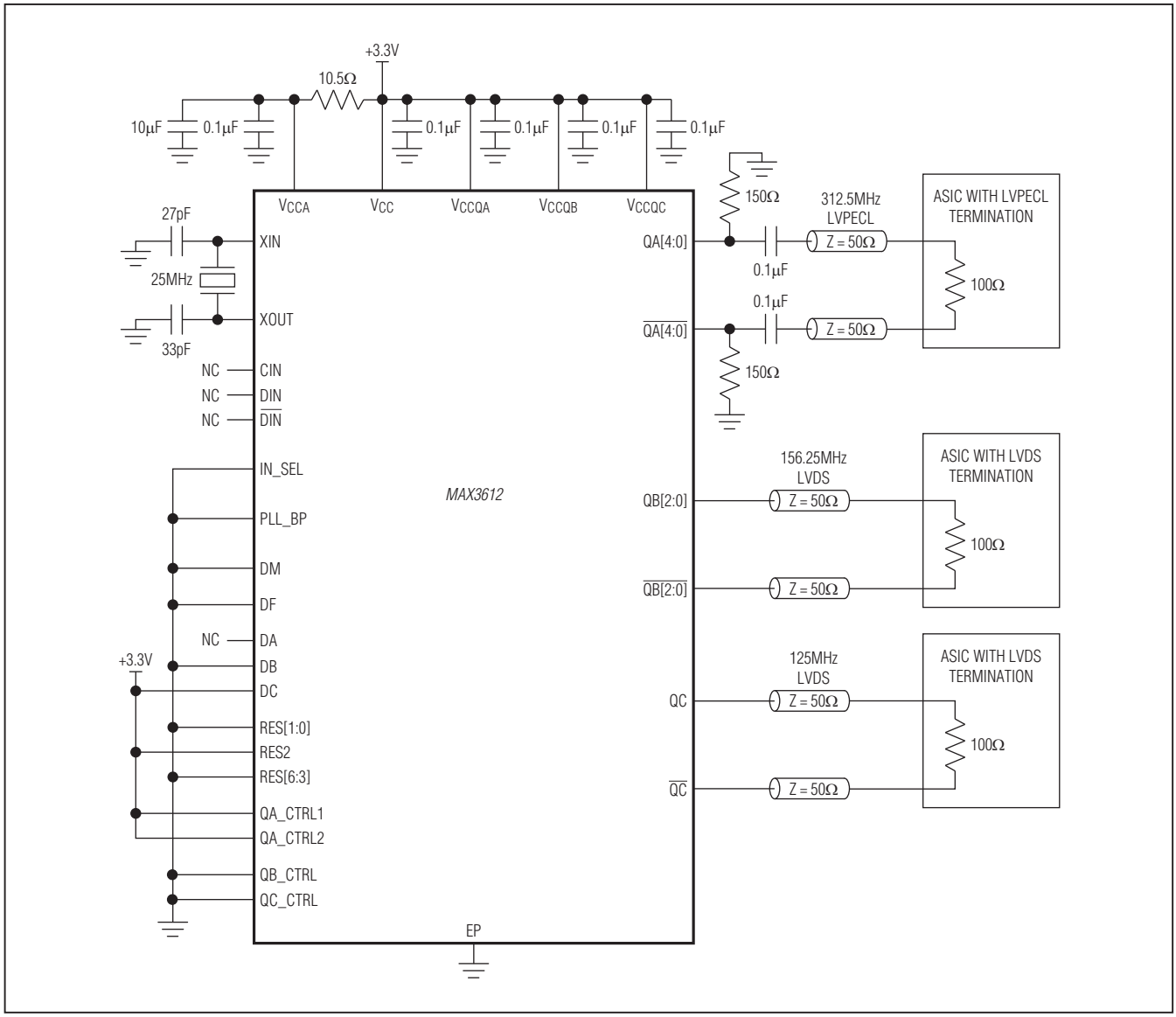
Pin Configuration



THIN QFN
(7mm × 7mm × 0.8mm)

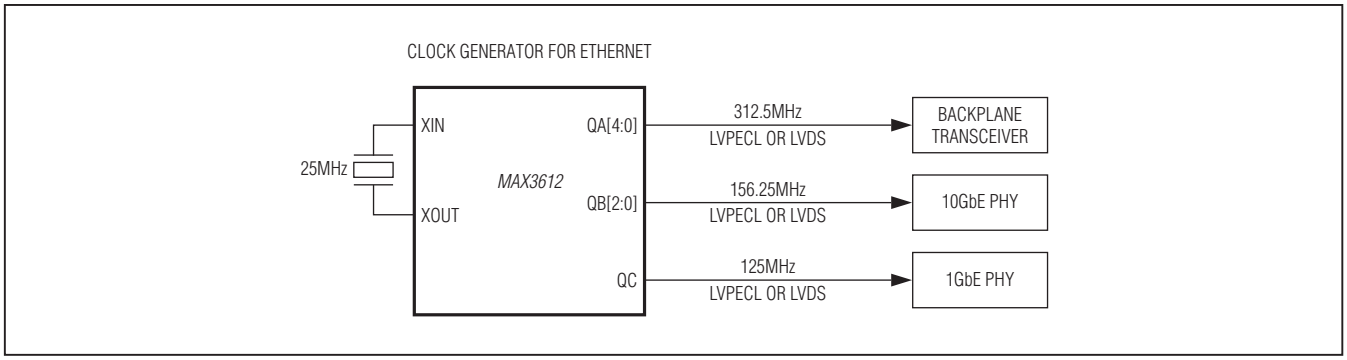
*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

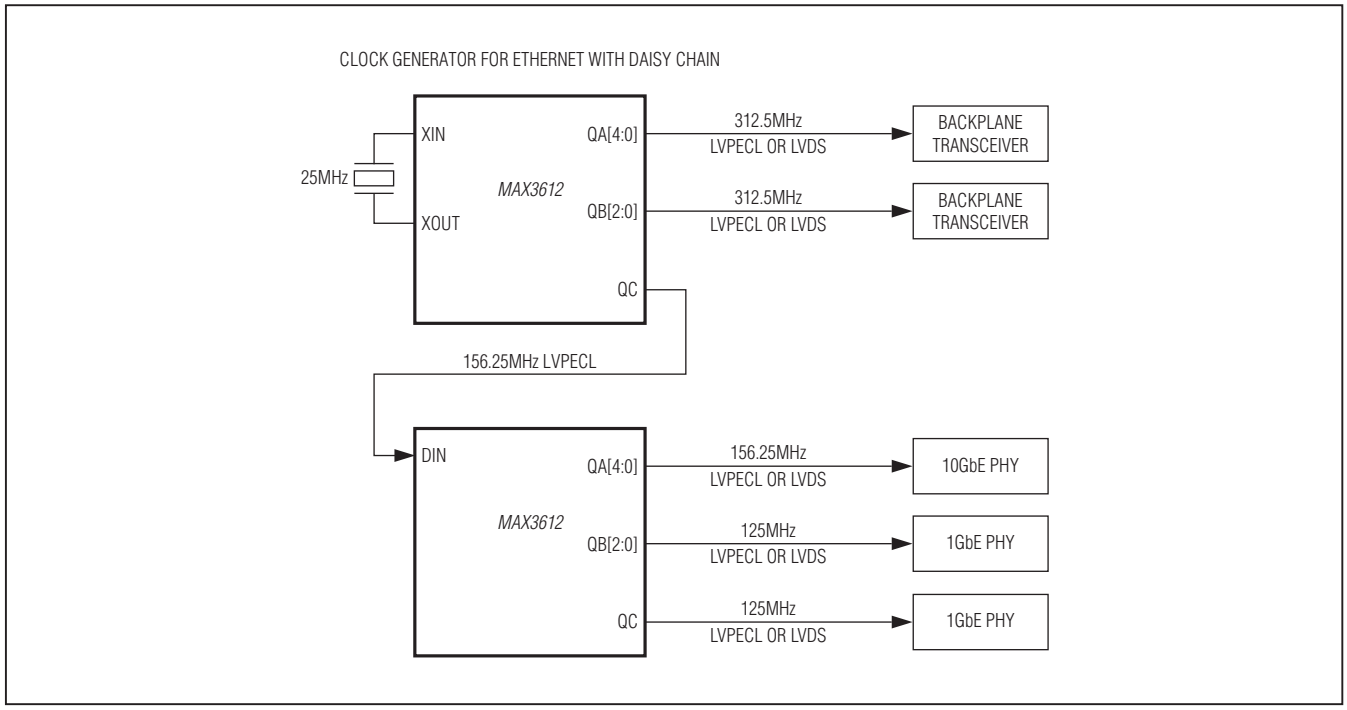
Typical Application Circuits



Low-Jitter Clock Generator with Nine LVDS/LVPECL Outputs

Typical Application Circuits (continued)





Package Information

For the latest package outline information and land patterns, go to **http://www.microsemi.com.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+4	21-0144	90-0130

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/09	Initial release	—
1	6/10	Added the lead and soldering temperatures to the *Absolute Maximum Ratings* section; changed the descriptions in the *Pin Description* table for RES2 (connect to V_{CC}) and RES6 (connect to GND); replaced Figure 5 with customer board layout; revised the RES pin connections to match the *Pin Description* descriptions in the *Typical Application Circuits;* updated the package code and added the land pattern no. to the *Package Information* table	2, 7, 12, 17, 18

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