High Frequency and Paralleling Modules for High Current

GaAs and SiC devices will find more and more use

The inevitable quest for smaller and lower cost systems push the designer to increase the operating frequencies, requiring always faster devices and making paralleling of power modules more difficult.

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Several power modules are often connected in parallel to achieve high output current capable systems.

Semiconductor technology is continually advancing, and ultra fast NPT and PT IGBTs as well as MOSFETs are capable of achieving the higher frequencies required. Most of the standard modules available on the market are designed to address applications where modules can be connected in parallel but switching frequencies remain low. Based upon a 62mm x 108mm standard package well known in the industry as SP6, APT Europe has engineered a full bridge module that can easily be configured as a phase leg by paralleling the two legs together. This low profile, low inductance module is tailored for high frequency operation, and many modules can be paralleled together to provide higher output current without sacrificing electrical performance.

Current asymmetry between modules can be caused either by device parameters or internal and external circuit parasitics. Circuit parasitics include connections between the dice within a module or between the modules themselves as well as between the driver circuit and the power stage.

A static current imbalance can be introduced by a difference in the output characteristic (IC = f(VCE)). The collector to emitter saturation voltage for an IGBT or the drain to source voltage for a MOSFET is the same for all devices once connected in parallel. Thus a difference in the output characteristic leads to a difference of current ΔI_{DC} between devices. Modules with the lowest $V_{CE(sat)}$ at a given current carry a higher share of current than other parallel connected modules. When a device carries more current, its power dissipation and consequently its junction temperature will increase higher than other devices. For transistors like NPT and TRENCH IGBTs or MOSFETs, $V_{CE(sat)}$ positive temperature coefficient (TC) limits the amount of current mismatch because thermal runaway is prevented. The balance in current sharing is more critical with PT IGBT devices having a negative $V_{CE(sat)}$ TC. (This is mainly true at low to medium current. At high current, often at about the rated current, the $V_{CE(sat)}$ TC transitions from negative to positive.)

A direct current imbalance causes variation in switching losses particularly at turn off of the devices. Differences in the transfer characteristics, IC = f(V_{GE}) and ID = f(V_{GS}) contribute also to variation in the static and dynamic losses of the power semiconductors.

The spread of delay and switching times also causes a problem of current sharing and generates higher switching losses. Both output and transfer characteristics are sensitive to temperature and influence current sharing. Dice within the same manufacturing lot exhibit a narrower distribution of parameters. Therefore, variation is minimized by utilizing dice from the same manufacturing lot in a module.

Loop inductance in the power circuit is a key factor to ensure good dynamic paralleling of the power devices. It must be as low as possible to minimize the voltage overshoot at device turn off.

The impedance of the driver seen by each module must be the same. Since the gate drive circuit itself is very low impedance, not much noise can couple into it directly unless it has a large loop area or there is capacitive coupling to a noise source. Feedback between the gate and drain/collector can result in oscillation, especially cross-coupled feedback between paralleled devices. Imbalance in gate drive impedance can result in asymmetrical switching. Individual gate resistors provide damping, which eliminates or at least reduces oscillation. Individual gate resistors also somewhat isolate the gates of each device from each other, reducing cross-coupling. In addition to gate resistors, ferrite beads added to each gate wire can be very effective at preventing oscillation

Fig.1 shows the electrical diagram of power modules connected in parallel. It is best to use a common gate driver for all paralleled modules because gate signals are synchronized (uniform propagation delay for each gate). Individual gate drivers for each module will insert some variation in turn-on and turn-off delay times, which would add to the switching times of the devices. It is however possible to parallel power devices and their associated drivers if the differences in delay times are negligible. It is usual practice to adjust turn-on and turn-off switching times mainly to minimize the stress applied to free wheeling diodes and keep over-voltages under control. This can be achieved by implementing separate turn-on and turn-off gate resistors, which is easily done if the driver circuit offers separate outputs. Gate resistors of the same value are distributed to each power device, and a matching return source resistor Re permits driving each power device input in a differential mode that helps compensating negative effects of possible differences in transfer characteristics between modules. Main common resistors can be placed on the driver if the multiple gate and source return resistors are not sufficient. It is imperative to parallel modules with same part number and issued from same production lot. This will ensure that all devices will exhibit the lowest spread of characteristics.

A perfectly symmetrical layout of both the driver and the power circuit must be adopted to minimize all loop inductances. All modules will preferably be mounted on the same heat sink to achieve the best possible thermal coupling. The modules need to be spaced apart on the heat-sink to use the maximum of its surface, avoid hot spots, and optimize heat sink cooling performance. Once all these steps are implemented, it is reasonable to obtain 80% to 90% of the total current capability of the each module. As the operating frequency of the system increases, the impact of the parasitic elements becomes more significant than at lower frequency, and all

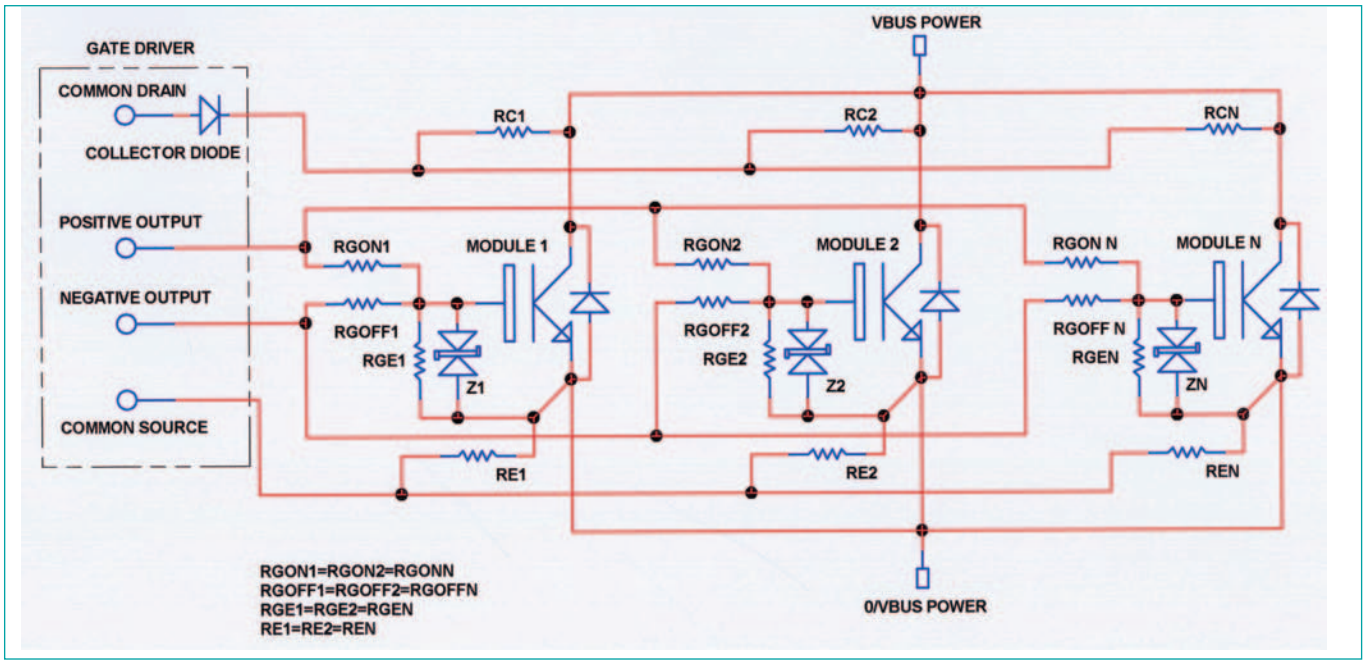

Figure1. Recommended circuit for parallel connection of power modules.

recommendations described above must be rigorously applied. It makes sense to take great care with the external parallel conditions, assuming that internal parallel wiring of the dies within the module is already optimized.

The limitations of existing standard modules are explained in the following. An example has been taken of a standard module with 62mm x 108mm, well known in the industry, used to offer phase legs both with IGBT and MOSFET technologies. Many of these modules are used in parallel to achieve high current systems.

Looking at the internal layout and control signal loop reveals some significant differences in the way each of the top and bottom switches are driven. Some significant differences in the control signal loop also exist at the same switch level between all the dice that are paralleled together.

First of all, as shown on Fig. 2, gate and emitter control pins are on the same side of the module, leading to a much longer control current path for the bottom switch. In most cases, internal gate and source connections are made by wires, and the same wire length is used both for top and bottom switches. This matches control signal loops but introduces a significant level of parasitic inductance that limits the operation of the module to low frequency. Such inductance in the gate path makes noise immunity a real concern when power devices used are from a very fast type, resulting in difficulty maintaining the switches off (due to dV/dt induced turn-on), even with high value of negative gate bias. Oscillations induced by the combination of gate inductance and device input capacitance are difficult to cancel except with high gate resistor values that do not allow utilizing the full performance of the fast devices.

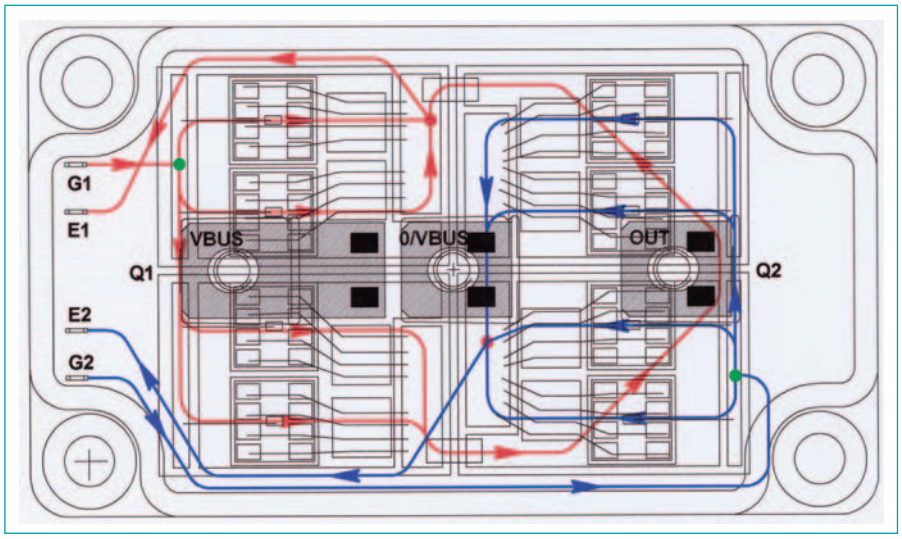

Figure 2. Relative gate-emitter loops of each cell of top and bottom switches.

Another concern is relative to the gate-emitter loop at the level of the power semiconductors. Fig. 2 also describes the relative gate-emitter loops of each cell of top and bottom switches. Each cell is made of two dice in parallel. One can see that the signal loop is the shortest for dice located on the top left substrate while it is very long for the ones located on the bottom left substrate.

Figure 3. APTE SP6 Full bridge modules greatly facilitates modules parallel connection.

The dice mounted on these two substrates are supposed to operate in parallel while the gate control signal loop of the bottom left substrate has to go all along the two right substrates to reach the module source return terminal. A less but still very significant loop imbalance is also observed on bottom switch Q2. If this works in an acceptable manner up to a few kHz, the parasitic inductances will significantly reduce performance and introduce major switching loss asymmetries between parallel connected dice as switching frequency increases. It is still possible to improve the module layout by taking the source return connections directly on the top of the dice, but the physical distance forced by pin-out location makes it impossible to reduce the total loop length.

APT Europe has engineered a module based on the same SP6 footprint where each cell of a given switch has an independent gate control signal. Each cell is located on its own substrate, and perfect symmetry of the cell design within the module makes the parallel connection of several modules straight-forward. This approach leads naturally to transforming the original phase leg configuration into a full bridge construction.

Fig. 4 shows the electrical diagram of the module with the associated control signal loops. External gate and emitter return sharing resistors are used according to best practice of paralleling of the two switch cells together. The other major improvement consists of placing control gate and source control terminals on both ends of the module; each pair of connectors is placed as close as possible to the power cell it is dedicated to drive, as shown on Fig. 5.

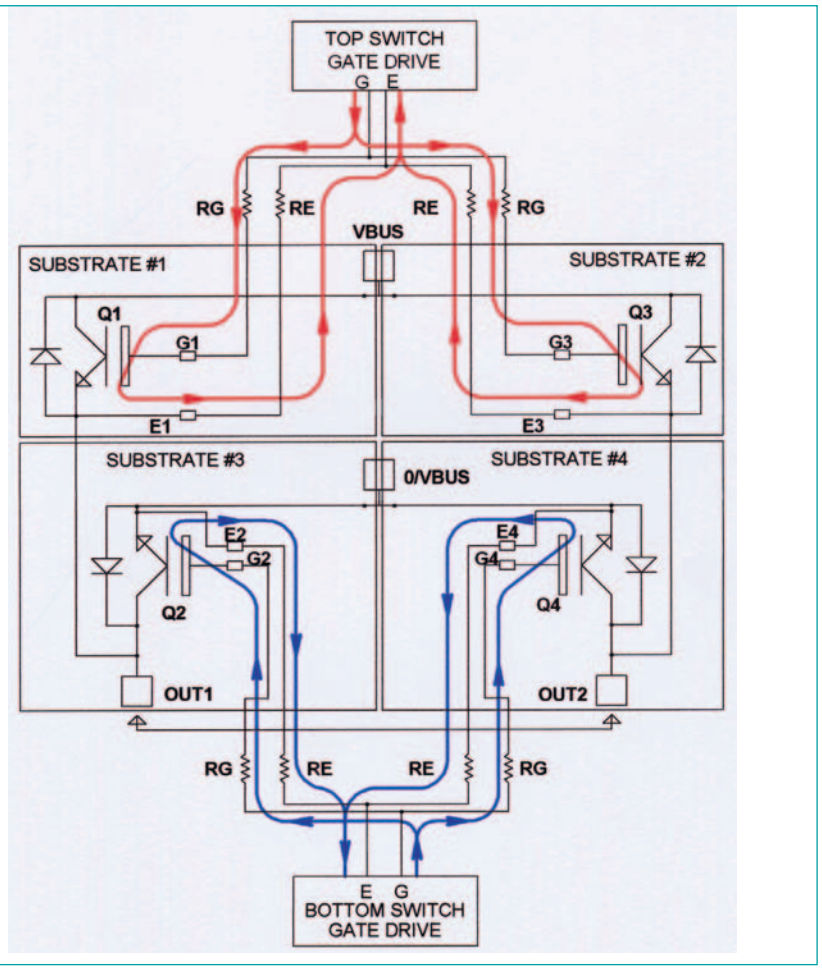

Figure 4. Electrical diagram of the module with the associated control signal loops.

The length of the gate and emitter connections is not only significantly reduced, but connecting the cells together reduces gate loop inductance by a ratio of two. In this way, the control loop of each cell becomes perfectly symmetrical, both for top and bottom switches. Such a module can be used as a full bridge, but it becomes a component of choice when parallel connection of modules is required to reach high current capability. Paralleling full bridge modules is performed the same as for paralleling the two legs of the same device. Each die of each cell incorporates a series gate resistor, either integrated at die level as is often the case with IGBTs, otherwise it is laid out on the substrate. For MOSFET operation in the range of 400kHz and above, it also makes sense to integrate inside the module a source return resistor for each die (instead of only for each cell) to further improve dynamic performance, starting from the elementary die to all modules switches in parallel. Such a configuration can be easily realized, starting from the standard design.

Being only 17mm in height (instead of 30mm for industry standard modules), the SP6 module has a very low profile and offers significant reduction in parasitic inductance and resistance of the power circuit. This is one of the conditions that allows taking full advantages of very fast devices such as ultra fast NPT and PT IGBTs and the fastest APT Power MOS 7 MOSFETs without any problems with over-voltage spikes at device turn off. Laminated bus bars offering excellent coupling between VBUS and VBUS return are highly recommended to supply the module or several modules in parallel. Filtering electrolytic capacitors are very often sepa-

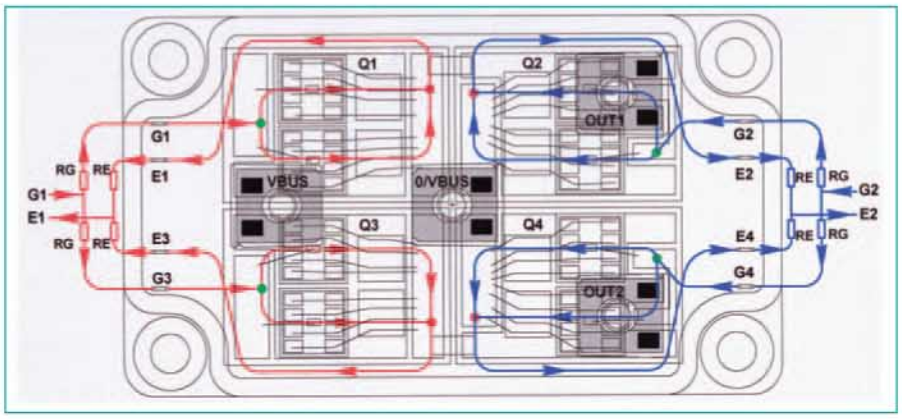

Figure 5 each pair of connectors is placed as close as possible to the power cell.

rate from the assembly, and polypropylene or any other fast type capacitors like multilayer ceramic must be distributed on each module, as close as possible to the power supply terminals to compensate the small inductance loop introduced by the bus bar network.

The SP6, low profile full bridge module is the best choice of component for power assemblies requiring modules to be connected in parallel, especially when high frequency operation in the range of several hundreds of kHz is specified. This module is available with ratings from 100V to 1700V and 50A to 200A using MOSFET and IGBT technologies. This module construction enables driving the ultra fast devices at high speed, and the parasitic elements are low enough to not require slowing down either turn-on or turn-off speeds for safe operating area considerations. Upon request, junction to case thermal resistance can be improved using DBC on aluminium nitride (AIN) substrates. Keeping power dissipation the same, this will decrease junction temperature for better long term reliability or will simply allow 25% more power dissipation at the same operating junction temperature. An aluminium silicon carbide (AlSiC) base plate instead of copper can also be specified to enhance reliability and reduce the weight of the system. Matched temperature coefficient of expansion (TCE) from silicon devices down to the base plate provides minimum stress within the materials assembly and ensures a very good behaviour of the module over wide range of temperature shocks and power cycling. For application in the high frequency range, silicon carbide (SiC) Schottky barrier diodes further decrease switching losses and improve overall system performance.

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