

Figure 2.

If a linear curve of  $\Delta f/\Delta V = 150$  kHz/volt is drawn, values of  $C_s$  which are both very large (.01 $\mu$ F) and very small (56 pF) result in deviations from this straight line which are not equal at 3.0 and 8.0 volts. The result of this is to produce more second harmonic distortion. By trial and error, a  $C_s = 120$  pF which produced a deviation from linearity of about 53 kHz at both 3 and 8 volts was found. If less distortion is desired, the modulating signal can be corrected before applying it to the VCO or a smaller voltage can be used to produce the 75 kHz deviation. The measured distortion of this VCO is 1.2% and the required audio level was 362 mV RMS.

In order to demonstrate the effect of lowering the required audio level necessary to produce the required deviation, consider the circuit in Figure 3:

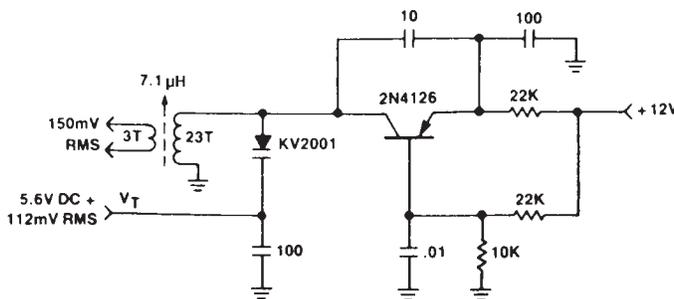


Figure 3.

Measured distortion of this VCO is less than .03% at 75 kHz deviation, and its tuning curve from 3 to 8 volts is shown in Figure 4.

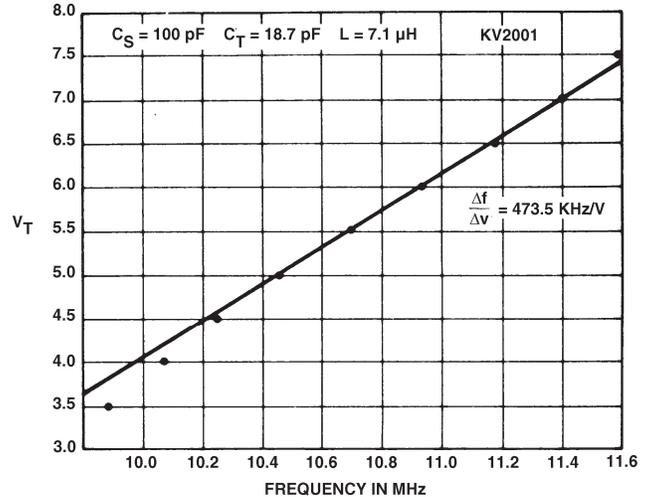


Figure 4.

It is important to keep the RF AC signal across the diode as low as possible since distortion will increase if it is too high. If higher levels such as is necessary to drive passive phase detectors are desired, two back-to-back diodes in series should be used to tune the coil.

## 10.7 MHz WIDE BAND DETECTOR:

As was mentioned in the introduction, a PLL FM detector can easily be constructed using a quadrature detector IC such as the CA3089E and one of the linear VCOs described previously. These ICs contain a high-gain limiting amplifier plus a phase detector which has an external input which is usually connected to some kind of phase-shifting circuit. In this case, the VCO is connected to the phase detector and the audio output pin is the VCO control voltage., Figure 5 shows one possible configuration:

# Application Notes

$K_d = 1.05 \text{ V/RAD}$   
 $K_o = 2.975 \times 10^6 \text{ RAD/SEC/V}$   
 $K_d K_o = 3.124 \times 10^6 \text{ SEC}^{-1}$   
 $\omega_n = 456 \times 10^3 \text{ FN} = 73 \text{ KHz}$   
 $\zeta = .5$   
 $\text{PULL IN} = \pm 275 \text{ KHz}$   
 $\text{HOLD IN} = \pm 389 \text{ KHz}$

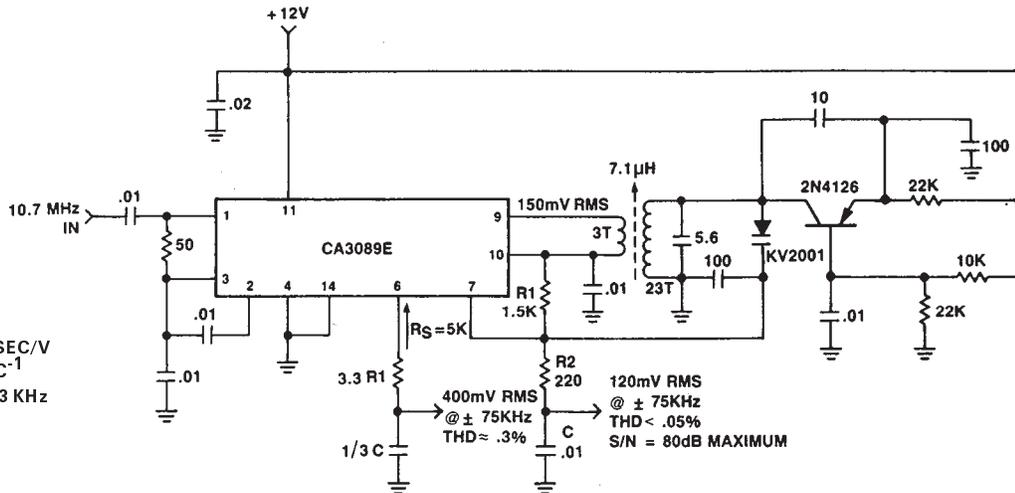


Figure 5.

In this application, the AFC output of the phase detector from pin 7 is used as the audio output. An alternate output from pin 6 can be muted using the mute input pin of the CA3089. It is a current source with a constant of 700  $\mu\text{A}/\text{radian}$ . A load of 1.5 K ohms gives it a  $K_d$  of 1.05 volts/radian. The oscillator in Figure 3 has a sensitivity of 473.5 kHz/volt giving a  $K_o = 2.975 \times 10^6$  radians/second/volt. Thus  $K_d K_o = 3.124 \times 10^6$ . Since  $K_d K_o$  and  $R_1$  (1.5 K ohms) is known,  $R_2$  and  $C$  can then be calculated to give the desired loop parameters: (See reference 2 for more detailed analysis.)

$$R_2 C = 2\zeta / \omega_n - 1/K_d K_o$$

$$R_1 C = K_d / K_o / \omega_n - R_2 C$$

$\zeta$  = loop damping factor

$\omega_n$  = loop natural frequency

It should be noted that the mute signal output of the IC cannot be used because it relies on a variable level signal into pin 9 for its operation, and the pin 9 signal is now the constant output of the VCO. Also, the signal appearing at pin 6 is now an amplified version of the signal at pin 7. The amplitude relationship is the ratio of the 5000 ohm resistor from pin 6 to the internal reference on pin 10 to  $R_1$ . Thus, it is 3.33 times as large and its distortion is larger because of non-linearities inside the IC.

## NARROW BAND FM DETECTORS:

If the detector for commercial FM signals in Figure 5 were to be used for FM communications signals, its output would be only 6.7 mV RMS for 5 kHz deviation. This could easily be amplified, but it would be better to redesign the oscillator to increase the detected output level. At first, it may seem that a hyperabrupt diode is not necessary for this application, but it has an advantage in that large values for  $C_s$  or  $C_t$  can be used to make the tuned

circuit relatively insensitive to diode capacitance drift and distortion will be acceptable.

Two approaches can be used for this design; Either  $C_s$  can be small or  $C_t$  can be large. The first step is to determine what audio output level is desired and then to design the VCO to have the desired frequency versus voltage slope.

let  $V_{out} = 100 \text{ mV RMS}$  for  $\Delta f = \pm 5 \text{ kHz}$

$$V_{peak} = 141 \text{ mV}$$

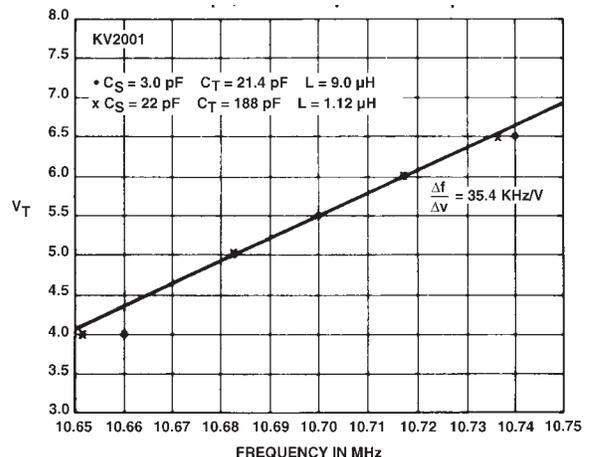
$$\Delta f / \Delta V = 35.46 \text{ kHz/V}$$

$$K_o = 222 \times 10^3$$

Since the deviation is small, the lowest capacitance diode, the KV2001 should be used. Assuming we want the frequency to be 10.7 MHz at a tuning voltage of 5.5 volts, the calculator program gives:

$$\text{If } C_s = 3.9 \text{ pF, } C_t = 21.4 \text{ pF, } L = 9.04 \mu\text{H}$$

$$\text{If } C_s = 22 \text{ pF, } C_t = 188.1 \text{ pF, } L = 1.124 \mu\text{H}$$



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Either of these will work, but as can be seen from Figure 6, the one with  $C_s = 22$  pF will give the lowest distortion.

Figure 7 shows the circuit used for the demodulator. The signal-to-noise improvement due to the loop bandwidth of only 3 kHz is substantial; With only 100 microvolts into

the CA3089, the output S/N is 57 dB. This is where a PLL detector can offer a big improvement over a non-synchronous detector; Since the modulating signal has a limited bandwidth, the PLL detector can be designed to have a narrow bandwidth to improve receiver sensitivity.

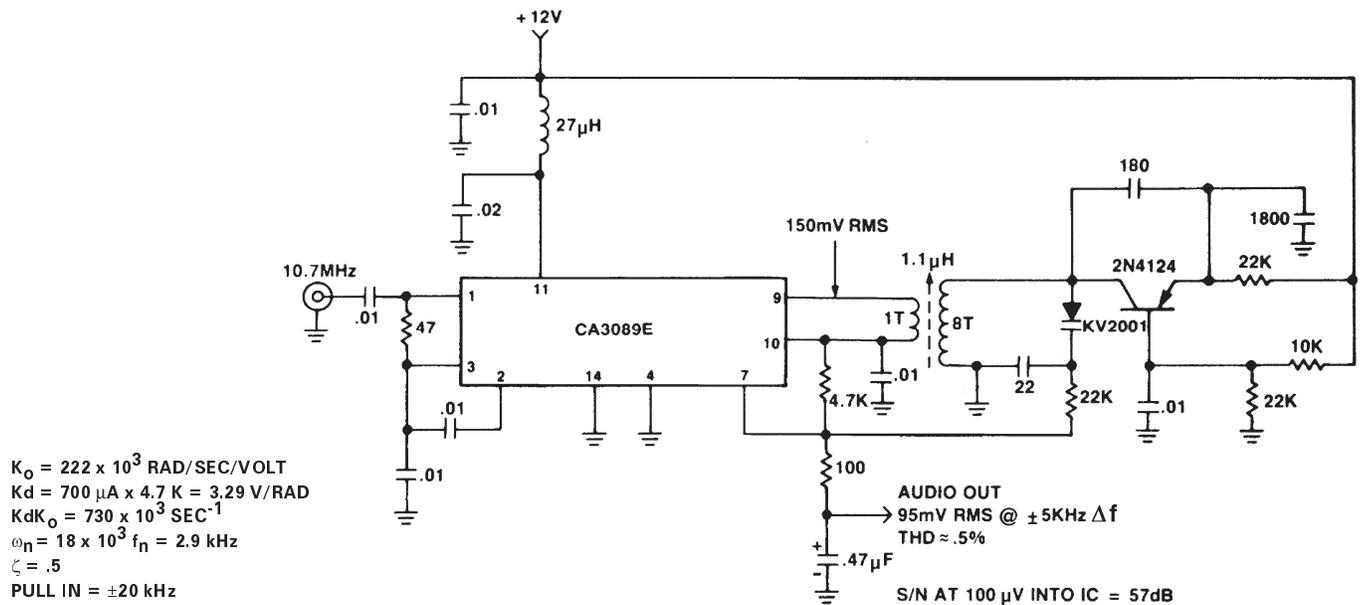


Figure 7.

## 21.4 MHz DETECTOR:

21.4 MHz is also a commonly used IF frequency for communications equipment, and a PLL detector for this frequency can be built just as easily as for 10.7 MHz. If we let the audio output level be 100 mV RMS for  $\pm 5$  kHz deviation, the loop constants and components will remain the same as in the 10.7 MHz case.

thus:  $\Delta f/\Delta V = 35.36 \text{ kHz/V}$

Using the KV2001 diode at 5.5V, we get:

if  $C_s = 3.9$  pF,  $C_t = 46$  pF and  $L = 1.12$   $\mu\text{H}$

The same coil as was used in the previous example can be used here. However, the distortion will be higher because a smaller  $C_s$  has been used. Figure 8 demonstrates this effect:

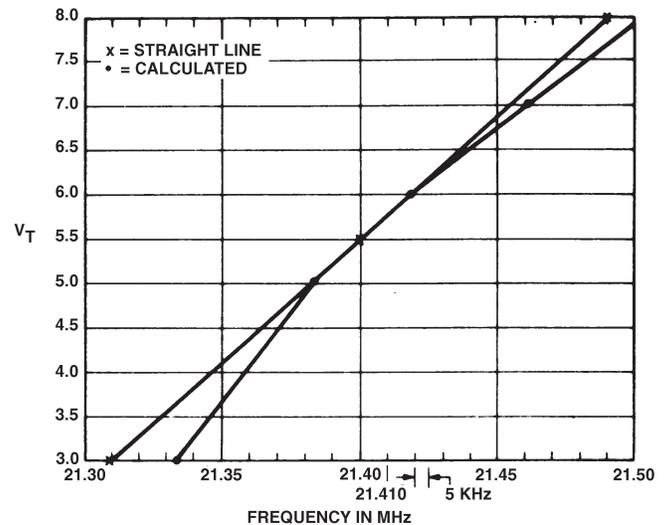


Figure 8.

# Application Notes

The measured distortion using this VCO was about 2%. This can be reduced by making a simple change in the circuit: The VCO is first designed using a convenient coil size and capacitors which will give acceptable distortion. In a case like this where the deviation is very small, the required tuning voltage deviation for the VCO will be very small, but since the loop gain is much greater than

is needed, the output of the phase detector can be reduced with a resistive divider. The result is that the output of the phase detector is increased by the attenuation of the resistive divider, and this can be set to a desired level.

Figure 9 shows the circuit used and the measured results:

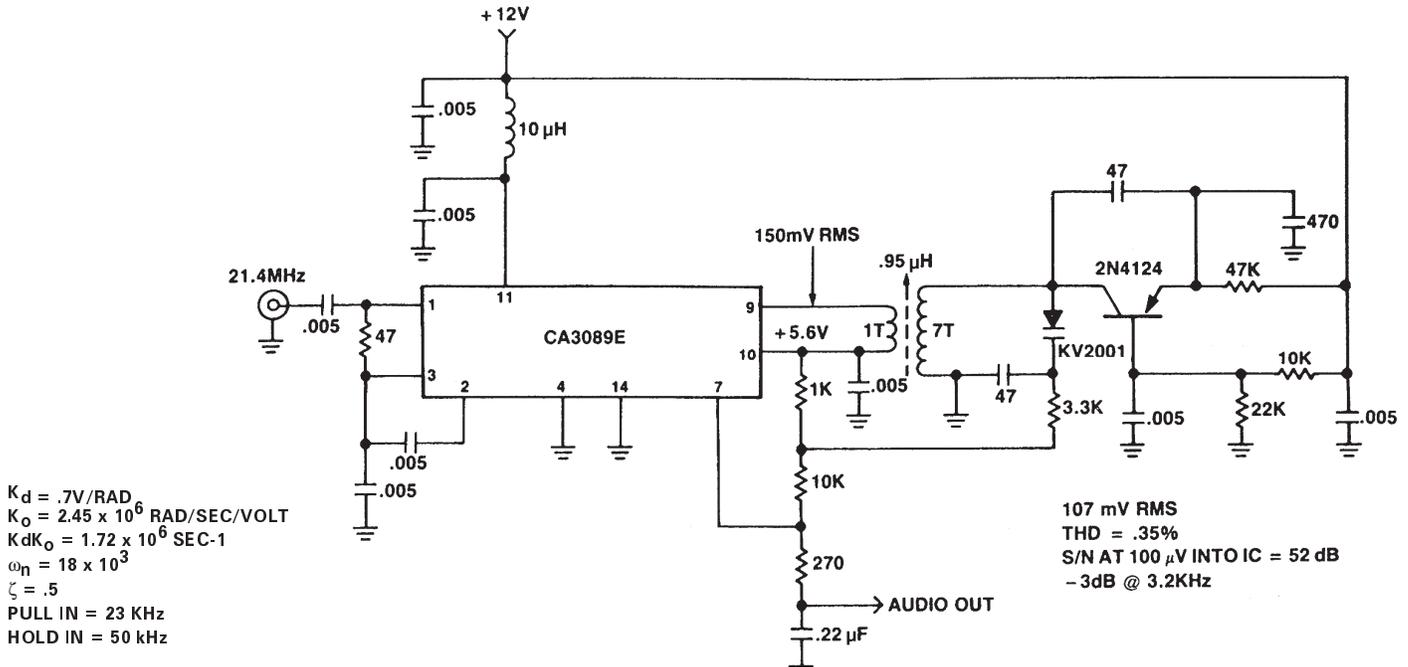


Figure 9.

## 70 MHZ SATELLITE RECEIVER DETECTOR

Many receivers for consumer and commercial satellite TV or telecommunications reception have a 70 MHz IF frequency. The signal is FM with a  $\pm 10.25$  MHz deviation and the modulating frequencies extend up to 8.0 MHz because some sound carriers are this high. The detector should at least be flat up to the highest video frequency of about 4 MHz, but it can attenuate the sound carriers somewhat. The most difficult requirement is to make a VCO which is linear over this range and which can be modulated at a rate of 10 MHz or more. This is not difficult if hyperabrupt tuning diodes are used:

let:  $f_o = 70 \text{ MHz}$        $\Delta f = 10.25 \text{ MHz}$   
 $f_{min} = 59.75 \text{ MHz}$        $f_{max} = 80.25 \text{ MHz}$

Because the VCO modulation frequency response must be so high, it would be quite difficult to drive the large Cs which would be necessary in a single diode oscillator. Therefore, two back-to-back diodes are used here. Also, it would be difficult to obtain a range of 3 to 8 volts out of a phase detector, so the oscillator should be designed to cover the range with a minimum voltage swing. This

requires keeping Ct as low as possible, and so the feedback for the oscillator should be produced with either inductive coupling or a tap on the oscillator coil. Figure 10 shows one possibility:

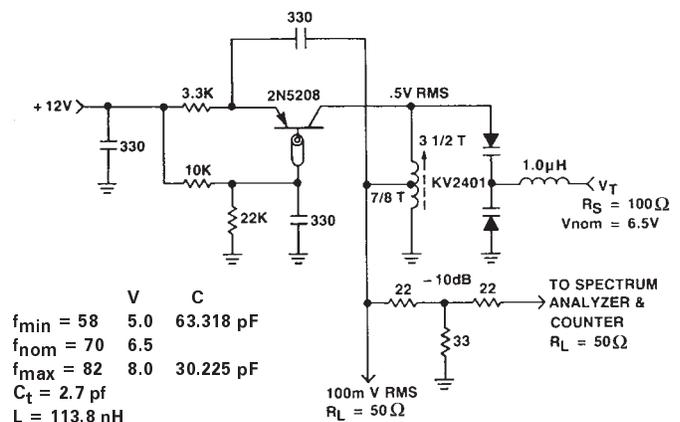


Figure 10.

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The stray capacitance in this circuit is only about 3 pF.

The first design used 6.0 V as the center tuning voltage, but the calculated curve of frequency versus voltage shows that the linearity is better above about 5.5 V, so the oscillator was designed to be centered at 6.5 V.

Therefore:  $V_{\min} = 5.0 \text{ V}$   $f_{\min} = 58 \text{ MHz}$   
 $V_{\text{nom}} = 6.5 \text{ V}$   $f_{\text{nom}} = 70 \text{ MHz}$   
 $V_{\max} = 8.0 \text{ V}$   $f_{\max} = 82 \text{ MHz}$

Using two KV2401 diodes in series:

$C_{\min} = 30.335 \text{ pF}$   $C_{\max} = 60.318 \text{ pF}$   
 $C_t = 2.7 \text{ pF}$   $L = 113.8 \text{ nH}$

Measured and calculated curves are shown in Figure 11:

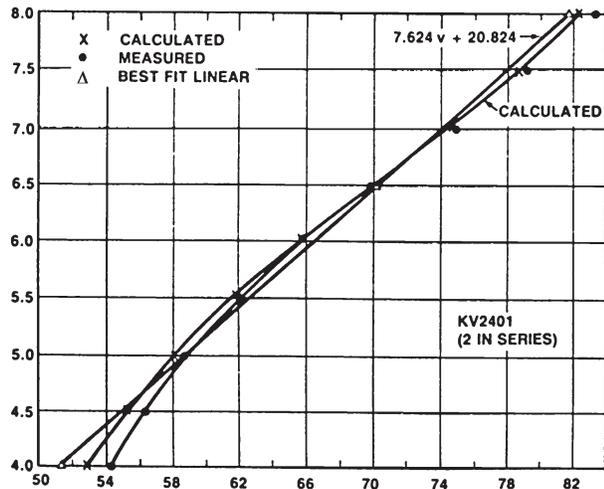


Figure 11.

The slope of the linear approximation gives:

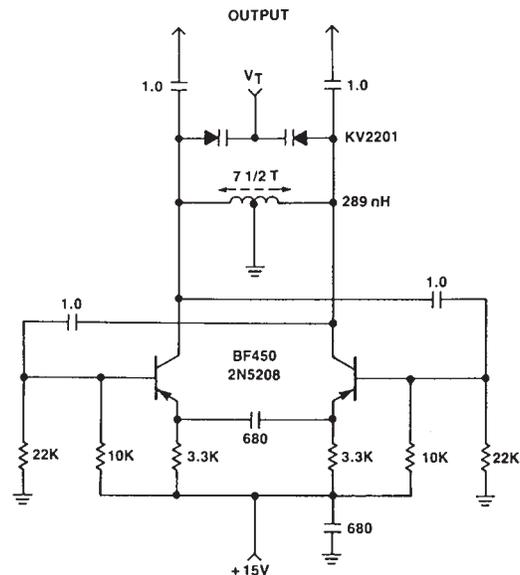
$$\Delta f / \Delta V = 7.62 \text{ MHz/V}$$

$$K_o = 47.9 \times 10^6 \text{ rad.sec/V}$$

With a 50 ohm load on the oscillator, the output level varies less than 1 dB from 58 to 82 MHz. Note that a 10 dB pad has been inserted at the oscillator output. This isolates the connecting cables from the spurious resonances of the coil tap. The combination of the cable and the variable tap impedance can cause relatively large amplitude variations over the tuning range. Another important point is that the tap is relatively high on the coil. This loads the coil heavily so the impedance changes and diode Q changes have less effect on the oscillator output level as it changes frequency. Because of this high coil loading, the second harmonic is relatively high (-20 dB) but the AC voltage at the transistor collector is only 500 mV RMS.

Note that the modulating source sees the diodes in parallel, so it must drive a capacitive load of about 128 pF at 5.0 V. Thus, its output resistance must be less than 155 ohms if the modulation frequency response is to be less than -3 dB at 8 MHz. Also, care must be taken in selecting the value of the 1.0  $\mu\text{H}$  coil between the diode cathodes and the modulation source. If it is too large, it will form a resonant circuit with the two diodes in parallel. If it is too small, the resistance of the modulation source will load the tuned circuit and may stop the oscillator.

Unfortunately, the VCO in Figure 10 is fine for generating signals, but it cannot be used for a VCO in a wideband PLL because the poles produced by the LC combination of the 2 parallel diodes and the input coil prevent construction of a stable loop with a frequency response greater than a few hundred kilohertz. The easiest way to eliminate this inductor would be to use a push-pull oscillator. Since the hyperabrupt diodes are very well matched and produce linear frequency excursions, it is possible to build a push-pull circuit which can be arranged to produce a very small component of the fundamental AC signal at the center tap of the coil and tuning diodes. Figure 12 shows one possibility:



KV2201  
 $C_4 = 50 \text{ pF}$   $C_{\min} = C_8 = 9.75 \text{ pF}$  (2 IN SERIES)  
 $C_{\max} = C_5 = 20.43 \text{ pF}$   
 $f_{\min} = 60 \text{ MHz}$   
 $f_{\max} = 80 \text{ MHz}$   
 $C_t = 3.9 \text{ pF}$   $L = 289 \text{ nH}$

MEASURED RESULTS:  
 70 MHz = 6.43 V  
 60 MHz = 5.1 V  
 80 MHz = 7.8 V

Figure 12.

# Application Notes

The coil is tuned with two cores instead of one so they can be adjusted to produce a null in the fundamental frequency of the oscillator at the cathodes of the tuning diodes.

Using this approach solves two problems: The first is elimination of any matching requirement for the diodes. The second is the problem of locating the exact center-tap of the coil. In this application, a coil tuned with an adjustable core was used, and the tap location would change with the placement of the core if two were not used. The final design used an upright molded coil which could be adjusted from the top and bottom of the PC board.

Since this oscillator produces a balanced output, it seems logical to use a balanced phase detector for the rest of the PLL. Unfortunately, this presents some problems which were mentioned previously; The phase detector sees two diodes in parallel (approximately 82 pF

at 5V) so its output impedance must be less than about 40 Ohms so this RC pole does not affect the loop too much. If a low output phase detector is followed by an amplifier, the combination must have a frequency response of DC to almost 100 MHz depending on the number of poles in the amplifier. This is difficult to construct, because it requires several stages, and the overall combination introduces so many poles that the loop cannot be made stable. A better approach is to construct a high output voltage, low output impedance phase detector operating at high current but most integrated phase detectors (LM1496, S042P) are designed for low current (less than 10 mA) operation. Matched discrete devices could be used, but this is not considered practical here. The CA3054, ULN2054 dual differential array can, however, be operated at high currents and, while it requires quite a few external components, it works quite well as a double balanced phase detector. Figure 13 shows the final arrangement:

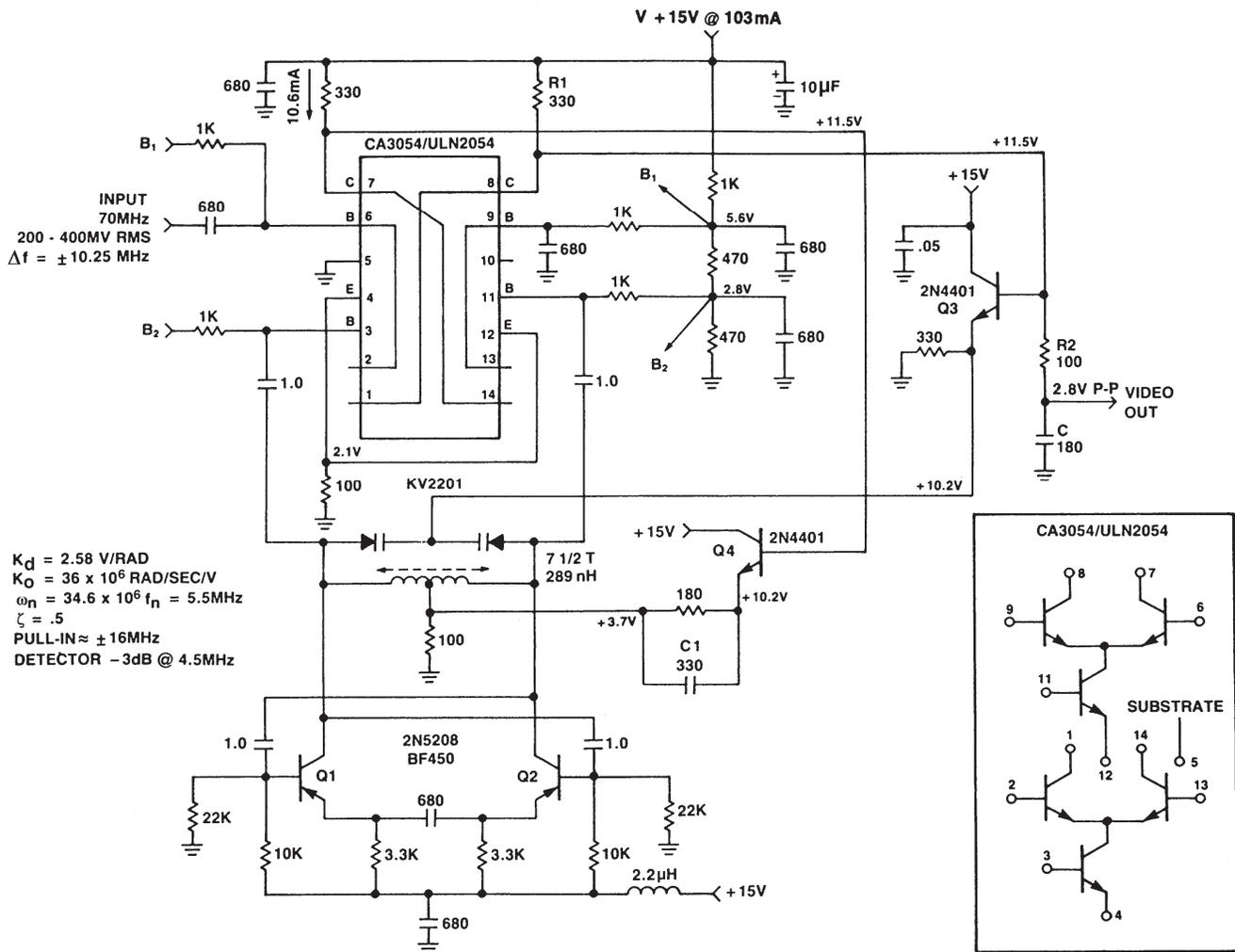


Figure 13.

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Note that the center tap of the coil has been brought up to 3.7 volts so that, at 70 MHz, the voltage across the diodes is 6.5 V. An adjustable voltage divider could be used for this instead, but the other output of the phase detector has been used here. The additional loop gain increases the pull-in range and eliminates the need for any set-up adjustments except for the initial adjustments of the coil cores to set the center frequency. The best way to adjust them seems to be with a swept input signal. Observe the emitter of Q3 and adjust for the best looking discriminator response and minimum residual 70 MHz.

Using the values shown, the detector produces a 2.8 V P-P video signal and has a -3 dB output frequency response of 4.5 MHz. Note that the detector video output can be taken from the emitter of Q3 or across the loop filter capacitor C. (see reference 2). The output across C is free of 70 MHz signals and is quieter than that at the

emitter of Q3, but care must be taken not to load C. Capacitor C1 has been added to correct for phase shifts which prevent the loop from following high modulation levels at high frequencies when the natural frequency of the loop is only 5.5 MHz. It may be possible to omit this depending on how much the received signal is pre-emphasized.

## 140 MHz SATELLITE RECEIVER DETECTOR

The 70 MHz PLL demodulator can easily be changed to operate at 140 MHz by changing a few values. The tuning coil is changed to 131 nH and KV2001 diodes are substituted for the KV2201 devices. The loop gain changes to  $137.9 \times 10^6$ , so the loop filter is changed, and bypass capacitors can be reduced to avoid possible resonances. Figure 14 shows the result:

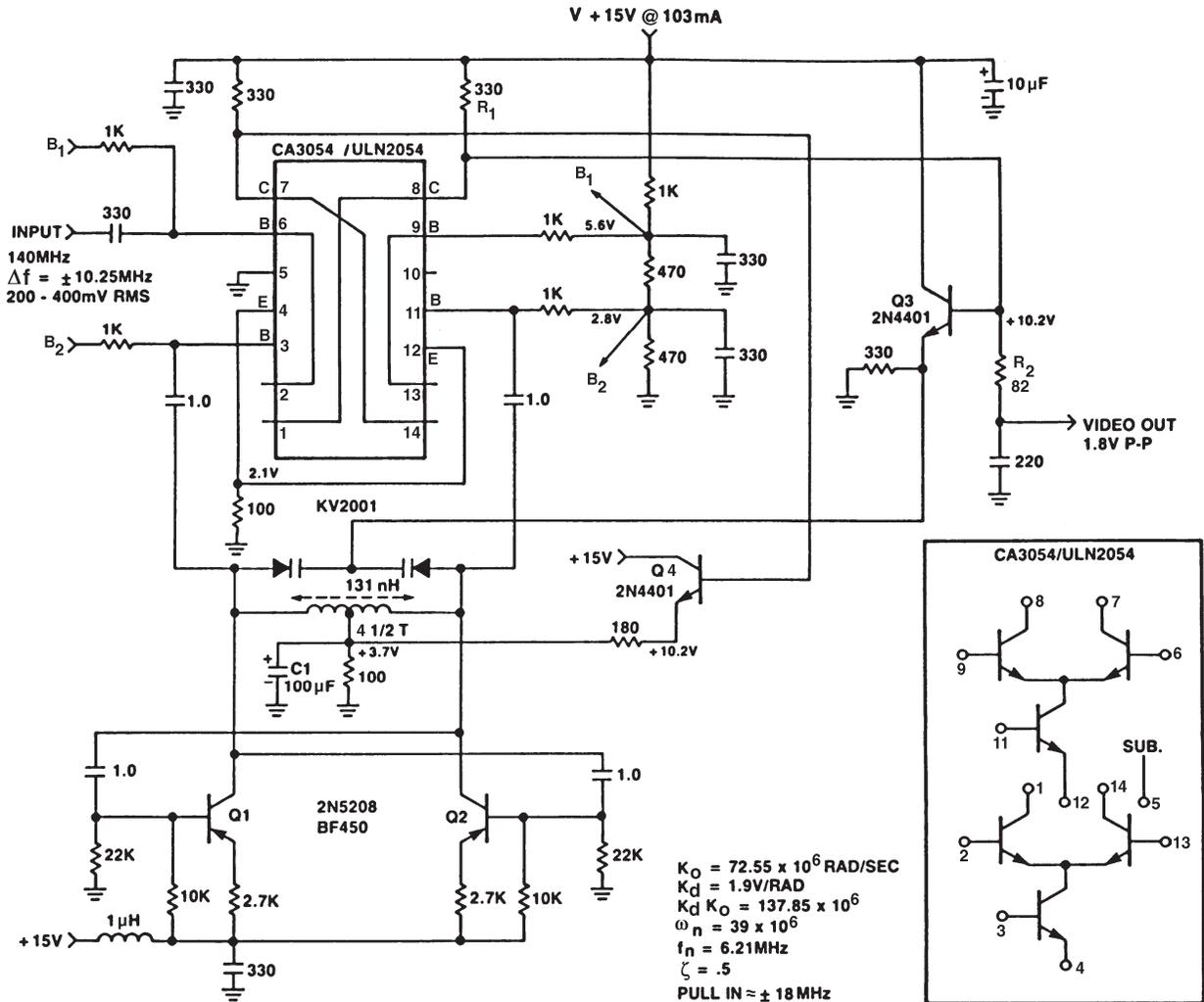


Figure 14.

# Application Notes

The opposite phase channel with Q4 and its associated components has been bypassed with C1 to increase the video output level and because its gain is not needed. Linearity is slightly better than that of the 70 MHz unit because of the smaller percentage change in the center frequency.

## 300 MHz SATELLITE RECEIVER DETECTOR

Some satellite receivers have a 300 MHz IF frequency, so it would be advantageous to demodulate the FM signal without having to mix it down to a lower frequency. This is not difficult because of the ease of constructing linear VCOs with hyperabrupt tuning diodes:  $f_{min} = 290$  MHz,  $f_{max} = 310$  MHz. The tuning range should be easy to accomplish, so a single diode oscillator with a small Cs can be used. Let  $C_s = 22$  pF, and consider the following circuit:

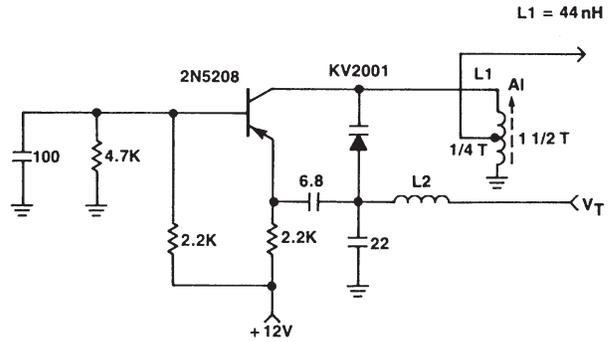


Figure 15.

40 nH is about the smallest inductance which can be obtained with a standard molded coil with an adjustable core, so this oscillator was actually designed around this inductance. The actual coil has 1 1/2 turns and a

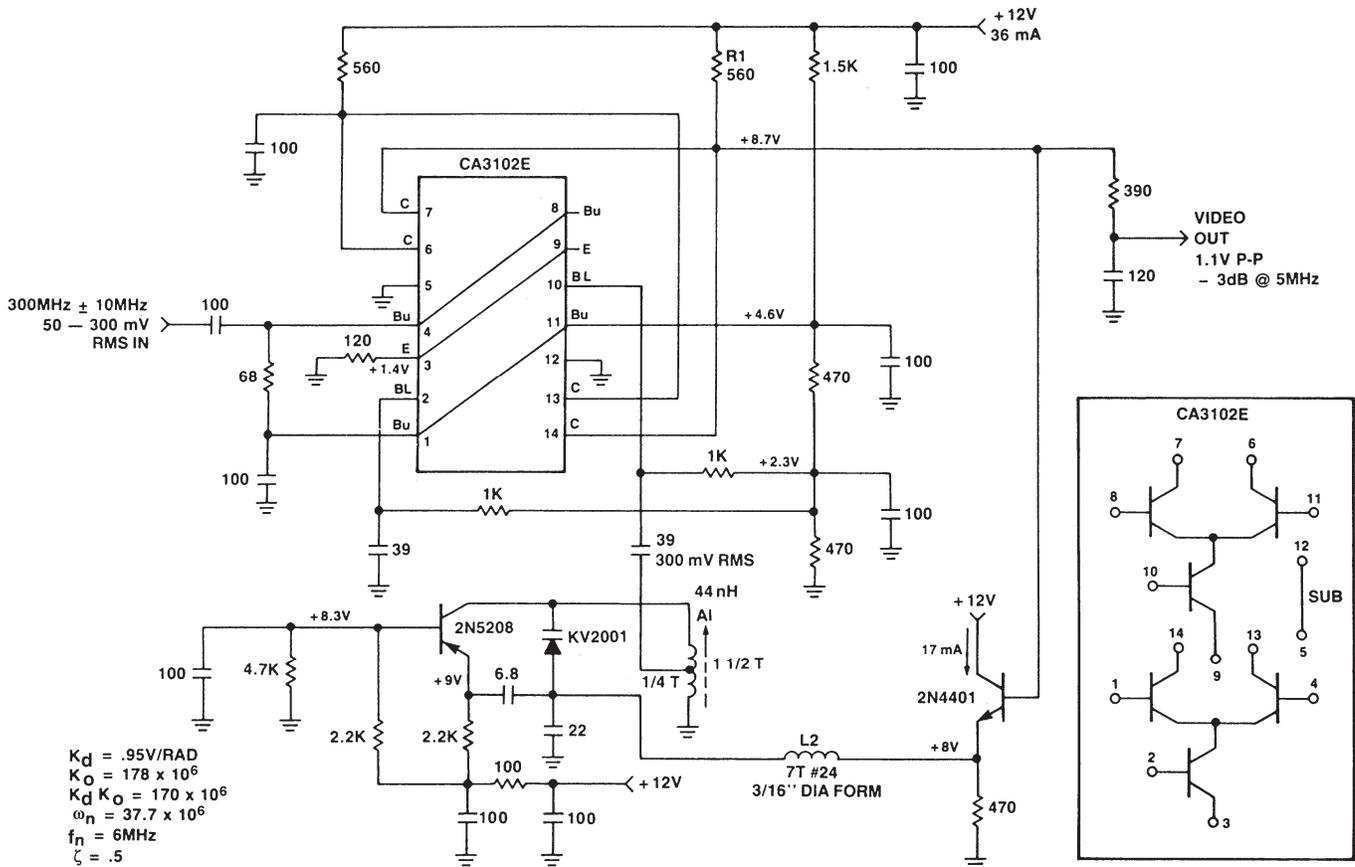


Figure 16.

10-32 x 5/16 inch aluminum core. Feedback is taken from the 22 pF capacitor and the output is from a 1/4 turn tap on the coil.

The choice of phase detectors for 300 MHz is somewhat limited. We do not want to use an amplifier between the VCO and phase detector because of the stability problems mentioned earlier, so a detector with a least  $\pm .5$  V output is needed. A high level balanced mixer would work, but they are expensive and require +17 dBm (1.58 V RMS) LO drive, so an amplifier after the oscillator would be required. The CA3054 IC used previously will not work at 300 MHz, but the RCA CA3102 will. It also consists of two differential amplifiers usable to 500 MHz, and they are also connected here to be a double balanced phase detector. The resulting circuit shown in Figure 16 is very similar to the ones used for 70 and 140 MHz except that a push-pull oscillator is not needed because the operating frequency is much higher than the modulating frequency, an a small inductance, L2, can be used to isolate the VCO from the low impedance of the emitter follower driving it.

Also, the capacitance which the phase detector must drive is relatively low because a small  $C_s$  can be used and the KV2001 capacitance is low. The result is that the 300 MHz PLL is somewhat easier to construct than the lower frequency loops.

The tuning voltage in the 300 MHz detector in Figure 16 is centered around 8.0 V. This was chosen to keep the collector voltage in the CA3102E as high as possible while having a small value for R1 and a tuning voltage for the KV2001 low enough to be approximately in its linear frequency versus voltage range. The result shown in Figure 17 is that, while the detector linearity is good, it tends to have the characteristic upward curvature at higher frequencies.

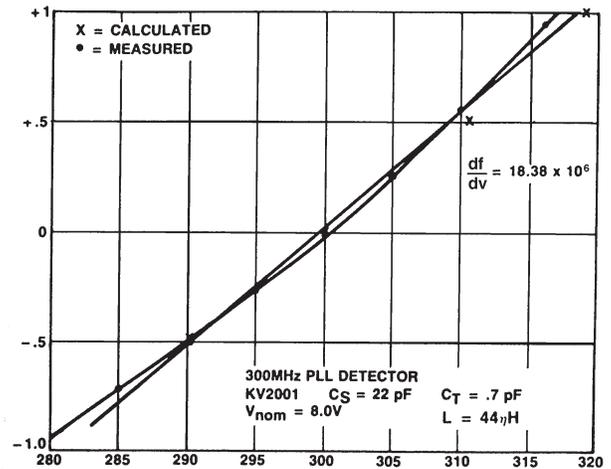


Figure 17.

While this would be acceptable for most applications, it can be improved by operating the KV2001 around 6.5 V. Figure 18 shows another 300 MHz PLL in which this has been done using two diodes in the oscillator. It could also be done with one diode as in the previous example, but the resulting coil would be too small to use an adjustable molded coil and therefore adjustment of the center frequency would be more difficult. If a small series capacitor were used with one diode, calculations show that the required tuning voltage range increases, and the detector becomes nonlinear again. Thus, using two diodes seems to be the best approach. Feedback for the oscillator is now taken from the coil tap and C2 across the 100 ohm resistor has been added to improve the phase response of the loop.

# Application Notes

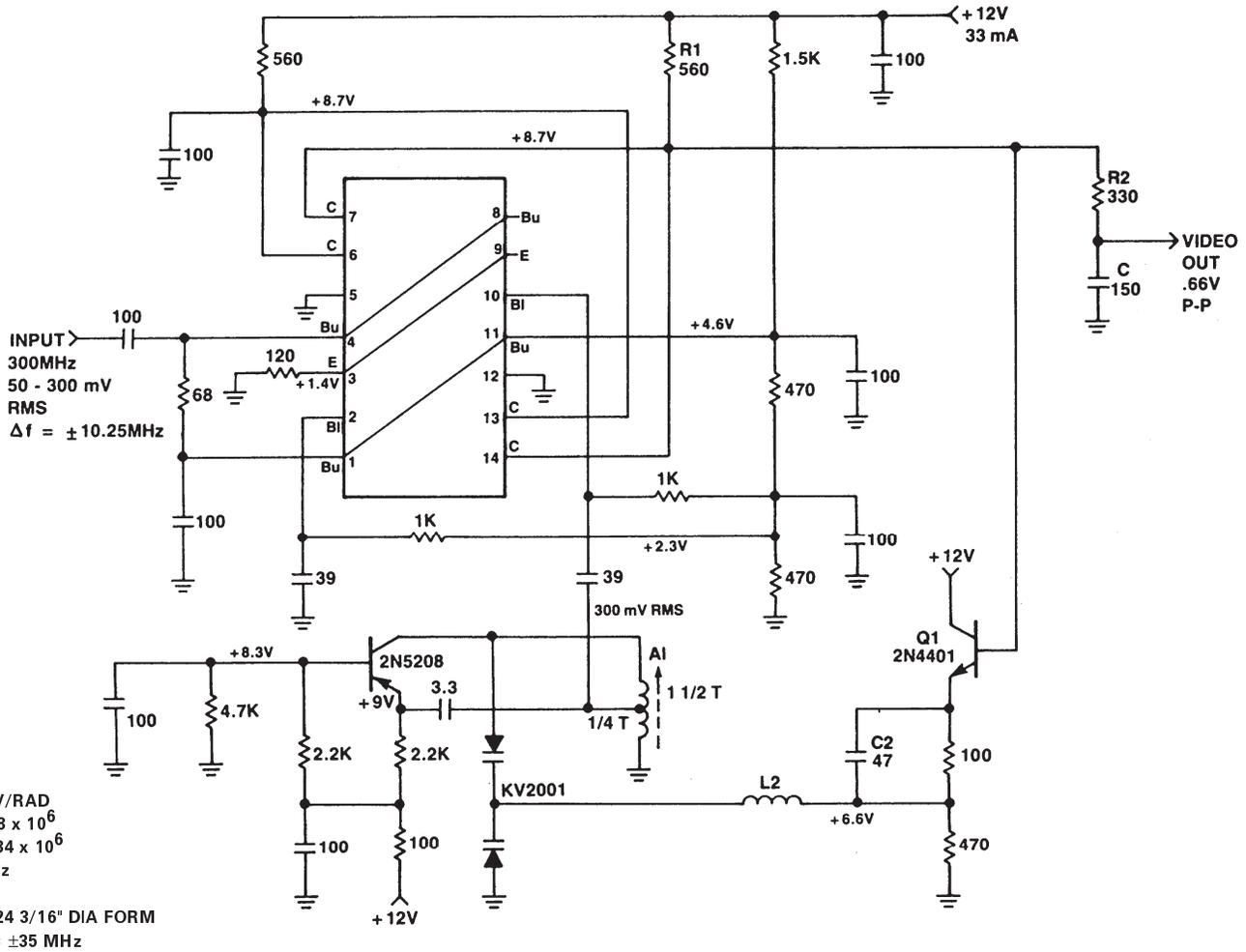


Figure 18.

Figure 19 shows the excellent results obtained. If desired, the linearity can be improved further by adding a potentiometer to the 120 ohm resistor on pins 3 and 9 of the CA3102E to adjust the center tuning voltage of the KV2001.

Note that the video output level of this detector is lower than that in Figure 15 because of the higher sensitivity of the VCO. A video amplifier such as the LM359 could be used to increase this to a desired level as well as to perform other functions like de-emphasis and elimination of the energy dispersal component of the modulated signal.

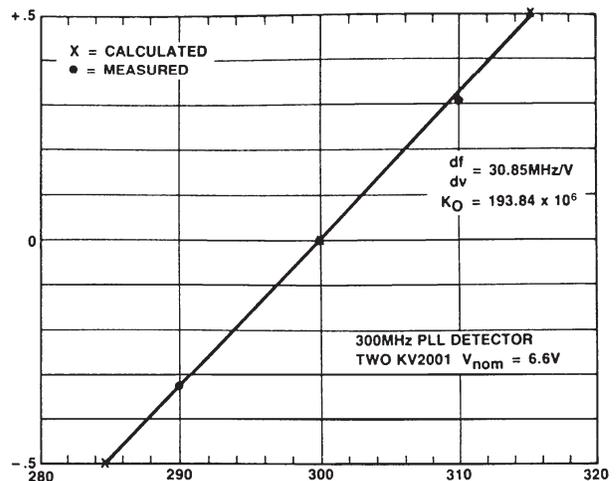


Figure 19.

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## SATELLITE TV SOUND DEMODULATOR

Satellite TV sound signals employ FM modulated sub-carriers between approximately 5.4 and 8.0 MHz. The most commonly used frequencies are 6.8, 6.2 and 7.4 MHz, and most receivers use a standard quadrature detector sound demodulator IC for this application. When the received signal contains multiple sound channels, a separate demodulator is used for each sound channel since it is difficult to tune a quadrature detector.

Much better and more versatile performance can be achieved with a PLL detector using a VCO tuned with hyperabrupt diodes for the following reasons:

1. The loop locks on the desired signal and its output distortion is almost independent of tuning errors.

2. The detector can be voltage tuned to any desired sound channel.
3. The PLL detector offers a signal-to-noise improvement over quadrature detectors and this particular detector has much better signal-to-noise than the available IC phase locked loops.
4. The loop has some inherent selectivity, so less pre-selection at the input is required.

The sound demodulator could be made to operate at a fixed frequency, but for this case, it would simply be a shifted frequency version of the 10.7 MHz detector discussed earlier.

In order to more fully utilize the capability of the hyperabrupt tuning diode, a tunable detector has been designed and is illustrated in Figure 20.

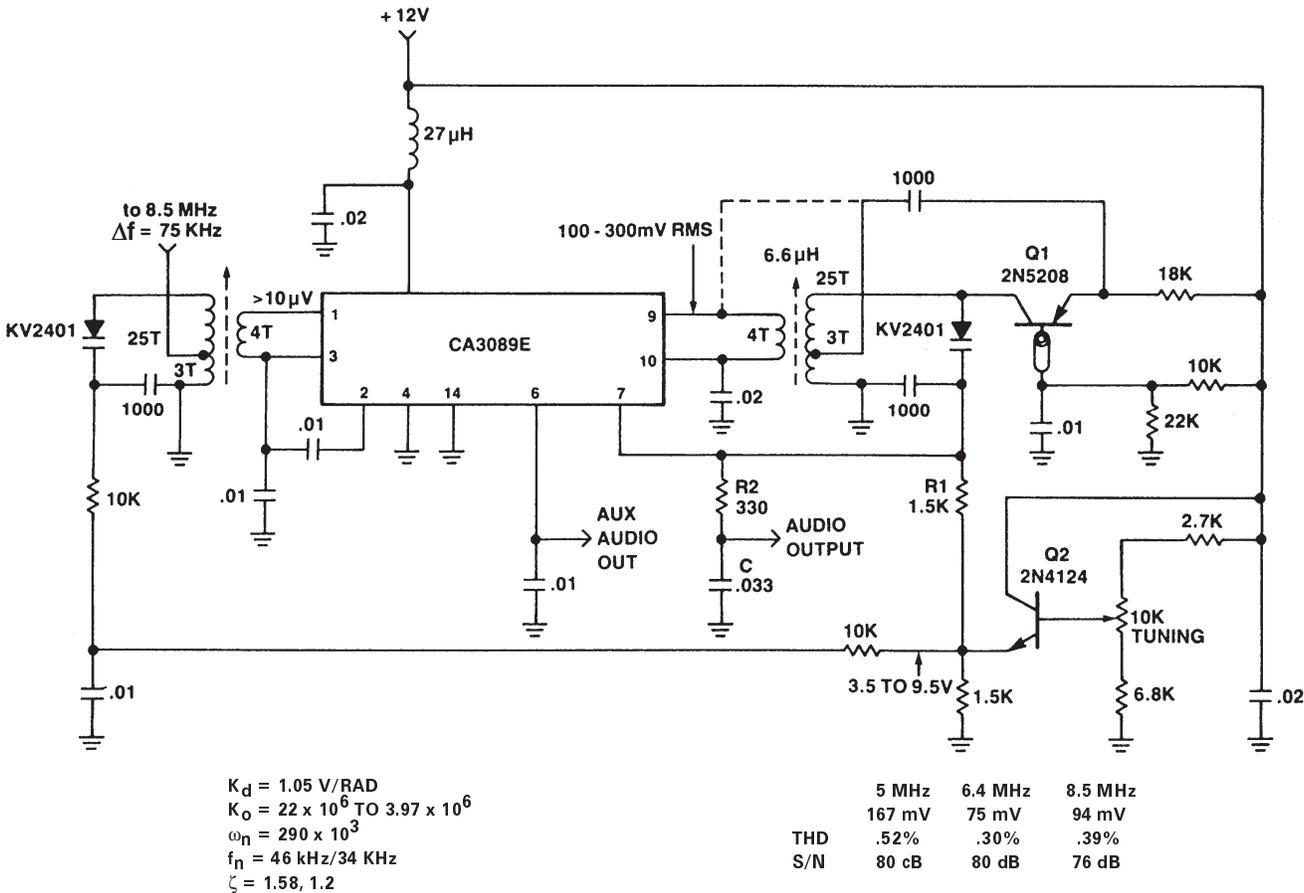


Figure 20.

# Application Notes

The CA3089E has been used as previously, but the VCO tuning voltage of 3.5 to 9.5 V is derived from the adjustable voltage at the emitter of Q2 instead of the reference voltage on pin 10 of the IC. Q2 provides a temperature compensation as well as a low impedance source for R1 of the loop filter. In order to keep the distortion over the tuning range low, the tuning voltage must be kept as close as possible to the linear tuning range of the diode. This necessitates keeping the stray capacitance as low as possible, so the VCO has been designed with feedback from a tap on the oscillator coil. The first design used a KV2201 diode to keep the effect of Cs in series with the diode low, but the coil had to have a relatively high inductance of 201  $\mu$ H. This results in a coil with too much stray capacitance, so the KV2401 turns out to be a better choice. The resulting tuning characteristic for the VCO is shown in Figure 21.

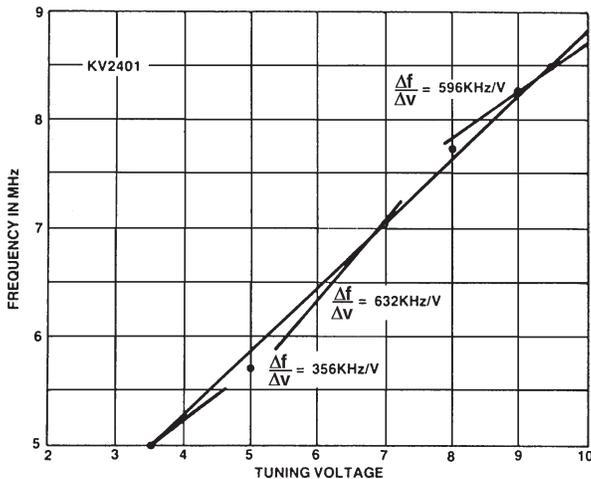


Figure 21.

Since the slope of the frequency versus voltage curve for the VCO changes at the ends of the tuning range, the oscillator constant,  $K_o$ , and the detected audio output level will also change. At 3.5V,  $K_o = 2.23 \times 10^6$  and at 6.0V,  $K_o = 3.97 \times 10^6$ . This results in a change in the closed loop response, but since  $\omega_n$  is proportional to  $\sqrt{K_d K_o}$ , the change will not be great. Audio output for  $D_f = \pm 75$  kHz does change from 167 mV RMS at 5 MHz to 75 mV RMS at 6.4 MHz to 94 mV at 8.5 MHz, so the audio amplifier gain following the detector should be made high enough to accommodate the lowest level.

At first, it seems like the audio signal-to-noise ratio could not be very good if the audio output level is only 75 mV, but note that it is 80 dB. This is mainly because the VCO is tuned with an LC circuit which is inherently quiet when its Q is high. Also note the low distortion of only about .3% over most of the tuning range.

If a separate demodulator for each sound channel is desired, the circuit of Figure 5 for the 10.7 MHz detector can be used with the tuning coil being changed from 7.1 mH to an appropriate value for the desired frequency. For this case, the ability to cover a large tuning range is not important so Cs and Ct can be adjusted as described earlier to produce minimum distortion. Either the KV2201 or KV2401 diodes will give good results.

## REFERENCES:

1. GrosJean, J.P., "Phased Locked Loops using Quadrature Detector Integrated Circuits", IEEE Transactions on Consumer Electronics, February 1976, Vol 22 Number 1 p. 95
2. Gardner, Floyd M., " Phaselock Techniques" John Wiley & Sons New York 1979 (Second Edition)

## SUMMARY

A wide variety of circuits for low distortion FM generation and detection has been described. The use of hyperabrupt tuning diodes ensures not only high performance but also excellent reproducibility and low cost. A novel push-pull VCO design facilitates implementation of practical wideband phase-locked loop detectors at 70 and 140 MHz, while a 300 MHz PLL detector preceded by an appropriate filter permits single conversion in satellite receivers. Additional circuits are provided for standard IF's in the 5 to 25 MHz range. Most designers will find that the circuits contained in this note will be directly usable in their systems, while the most sophisticated requirements can be addressed with only slight modification of these proven designs.