AC462
Application Note
PolarFire FPGA Package Fanout

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

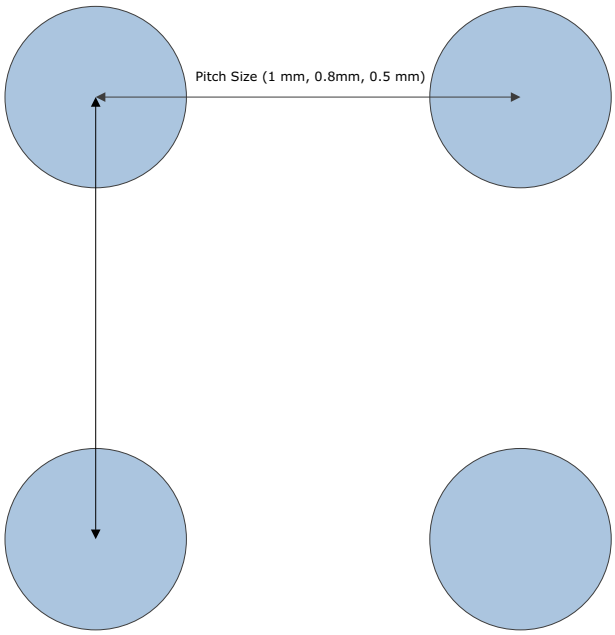
2 PolarFire FPGA Package Fanout

Microsemi offers FPGA devices with three different pitch sizes—0.5 mm, 0.8 mm, and 1 mm. The density, complexity, and type of routing differ across devices based on the application and size of the board. This application note provides information about the number of layers, cost implications, and the size of pads and vias for different package sizes. Contact the PCB manufacturer for accurate information.

2.1 Pitch Size

The following figure illustrates the pitch size between the adjacent pads in a device package.

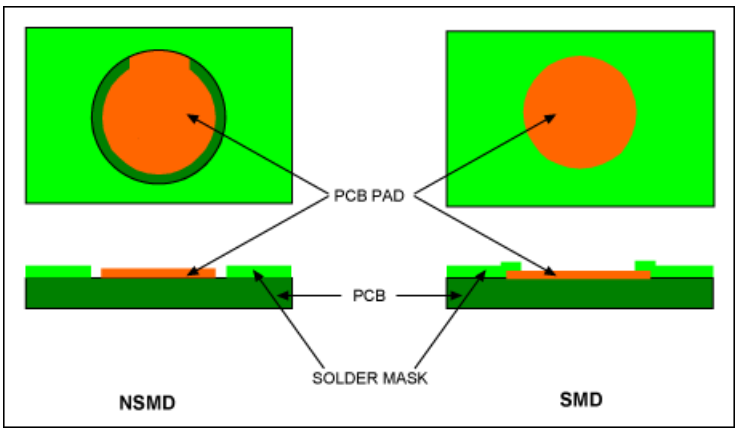
Figure 1 • **Pitch Size**



2.2 Pad Recommendation

There are two types of BGA pads—non-solder mask defined (NSMD) and solder mask defined (SMD). Microsemi recommends NSMD type of pads for all the devices. NSMD type of pads helps to achieve balanced stress on solder joints. The following figure illustrates the two BGA types.

Figure 2 • **BGA Pad Types**



2.3 Types of Routing

A device has routing to all four directions for different signals. Following are the two types of signal fanouts:

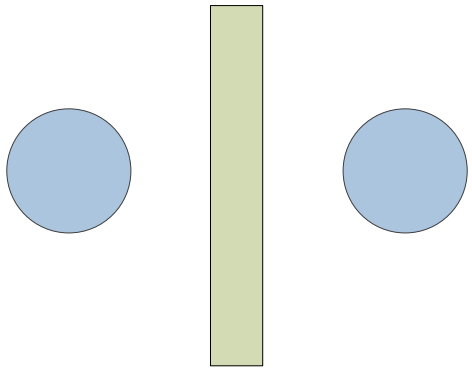
- Single-trace breakout
- Dual-trace breakout

2.3.1 Single-Trace Breakout

In single-trace breakout, a single trace is fanned out between two pads on the outer layers and two fanout vias on the internal signal layers, as illustrated in the following figure.

Single-trace breakout has high amount of copper-to-copper clearance. It, therefore, does not need an advanced technology for PCB fabrication. The per-layer cost for copper etching is less than that of compared to dual-trace breakout.

Figure 3 • **Single-Trace Breakout**

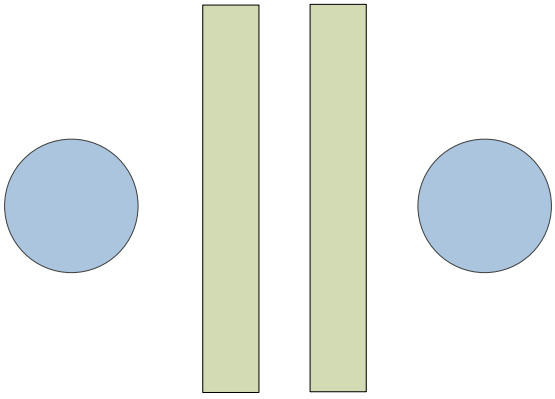


2.3.2 Dual-Trace Breakout

Dual-trace breakout employs two signal traces between two BGA pads on the outer layers and two traces between two fanout vias on the internal signal layers, as illustrated in the following figure. This kind of fanout needs very precise control for copper clearance and trace width, therefore, costing more than the single-trace breakout.

Note: Dual-trace breakout is only possible with 1 mm pitch packages. For smaller packages, the space between two pads/vias may not be sufficient to route two traces, and PCB fabrication is costly.

Figure 4 • **Dual Trace Breakout**



Note: No blind or buried via technology is employed for the fanout.

Table 1 • **Signal Layer Requirements**

BGA Pins	Pitch Size (mm)	Number of Signal Layers Needed	
		Dual Trace	Single Trace
484	0.8	3	4
484	1.0	2	4
536	0.5		3
784	1.0	3	5
1152	1.0	3	6

2.4 Layout Consideration

The numbers of layers depends on the number of signals routed from the package. In Microsemi FPGA devices, the signal pins constitute about 55-65% of the total pins in the package. The number of layers increases linearly with the amount of signal pins to be routed. In applications with space constraints, the trace width can be narrowed down to route multiple traces between two pads/vias. Though this approach accommodates more traces in the BGA area, it causes impedance discontinuity in that region and increases crosstalk between the signals. Microsemi recommends contacting the signal integrity engineers if a narrowing down approach is followed.

2.5 Stack-Up Design

A good stack-up leads to better performance. The number of layers in the stack-up depends on factors such as the board's form factor, number of signals to be routed, and power requirements. Based on these factors, the designer chooses how many layers the board requires.

The upper-power layers should be used for high-priority supplies. High-switching current supplies should be placed vertically close to the devices to decrease the distance that the current needs to travel through the vias. Ground planes should be placed adjacent to the high-transient current power planes to reduce inductance and to provide the decoupling of noise at higher frequency noise.

It is good to have power and ground layers side-by-side so that the inter-plane capacitance provides better decoupling at high frequencies. The effect of vias on power pins is reduced by placing a power plane near the device. Signal integrity depends on how well the traces have controlled impedance, so it is always recommended to have controlled impedance.

Microsemi recommends that all critical high-speed signals such as DDR and transceiver PCIe signals have a solid ground reference. These signals should be separated from each other by good distance, ground, or power planes. This minimizes crosstalk and provides balanced and clean transmission lines with properly controlled characteristic impedance between devices and other board components. For best performance, use dedicated ground plane layers that are continuous across the entire board area. Power planes can provide adequate reference; however, the power planes should be related to the signals they serve to reference.

Note: Do not use unrelated power planes as a signal reference.

Slots should not interrupt the planes, or else they can possibly force current to find an alternate return path. This undesired return path may cause a localized bounce on the power or ground plane that can possibly be capacitive coupled to all signals adjacent to the planes.

For example,

- FC484 1.0 mm has a single-trace breakout. The FC484 package requires the following layers:
  - Signal layers—4
  - Power plane—2
  - Ground layer—4

Figure 5 • **Sample Stack-Up Layers**

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness
		Solderm...		Dielectric	3.3	0.5	
1	8	Signal	Top/Signal	Conductive			1.4
		Prepreg		Dielectric	4.3	3	
2		Plane	GND	Conductive			1.4
		Core		Dielectric	4.3	5	
3		Signal	Signal Layer	Conductive			1.4
		Prepreg		Dielectric	4.3	5	
4		Signal	GND	Conductive			1.4
		Core		Dielectric	4.3	5	
5		Plane	VDD / Power Supply	Conductive			1.4
		Prepreg		Dielectric	4.3	18	
6		Plane	VDD / Power supply	Conductive			1.4
		Core		Dielectric	4.3	5	
7		Signal	GND	Conductive			1.4
		Prepreg		Dielectric	4.3	5	
8		Signal	Signal Layer	Conductive			1.4
		Core		Dielectric	4.3	5	
9		Plane	Ground	Conductive			1.4
		Prepreg		Dielectric	4.3	3	
10		Signal	Bottom/Signal	Conductive			1.4
		Solderm...		Dielectric	3.3	0.5	

2.6 Pinout

Some pins in the device are assigned with specific functionality, such as JTAG and clock inputs. For these pins, the routing constraints are fixed, and swapping is not allowed.

For the DDR interface, the software defines the pin functionality, and limited swapping support is available.

2.7 Fabrication Technology

For fabrication, the following aspects need to be considered:

- Aspect ratio
- Micro via and back-drilled via
- Via on pad

2.7.1 Aspect Ratio

Aspect ratio is the ratio of thickness of the board and maximum drill diameter of the plated through holes (PTH) used on the board. By traditional PCB fabrication methods, the aspect ratio must not be more than 1/10. This means the PTH diameter on the board must be 1/10 of the board thickness or more. When a smaller via hole is required, blind and buried via on PCB must be used. The drill hole is usually 3 mils wider than the required diameter, as the via plating process reduces the drill diameter by 3 mils. Contact the fabrication vendor for accurate aspect ratio.

2.7.2 Micro Via and Back-Drilled Via

The use of blind and buried vias for signals increases the cost of PCB compared to PTH via, as the micro via needs more precise tolerance control on the PCB for drilling and copper clearance. In some applications, the PTH via needs to be drilled from one end of the board to get rid of extra via stub on high frequency signals. The back drilling increases the cost of PCB because of the increase in fabrication complexity.

2.7.3 Via on Pad

The use of via on pad increases the cost of PCB because of the extra fabrication cycle of PCB, as it requires copper plating to cover the via on the pad. The pad is used to mount the components.

Note: The addition of micro vias, via-in-pad, and layers increases the PCB cost. For information about the PCB fabrication costs, contact the PCB fabrication vendor.

2.8 Routing Guidelines for 1 mm Pitch Packages

The following figures illustrate the routing guidelines for fabricating 1 mm pitch packages, such as FC1152 and FCG484.

Figure 6 • **Single-Trace Breakout Between Two Balls (mils)**

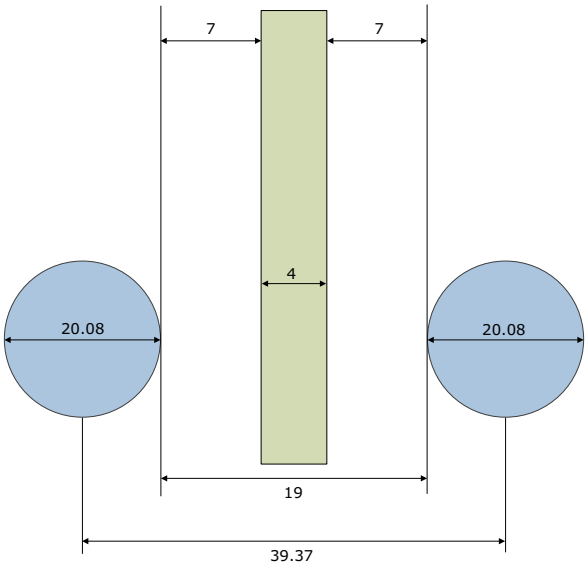


Figure 7 • **Dual Trace Breakout Between Two Balls (mils)**

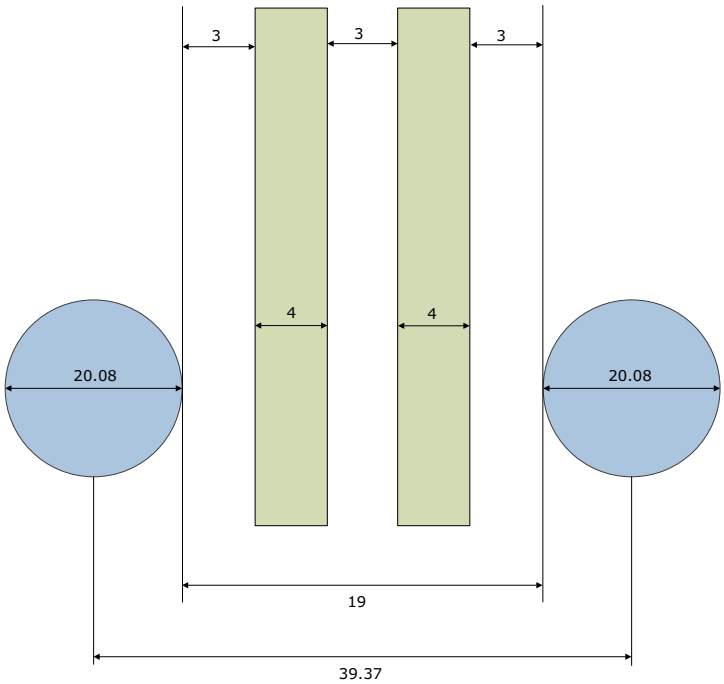


Figure 8 • **Single Trace Route Between Two Vias (mils)**

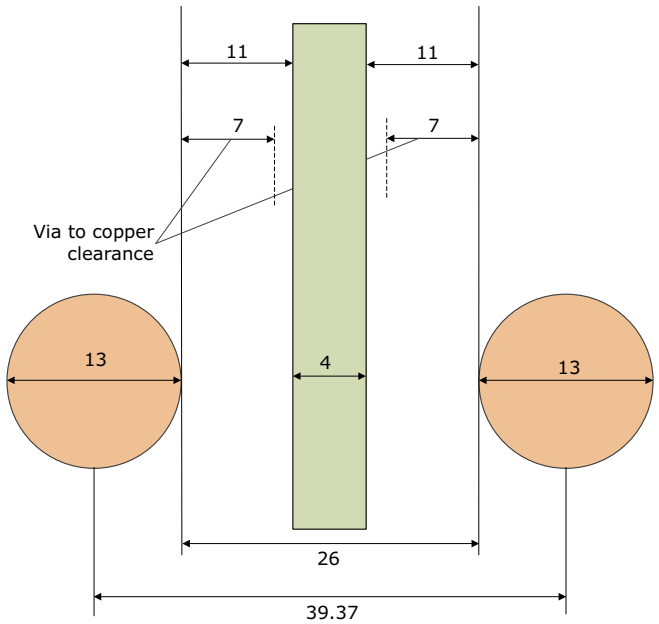
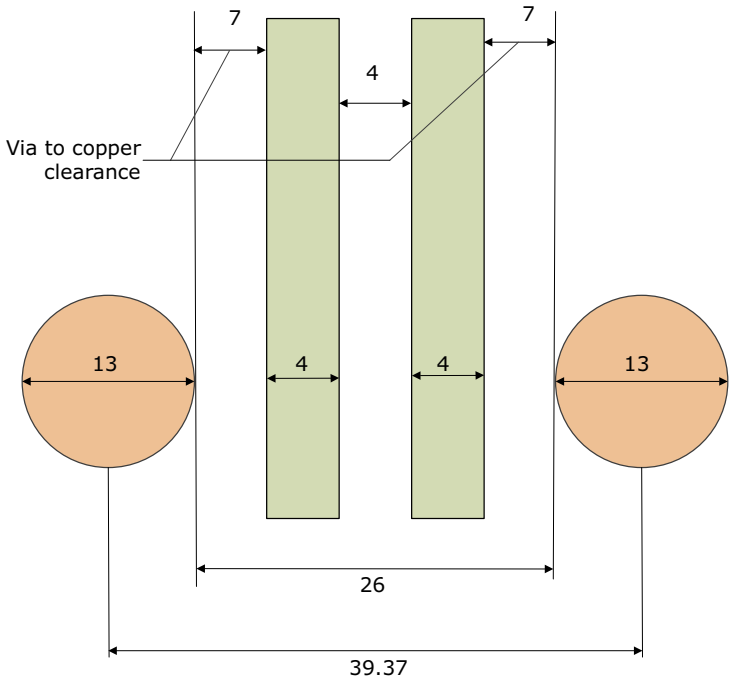


Figure 9 • **Double Trace Route Between Two Vias (mils)**



2.8.1 Single-Trace Breakout for FC1152

The following figures illustrate the single-trace breakout for FC1152.

Figure 10 • **Layer-1, Single-Trace Breakout (1 mm Pitch)**

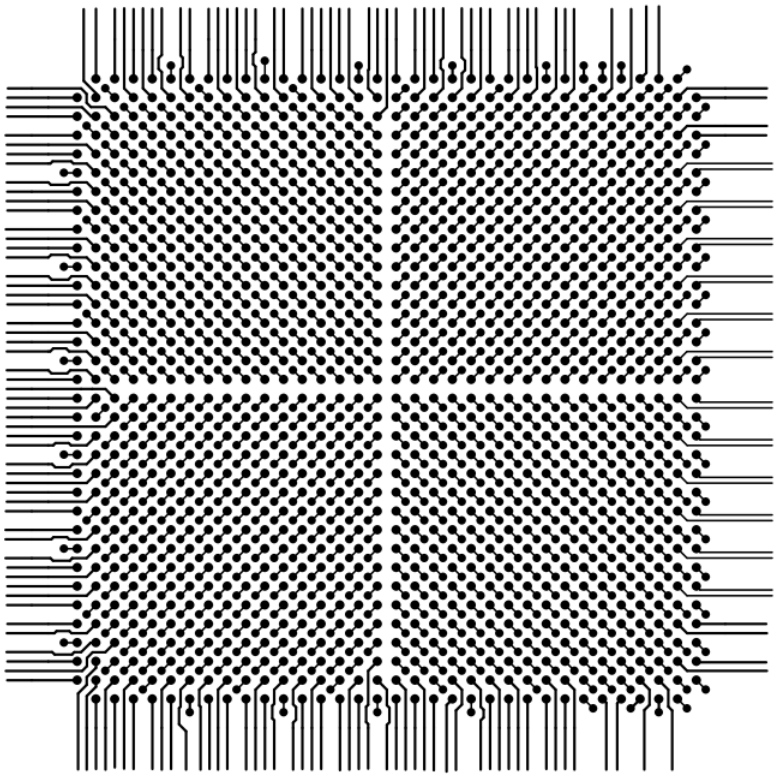


Figure 11 • **Layer-2, Single-Trace Breakout (1 mm Pitch)**

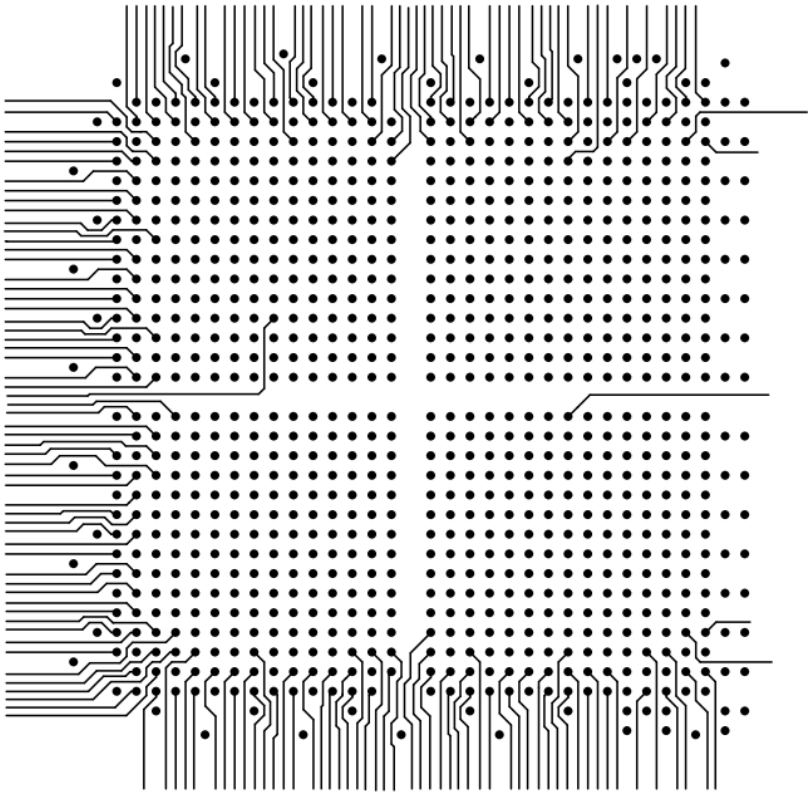


Figure 12 • **Layer-3, Single-Trace Breakout (1 mm Pitch)**

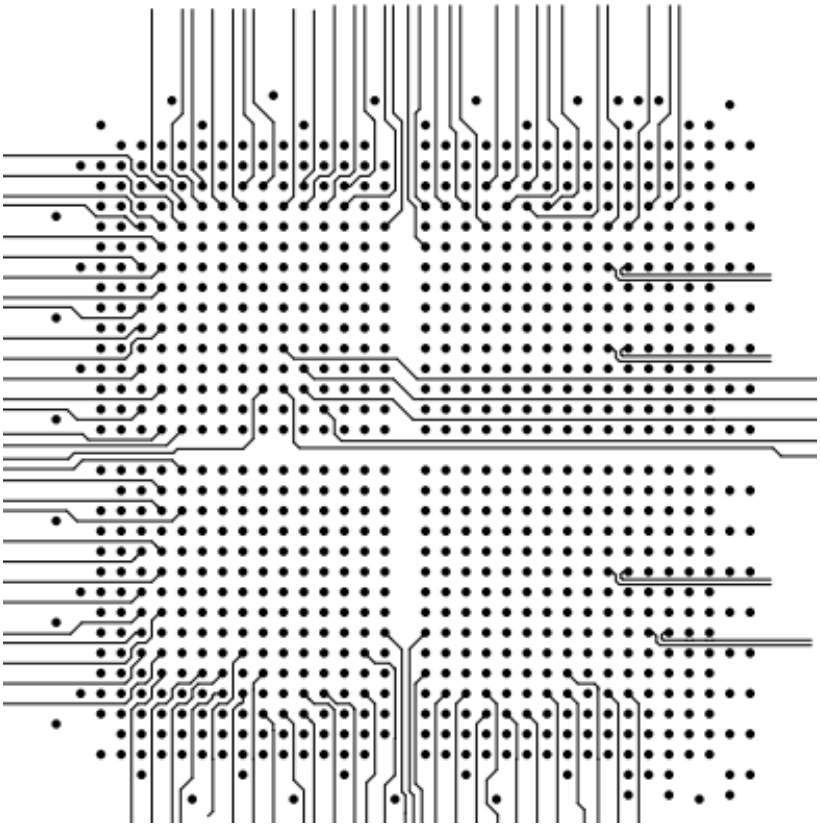


Figure 13 • **Layer-4, Single-Trace Breakout (1 mm Pitch)**

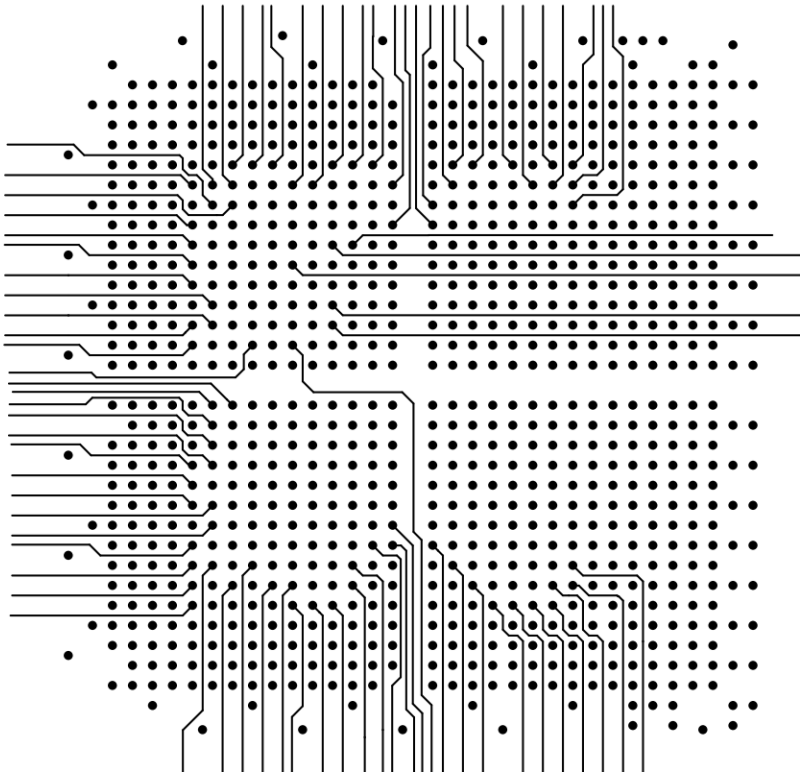


Figure 14 • **Layer-5, Single-Trace Breakout (1 mm Pitch)**

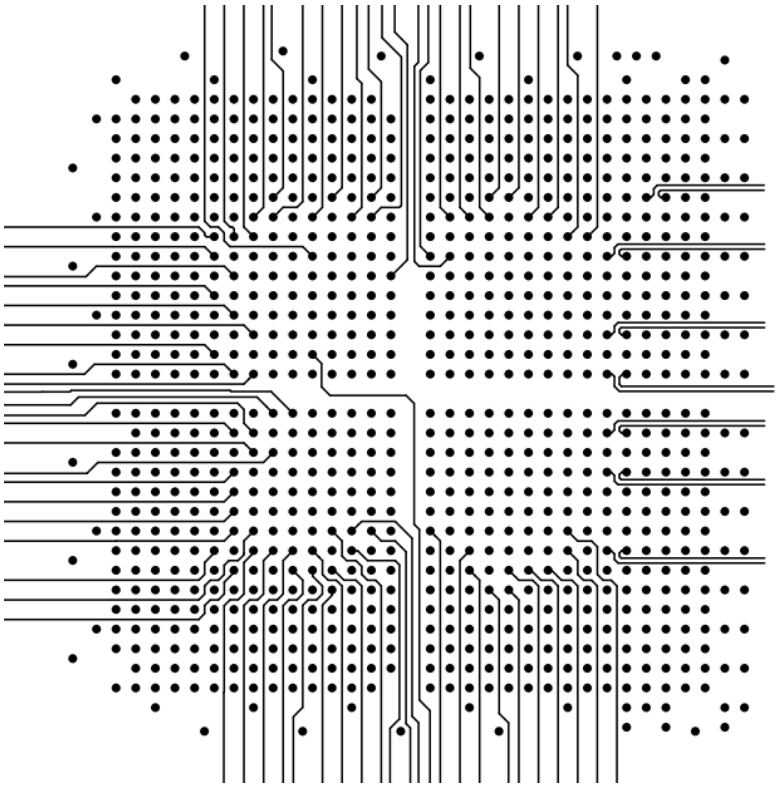
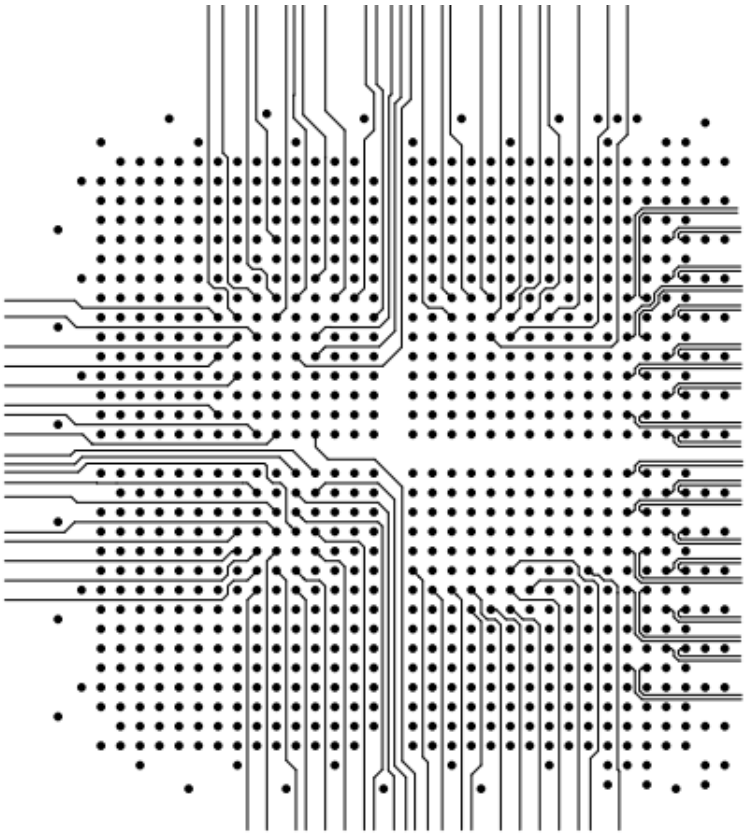


Figure 15 • **Layer-6, Single-Trace Breakout (1 mm Pitch)**



2.8.2 Dual-Trace Breakout for FC1152

The following figures illustrate the dual-trace breakout for FC1152.

Figure 16 • **Layer-1, Dual-Trace Breakout (1 mm Pitch)**

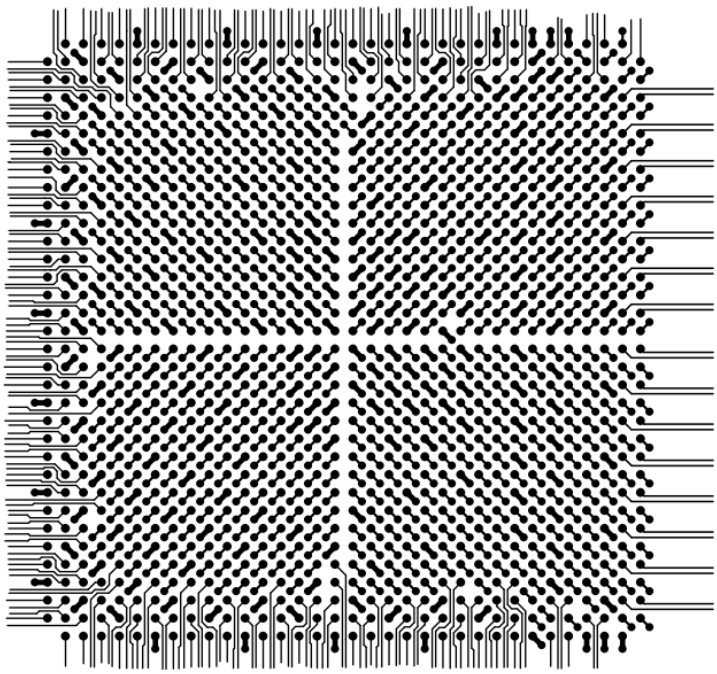


Figure 17 • **Layer-2, Dual-Trace Breakout (1 mm Pitch)**

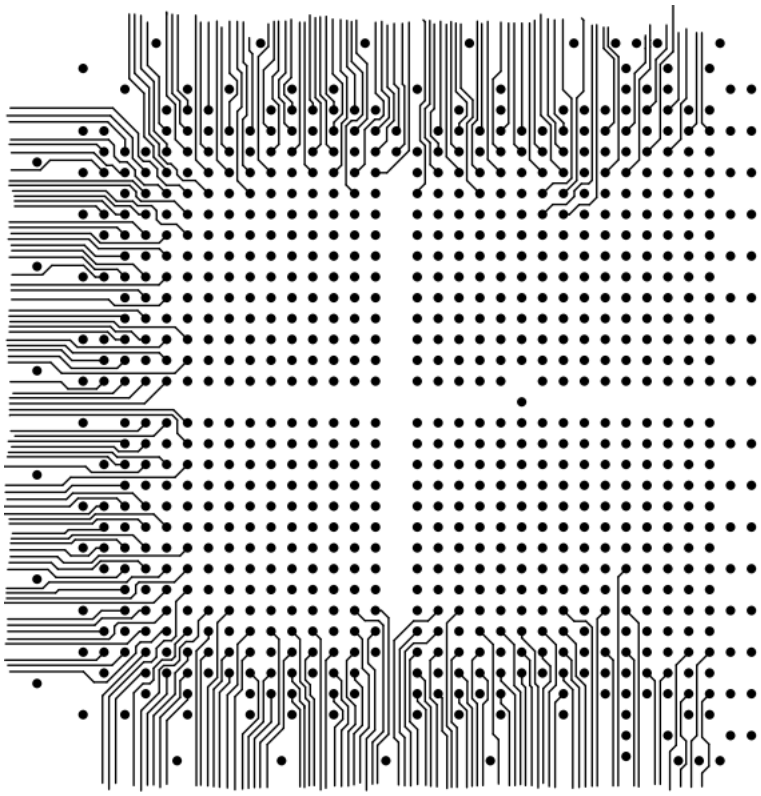


Figure 18 • **Layer-3, Dual-Trace Breakout (1 mm Pitch)**

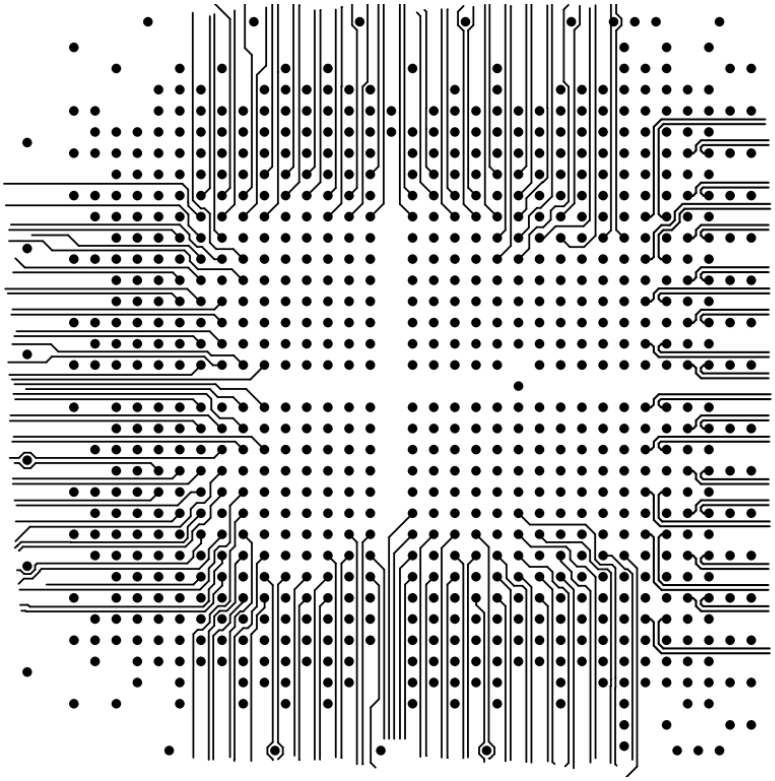
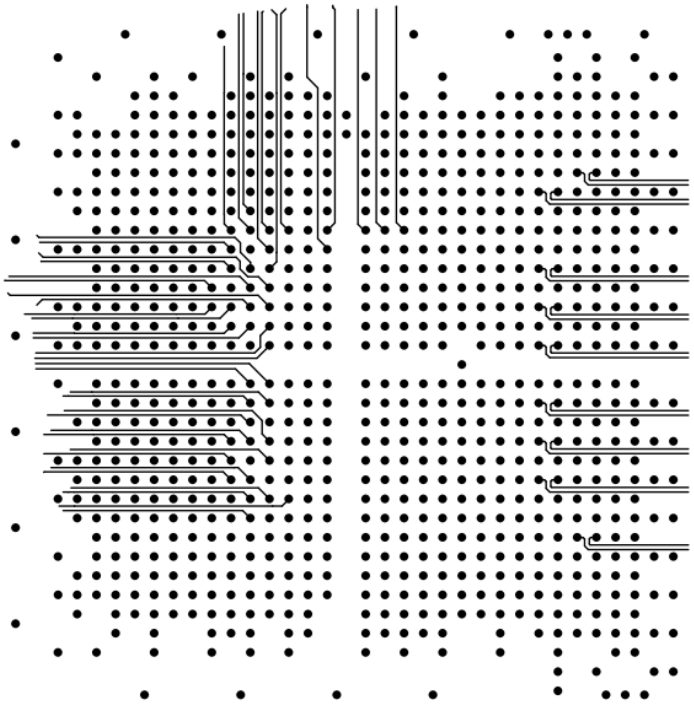


Figure 19 • **Layer-4, Dual-Trace Breakout (1 mm Pitch)**



2.8.3 Single-Trace Breakout for FCG784

The following figures illustrate the single-trace breakout for FCG784.

Figure 20 • **Layer-1, Single-Trace Breakout (1 mm Pitch)**

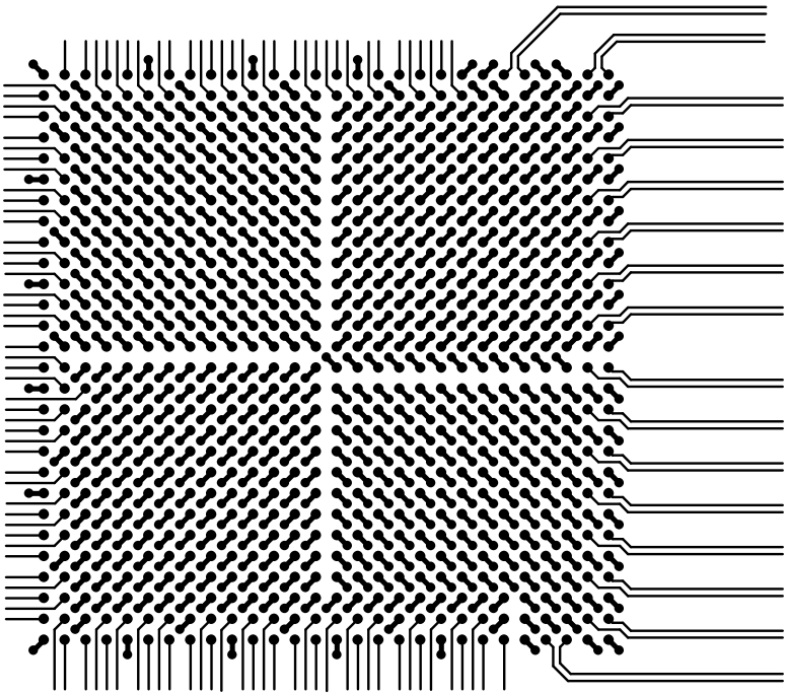


Figure 21 • **Layer-2, Single-Trace Breakout (1 mm Pitch)**

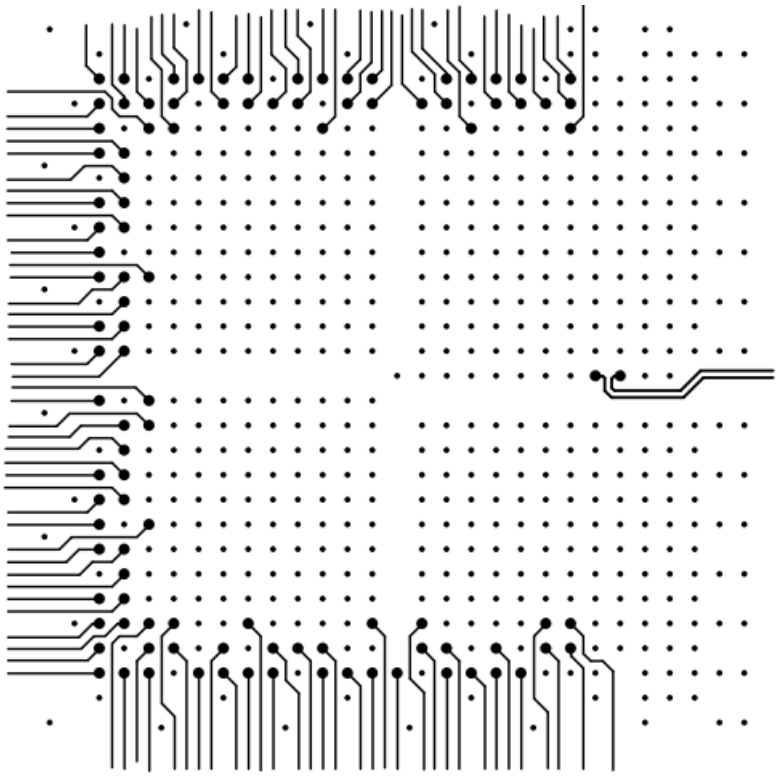


Figure 22 • **Layer-3, Single-Trace Breakout (1 mm Pitch)**

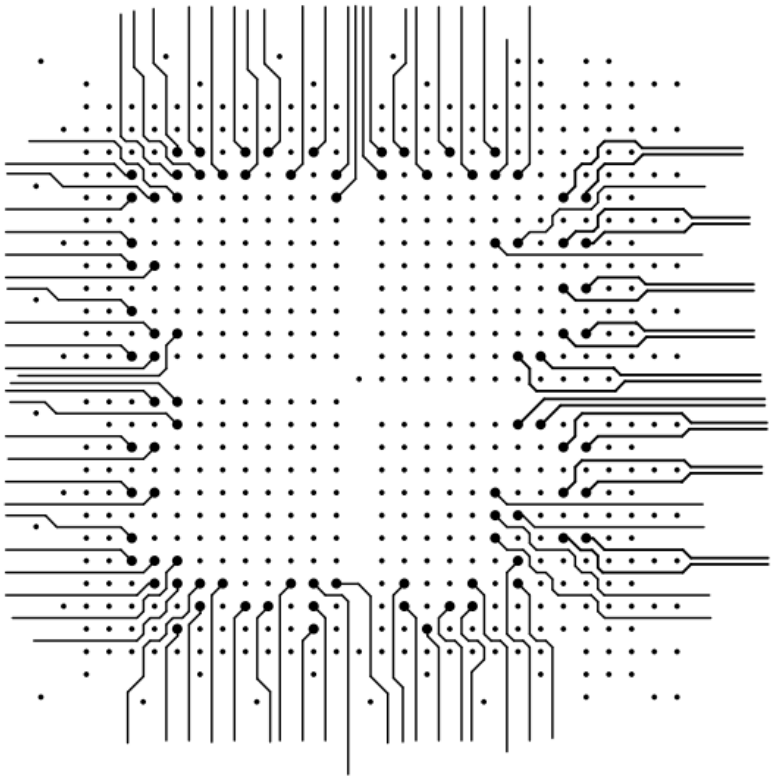


Figure 23 • **Layer-4, Single-Trace Breakout (1 mm Pitch)**

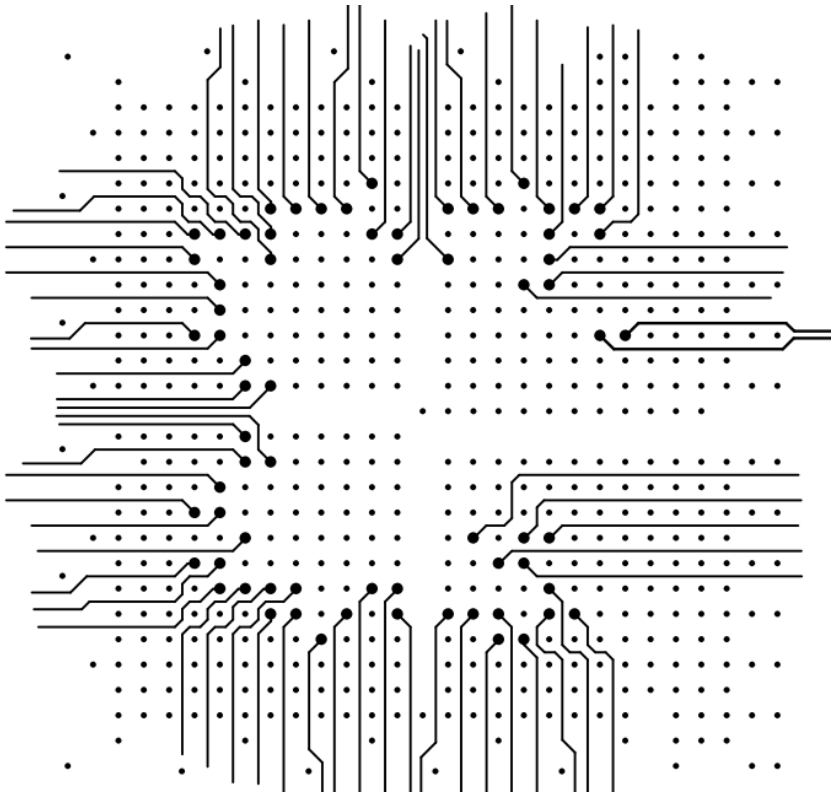
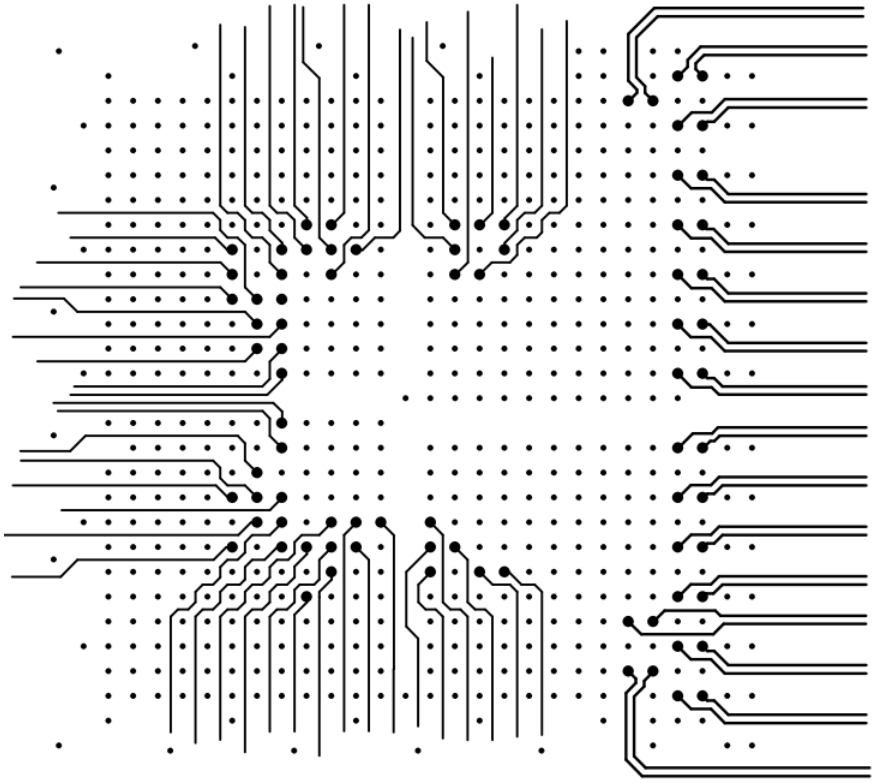


Figure 24 • **Layer-5, Single-Trace Breakout (1 mm Pitch)**



2.8.4 Dual-Trace Breakout for FCG784

The following figures illustrate the dual-trace breakout for FCG784.

Figure 25 • **Layer-1, Dual-Trace Breakout (1 mm Pitch)**

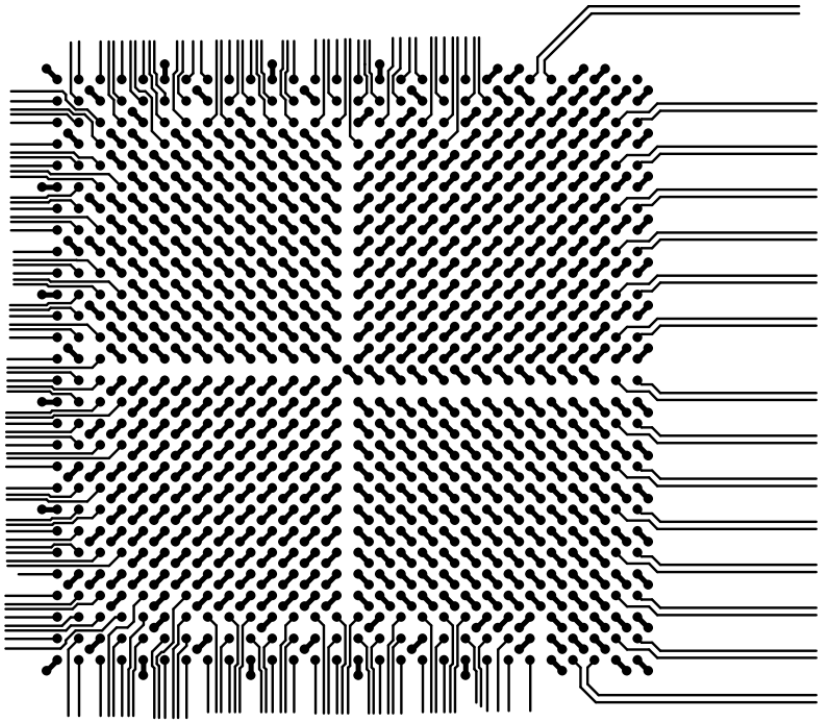


Figure 26 • **Layer-2, Dual-Trace Breakout (1 mm Pitch)**

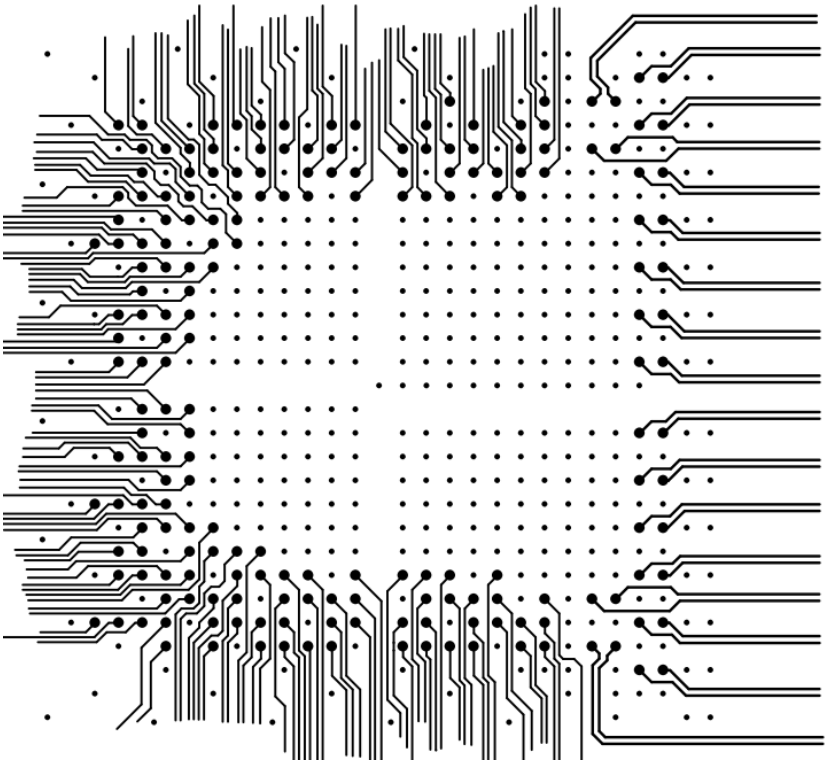
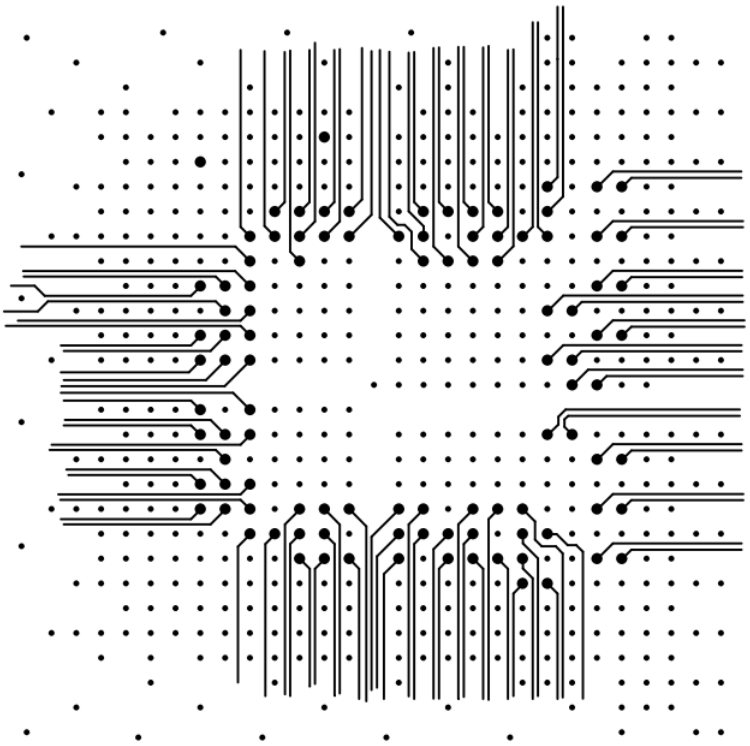


Figure 27 • **Layer-3, Dual-Trace Breakout (1 mm Pitch)**



2.8.5 Single-Trace Breakout for FCG484

The following figures illustrate the single-trace breakout for FCG484.

Figure 28 • **Layer-1, Single-Trace Breakout (1 mm Pitch)**

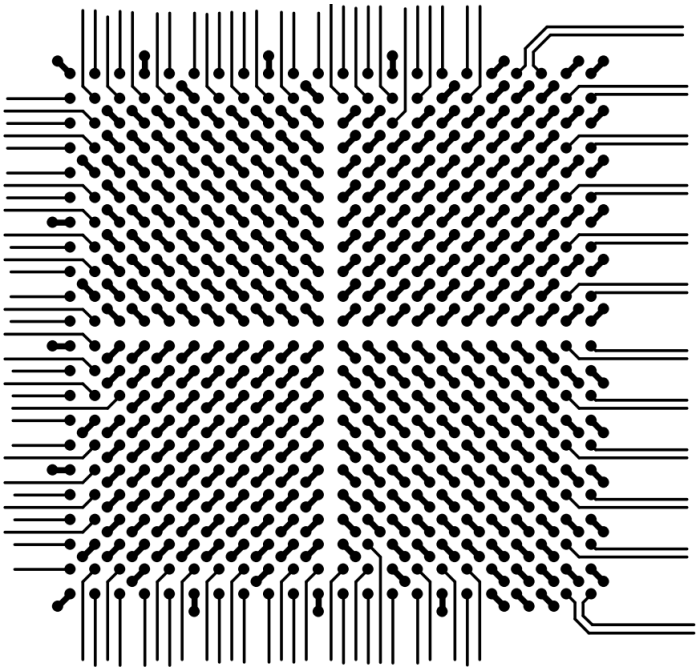


Figure 29 • **Layer-2, Single-Trace Breakout (1 mm Pitch)**

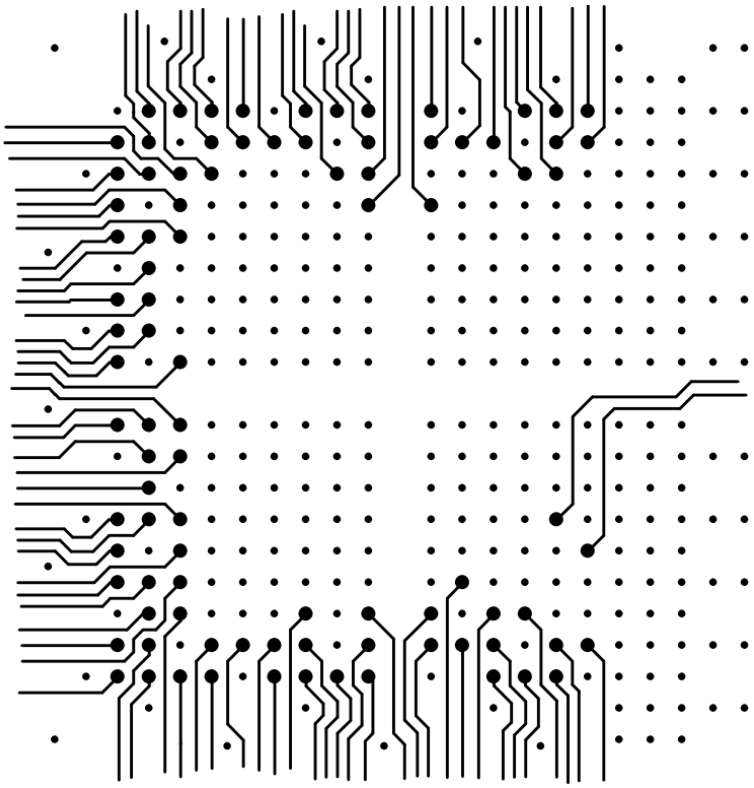


Figure 30 • **Layer-3, Single-Trace Breakout (1 mm Pitch)**

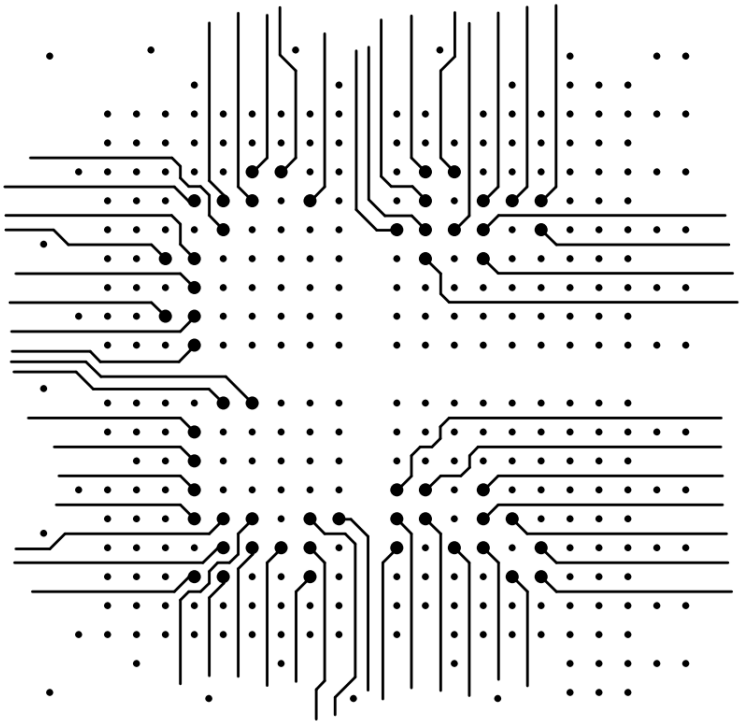
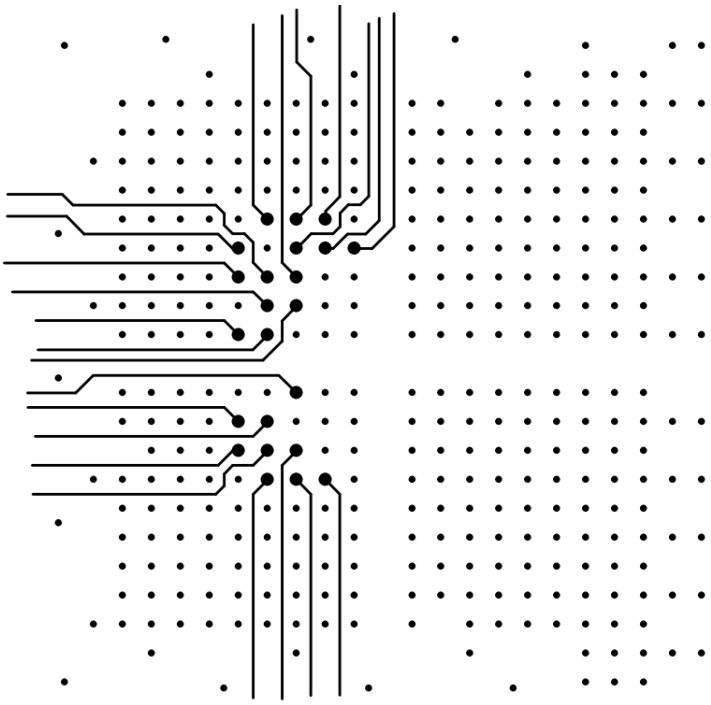


Figure 31 • **Layer-4, Single-Trace Breakout (1 mm Pitch)**



2.8.6 Dual-Trace Breakout for FCG484

The following figures illustrate the dual-trace breakout for FCG484.

Figure 32 • **Layer-1, Dual-Trace Breakout (1 mm Pitch)**

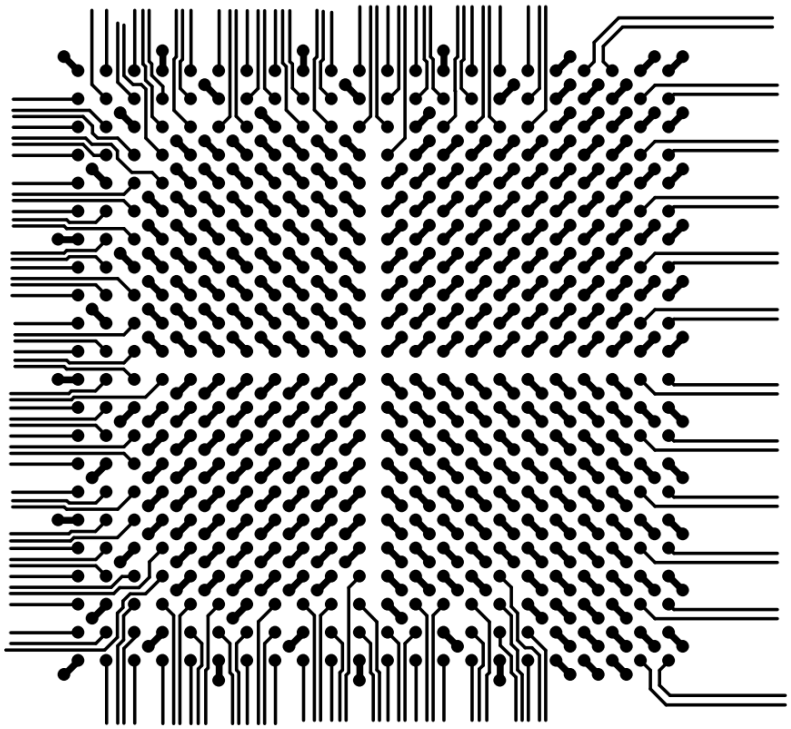
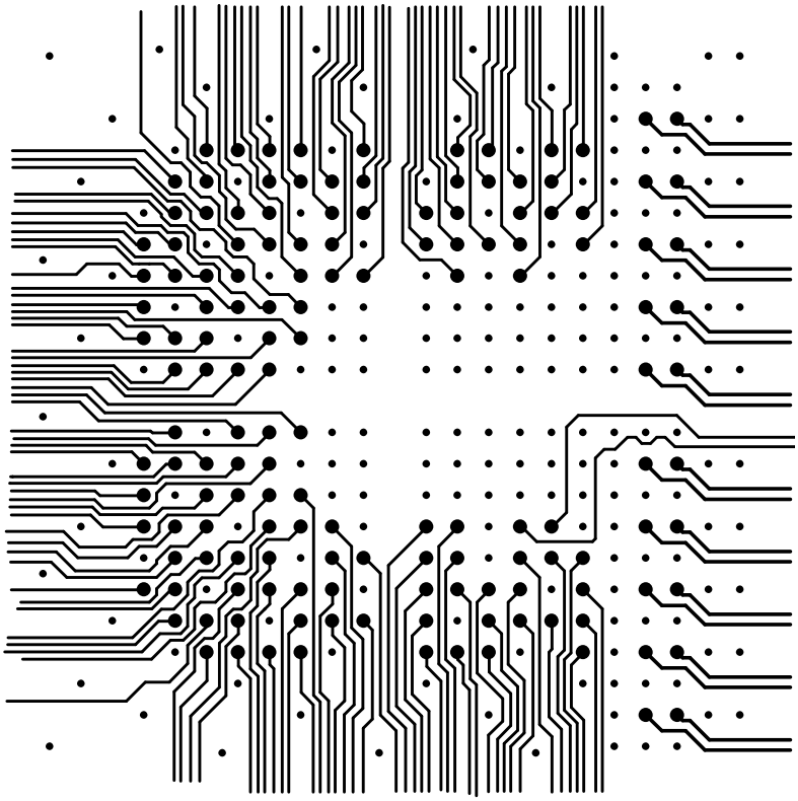


Figure 33 • **Layer-2, Dual-Trace Breakout (1 mm Pitch)**



2.9 Routing Guidelines for 0.8 mm Package

The following figures illustrate the routing guidelines for fabricating 1 mm pitch packages, such as FCV484.

Figure 34 • **Single-Trace Breakout Dimensions (mils)**

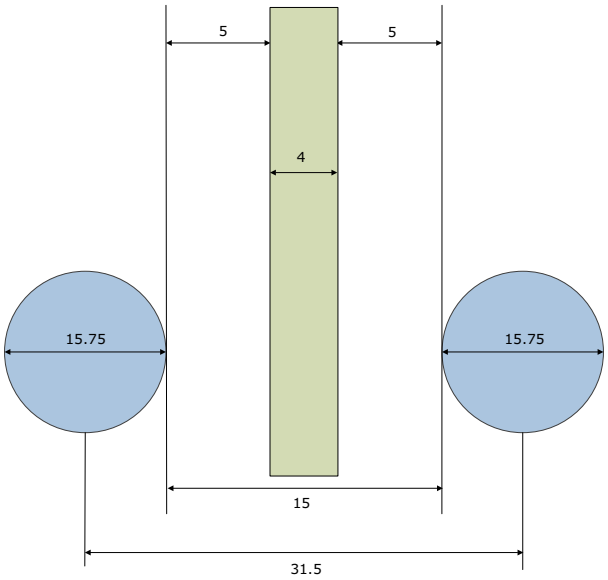


Figure 35 • **Dual-Trace Breakout Dimensions (mils)**

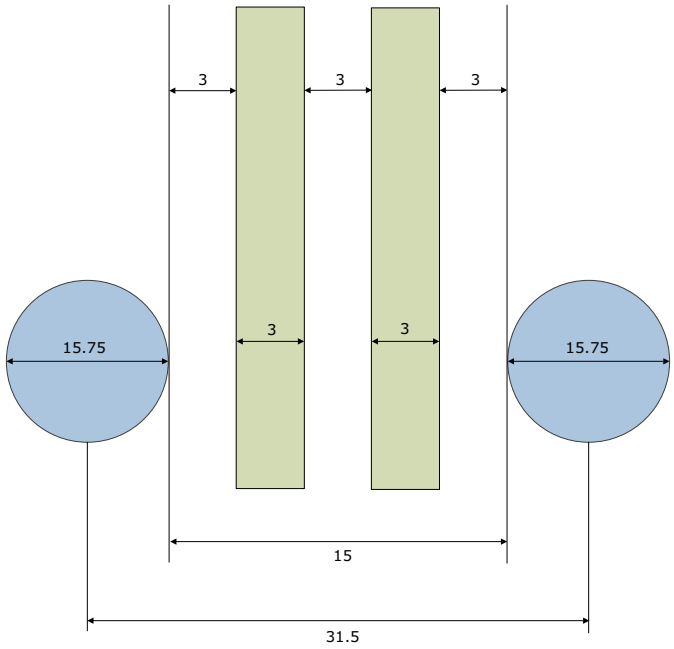
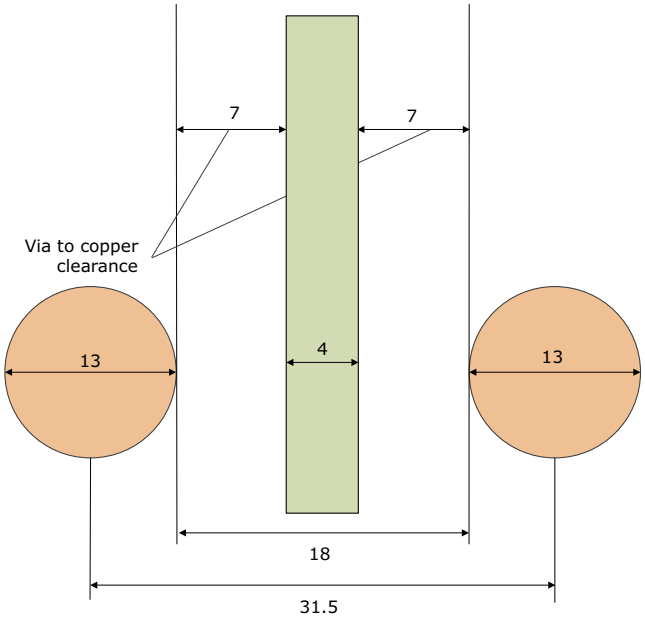


Figure 36 • **Single-Trace Breakout Between Two Vias (mils)**



2.9.1 Single-Trace Breakout for FCV484

The following figures illustrate the single-trace breakout for FCV484.

Figure 37 • **Layer-1, Single-Trace Breakout (0.8 mm Pitch)**

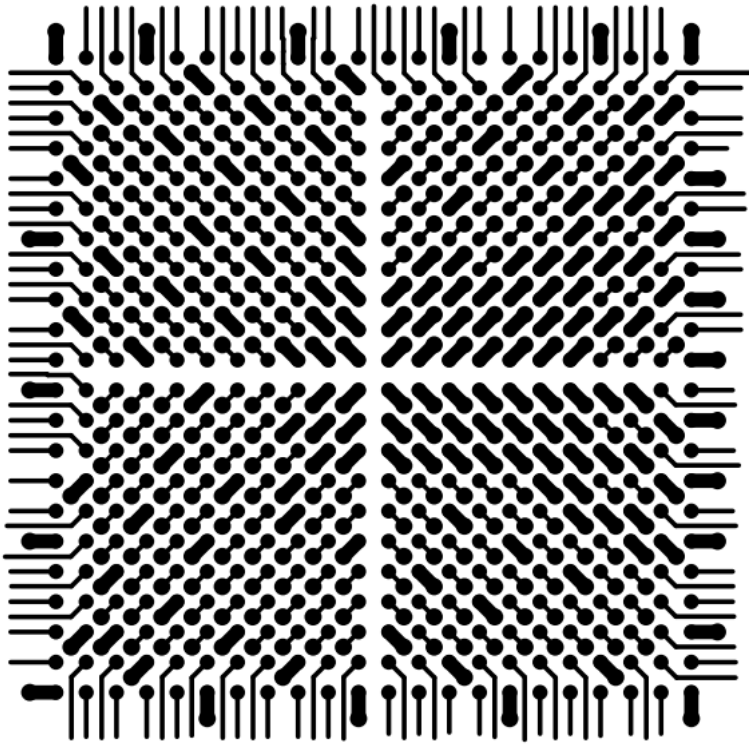


Figure 38 • **Layer-2, Single-Trace Breakout (0.8 mm Pitch)**

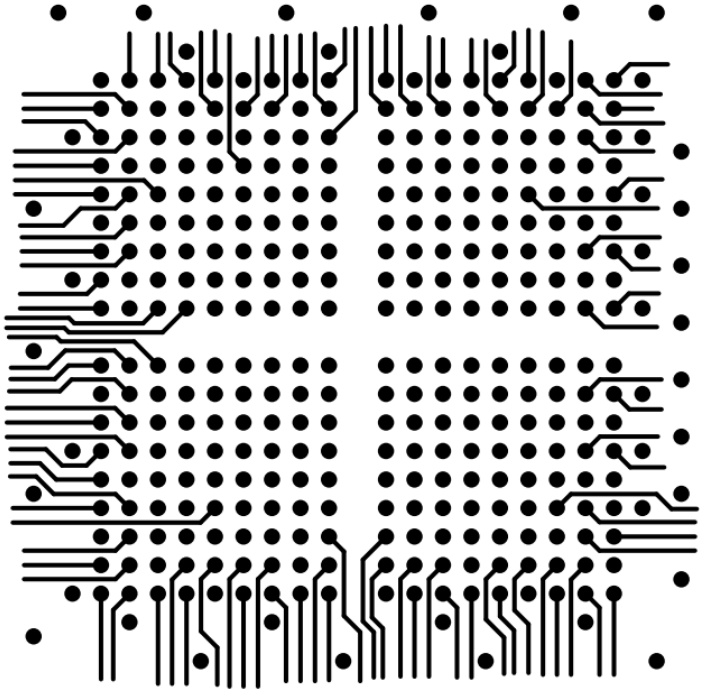


Figure 39 • **Layer-3, Single-Trace Breakout (0.8 mm Pitch)**

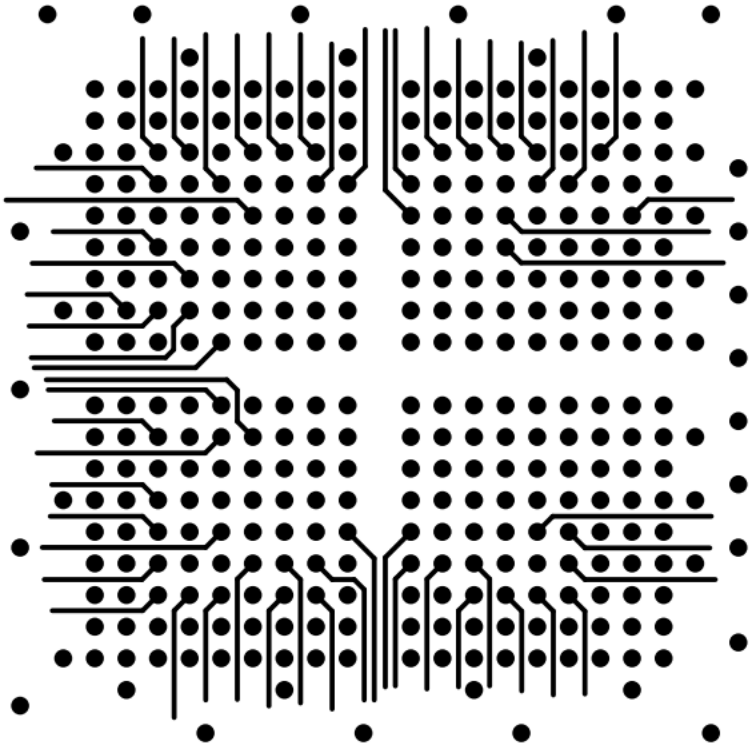
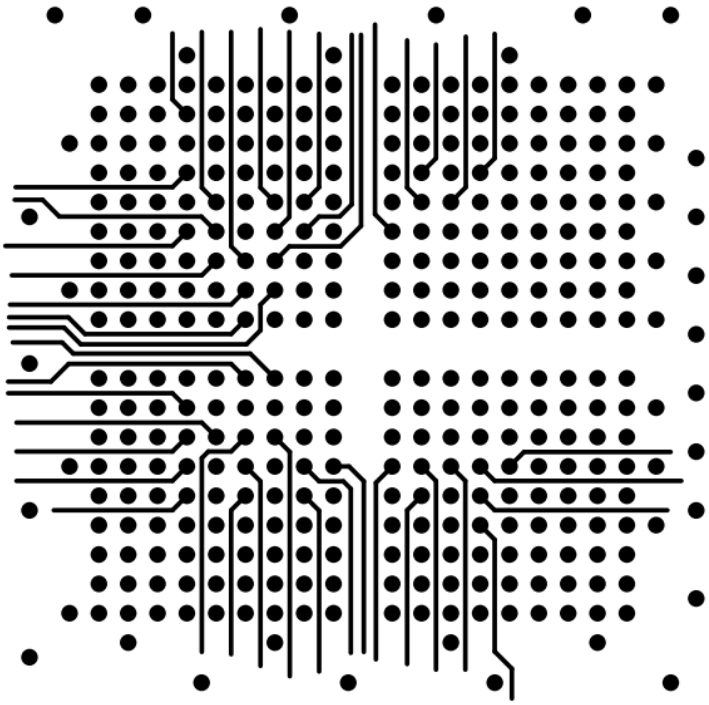


Figure 40 • **Layer-4, Single-Trace Breakout (0.8 mm Pitch)**



2.9.2 Dual-Trace Breakout for FCV484

The following figures illustrate the dual-trace breakout for FCV484.

Figure 41 • **Layer-1, Dual-Trace Breakout (0.8 mm Pitch)**

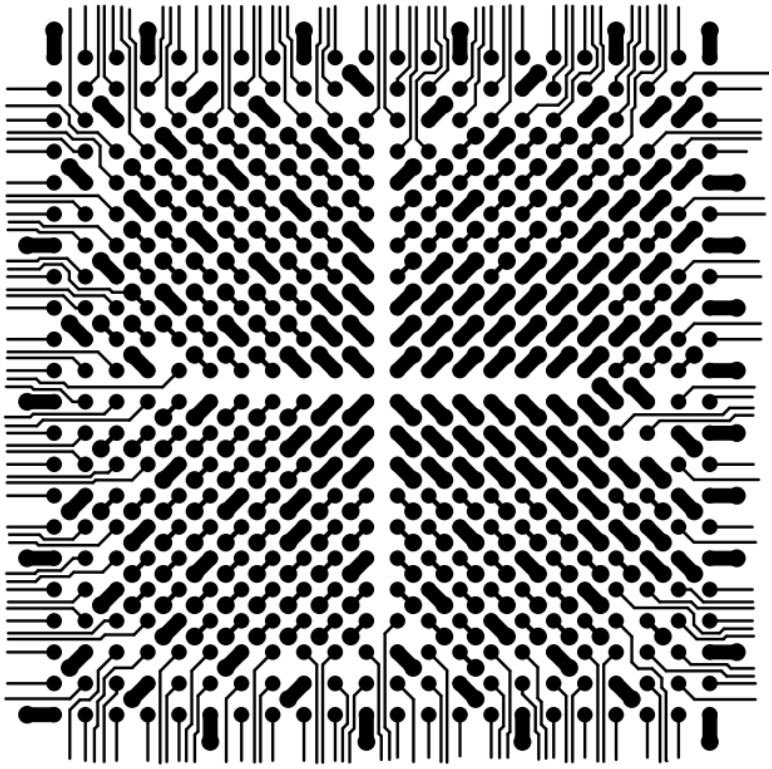


Figure 42 • **Layer-2, Dual-Trace Breakout (0.8 mm Pitch)**

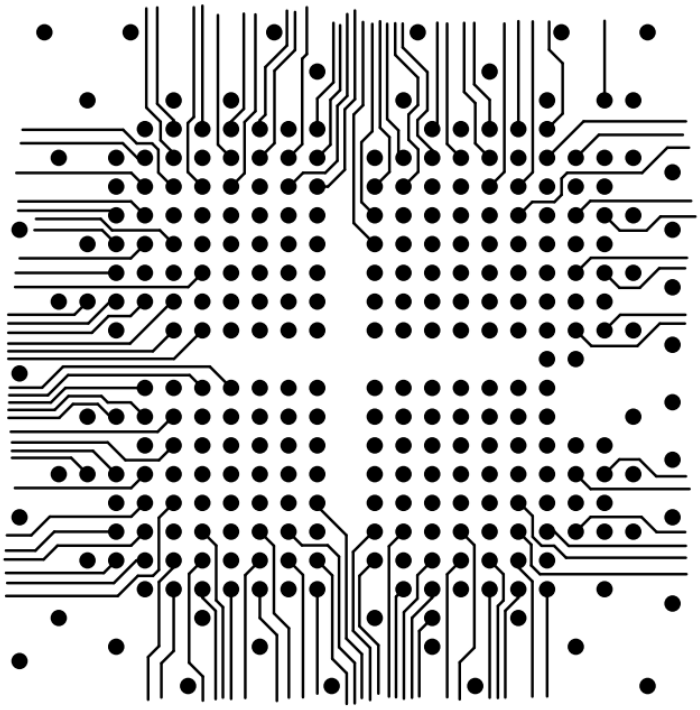
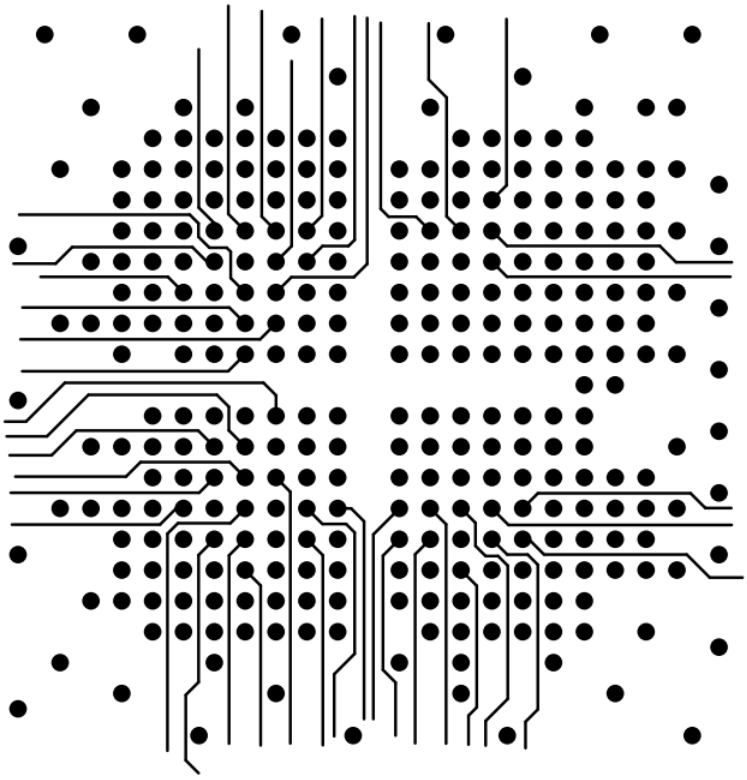


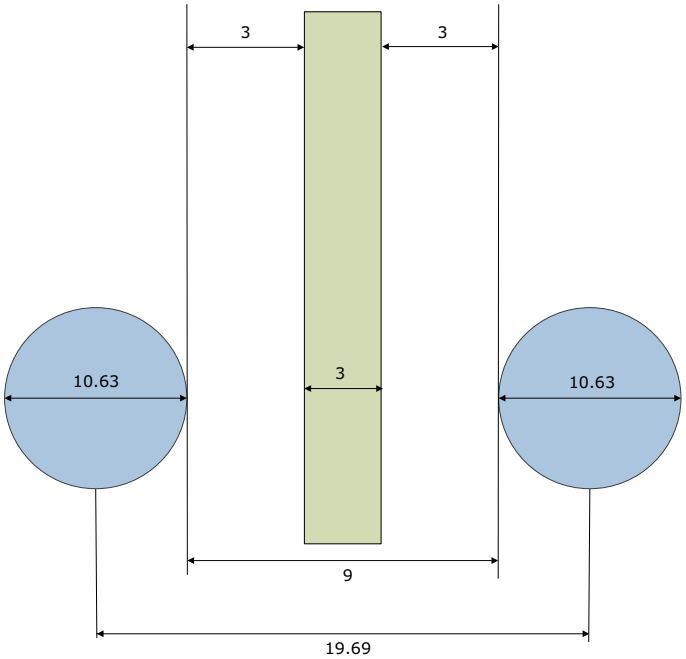
Figure 43 • **Layer-3, Dual-Trace Breakout (0.8 mm Pitch)**



2.10 Routing Guidelines for 0.5 mm Package

The following figures illustrate the routing guidelines for fabricating 0.5 mm pitch packages, such as FCS536.

Figure 44 • **Single-Trace Breakout Dimensions (mils)**



2.10.1 Single-Trace Breakout for FCS536

The following figures illustrate the single-trace breakout for FCS536.

Figure 45 • **Layer-1, Single-Trace Breakout (0.5 mm Pitch)**

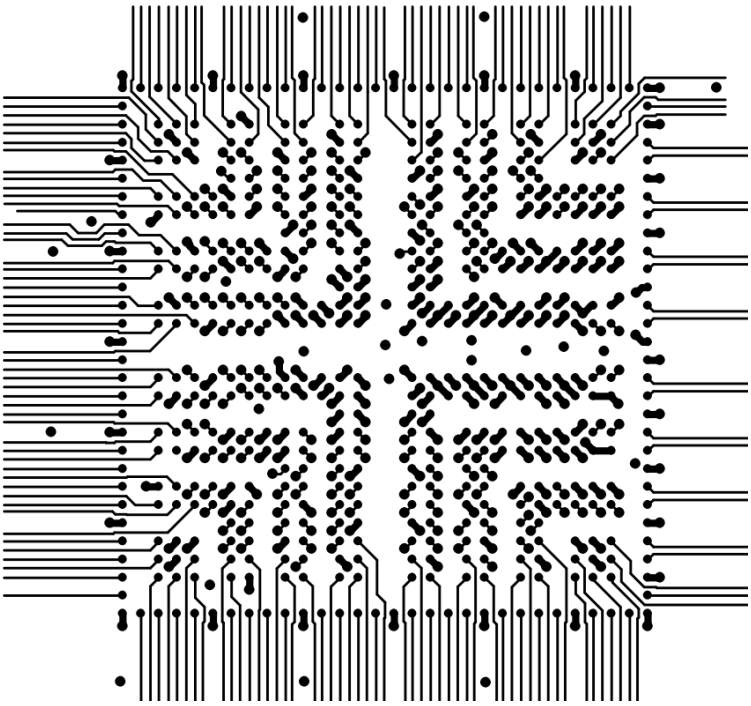


Figure 46 • **Layer-2, Single-Trace Breakout (0.5 mm Pitch)**

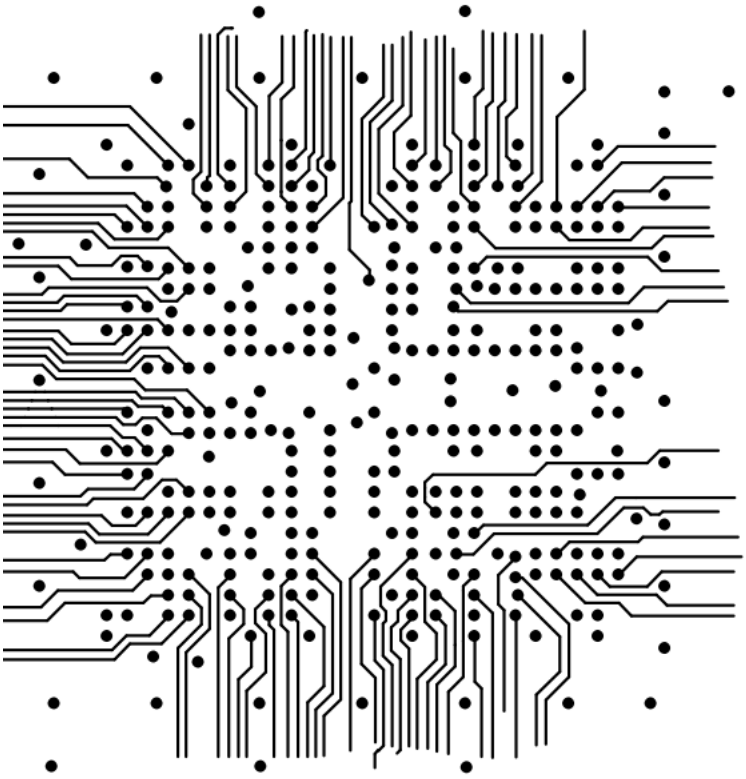


Figure 47 • **Layer-3, Single-Trace Breakout (0.5 mm Pitch)**