TR0036
Test Report
PolarFire FPGA CoreJESD204BRX Interoperability for ADS54J60

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51000036.1.0 11/17

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 PolarFire FPGA CoreJESD204BRX Interoperability for ADS54J60 Test Report

Microsemi provides interfacing solutions for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC standards. These solutions are provided as DirectCore soft IPs (CoreJESD204BRX and CoreJESD204BTX) in Libero® System-on-Chip (SoC) and interfaced with transceivers of PolarFire® FPGA devices. This report provides the results of interoperability tests performed on a third-party ADC device. The interoperability test results describe the JESD204B link parameters, hardware test setup, equipment used, and final test report of Microsemi DirectCore - CoreJESD204BRX.

2.1 References

- *CoreJESD204BRX IP Handbook*
- *CoreJESD204BTX IP Handbook*
- *UG0677: PolarFire FPGA Transceiver User Guide*
- *ADS54J60 Datasheet*
- *Identify ME User Guide*

2.2 Scope

This report describes the hardware setup used for interoperability testing and the test results of the JESD204B link. The following table lists the configuration of the tested device.

Table 1 • **Device Requirements**

Device	Link Rate (Gbps)	Link Width	Subclass
ADS54J60	4.9152 Gbps	×4	0,1

2.3 Test Requirements

The following sections list the hardware and software requirements for interoperability tests.

2.3.1 Hardware Requirements

- PolarFire Evaluation Kit
- ADS54J60 EVM
- Function generator
- 110 V to 240 V AC to 12 V DC - Power adapter
- 110 V to 240 V AC to 5 V DC - Power adapter
- 2 -USB A to mini-B cable
- SMA cables

2.3.2 Software Requirements

- Libero SoC PolarFire
- ADS54J60 EVM GUI

2.3.3 Source Files

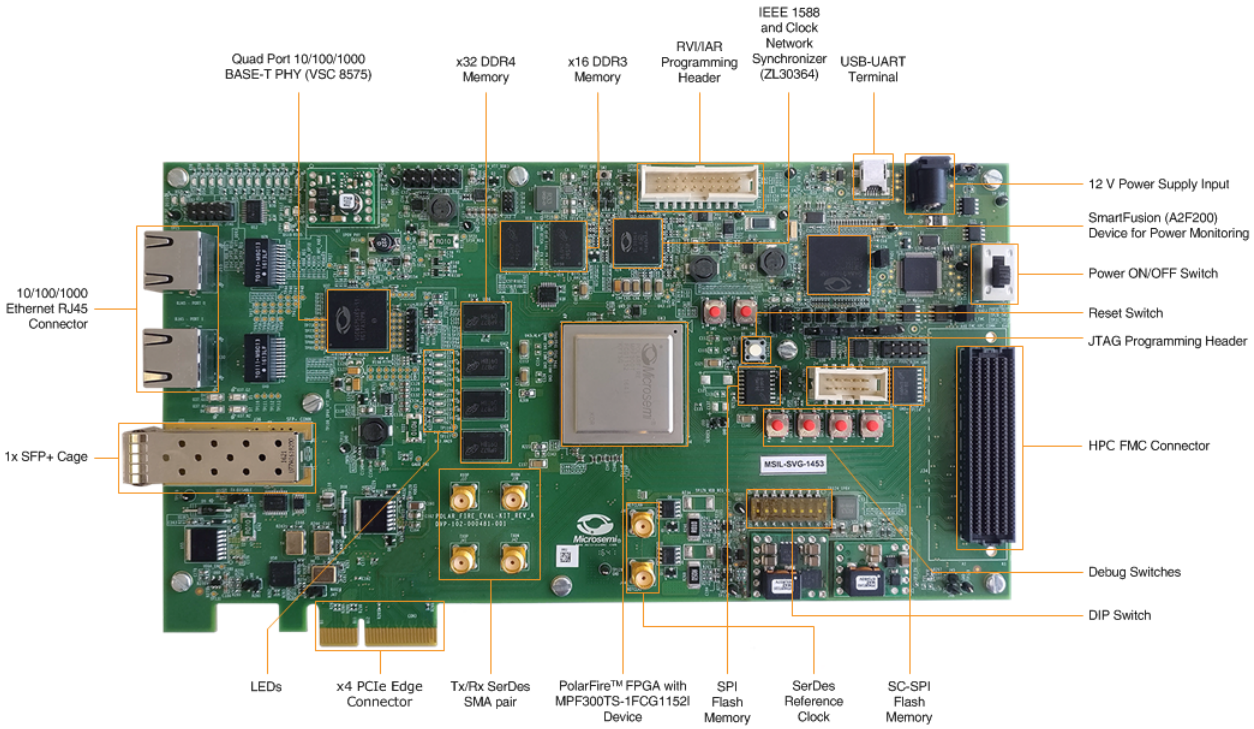
For design files, contact Microsemi Technical Support Team at *soc_tech@microsemi.com*.

2.4 Interoperability Test Setup

The interoperability test is performed on the PolarFire Evaluation Kit board with the MPF300TS-1FCG1152I device as shown in Figure 1, page 3 and Texas instruments ADS54J60 EVM as shown in Figure 2, page 3. The ADS54J60 is a low-power, wide-bandwidth, 16-bit, 1.0 - GSPS, dual-channel, analog-to-digital converter (ADC). The device supports the JESD204B serial interface with data rates up to 10 Gbps, supporting two or four lanes per ADC. The design for the test is developed using the Libero SoC Polarfire software by instantiating the CoreJESD204BRX IP and other required IP cores in SmartDesign. The register configuration of ADS54J60 is done using ADS54Jxx GUI by Texas instruments. ADS54J60EVM is used to evaluate the ADS54J60. It is connected to the FPGA mezzanine card high pin count (FMC HPC) connecter of the PolarFire Evaluation Kit.

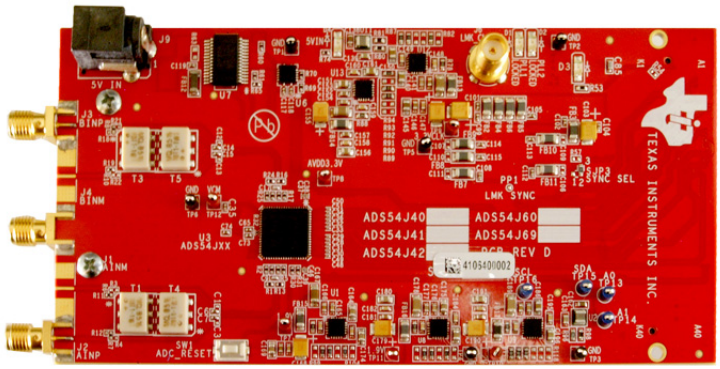
The following figure shows the hardware setup.

Figure 1 • **PolarFire Evaluation Kit**



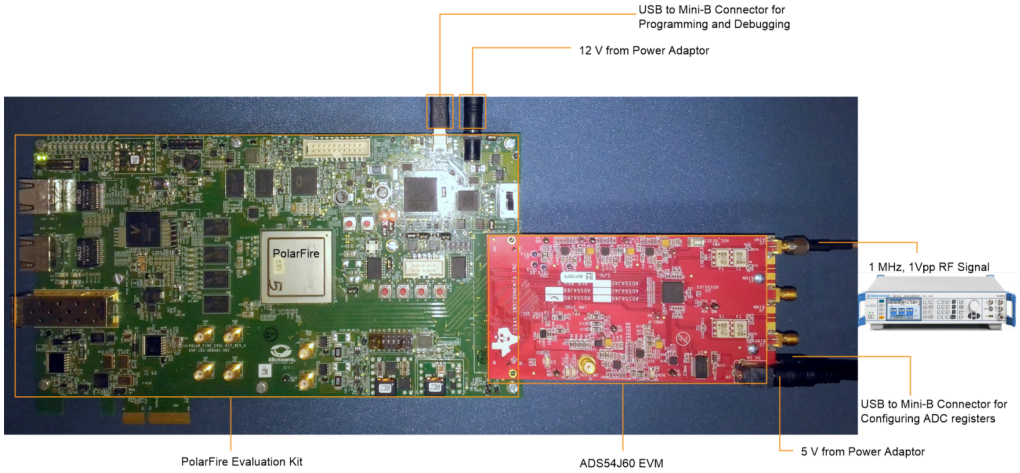
The following figure shows the ADS54J60 EVM evaluation board.

Figure 2 • **ADS54J60 EVM**



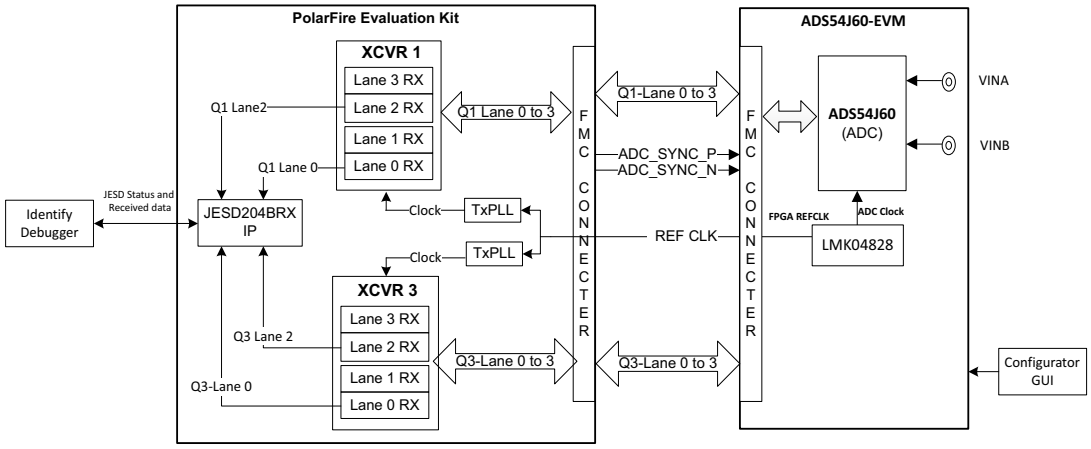
The following figure shows the hardware setup for Interoperability test.

Figure 3 • **Hardware Setup for Interoperability Tests with ADS54J60**



The following block diagram illustrates how signals flow in the hardware setup for interoperability tests.

Figure 4 • **Block Diagram of Interoperability Tests**



2.5 Interoperability Test Settings

CoreJESD204BRX and ADC-ADS54J60 are configured, as shown in the following table.

Table 2 • **CoreJESD204BRX and ADC-ADS54J60 Configurations**

Parameter	CoreJESD204BTX	ADC-ADS54J60	Description
SCR	0/1	0/1	Scramble enable/disable
L	4	4	Lanes
F	4	4	Octets per frame
K	32	32	Frames per multi-frame
M	2	2	Converters
CS	0	0	Control bits per sample
N	16	16	Sample resolution
N'	16	16	Sample envelope
S	4	4	Samples per converter per frame
HD	0	0	High density mode
CF	0	0	Control bits per frame
SUBCLASSV	0/1	0/1	0×0/0×1

2.6 ADC-ADS54J60 Interoperability Tests

The following interoperability tests were performed on **CoreJESD204BRX** and **ADC-ADS54J60**:

- Test 1: Data Link Layer—Code Group Synchronization, page 6
- Test 2: Data Link Layer—Initial Lane Alignment Sequence, page 7
- Test 3: Receiver Transport Layer, page 8
- Test 4: Descrambling, page 8
- Test 5: Deterministic Latency, page 9

2.6.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify Debugger is used to monitor the operation of the receiver data link layer. The following table shows the data link layer—code group synchronization (CGS) test results.

Table 3 • **Data Link Layer—Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC1.1	Check if the receiver asserts SYNC_N signal when the link is down.	CoreJESD204BRX_0 -> SYNC_N signal is observed in Identify Debugger.	SYNC_N is low.	Passed
ADC1.2	Check if SYNC_N request is de-asserted on receiving at least four successive /K/ characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], and SYNC_N signals are observed in Identify Debugger.	K28.5 or /K/ character (0 × BC) is observed on DATA_OUT and SYNC_N is de-asserted on receiving at least four successive /K/ characters.	Passed
ADC1.3	Check the full code group synchronization at receiver on receiving another four successive 8B/10B characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], SYNC_N and CGS_ERR[3:0] signals are observed in Identify Debugger	CGS error is not asserted	Passed

2.6.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table lists the data link layer—initial lane alignment sequence (ILAS) test results.

Table 4 • **Data Link Layer—Initial Lane Alignment Sequence Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC2.1	Check if the ILA phase starts after the CGS phase.	CoreJESD204BRX_0-> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0], SOF_0[3:0], SOF_1[3:0], SOF_2[3:0], SOF_3[3:0] signals are observed in Identify Debugger.	Multi-frame starts with 0×1C and is aligned to SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0]	Passed
ADC2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0], SOF_0[3:0], SOF_1[3:0], SOF_2[3:0], SOF_3[3:0], and LINK_CD_ERROR[3:0] signals are observed in Identify Debugger.	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data.	Passed

2.6.3 Test 3: Receiver Transport Layer

The following table shows the receiver transport layer test results.

Table 5 • **Receiver Transport Layer Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC3.1	Check data integrity in test mode	ADC is configured in long transport layer test pattern mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals are observed in Identify Debugger.	Received signal correlates with the transport layer test pattern.	Passed
ADC3.2	Check data integrity in normal mode	ADC is configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0] signals are observed in Identify Debugger.	Received signal correlates with the input signal given for ADC sampling.	Passed

2.6.4 Test 4: Descrambling

Scrambler is enabled in ADC, and descrambler is enabled in CoreJESD204BRX IP. The following table shows the descrambling test results.

Table 6 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC4.1	Check descrambler functionality.	ADC is configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals are observed in Identify Debugger.	Received signal (monitored in identify tool) correlates with the analog sine wave input given for ADC sampling.	Passed

2.6.5 Test 5: Deterministic Latency

CoreJESD204BRX IP and ADS54J60 are configured in **Subclass 1** mode. The following table shows the JESD204B deterministic latency measurement test results.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results – Subclass 1 Mode**

Test Case	Objective	Description	Passing Criteria	Results
ADC5.1	Check local multi-frame counter (LMFC) alignment	CoreJESD204BRX_0 -> clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger.	SYSREF_IN is aligned to clkgen_lmfc.	Passed
ADC5.2	SYSREF capture	CoreJESD204BRX _0 -> c2l_mf_phase, and SYSREF_IN signals are observed in Identify Debugger.	LMFC counter restarts after the SYSREF_IN capture.	Passed
ADC5.3	Check latency from start de-assertion of SYNC_N to first user data output.	Check if latency is fixed for every link reset/initialization.	Latency must be same for link reset/initialization (around 10940 ns)	Passed
ADC5.4	Check the data latency during user data phase.	Check if the data latency is fixed during the user data phase. CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals are observed in Identify Debugger.	The user data is seen without distortion.	Passed