Power Matters.™

Radiation-Capable Power Supply Solutions for Space Platforms

Presenter: Brian Wilkinson, Sr. Director of Applications Engineering

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Radiation-Capable Components and Space Reference Design

- Company Overview
- Portfolio Breadth
- Introduction of a Space Reference Platform concept.
- RTG4 limits and good practices.
- Utilizing the SA50 DC-DC and MHP8565A POL.
- Performance characteristics of MHP8565A for 1.0V Vout.
- Alternative Rad Tolerant Power Distribution schemes.
- Summary.

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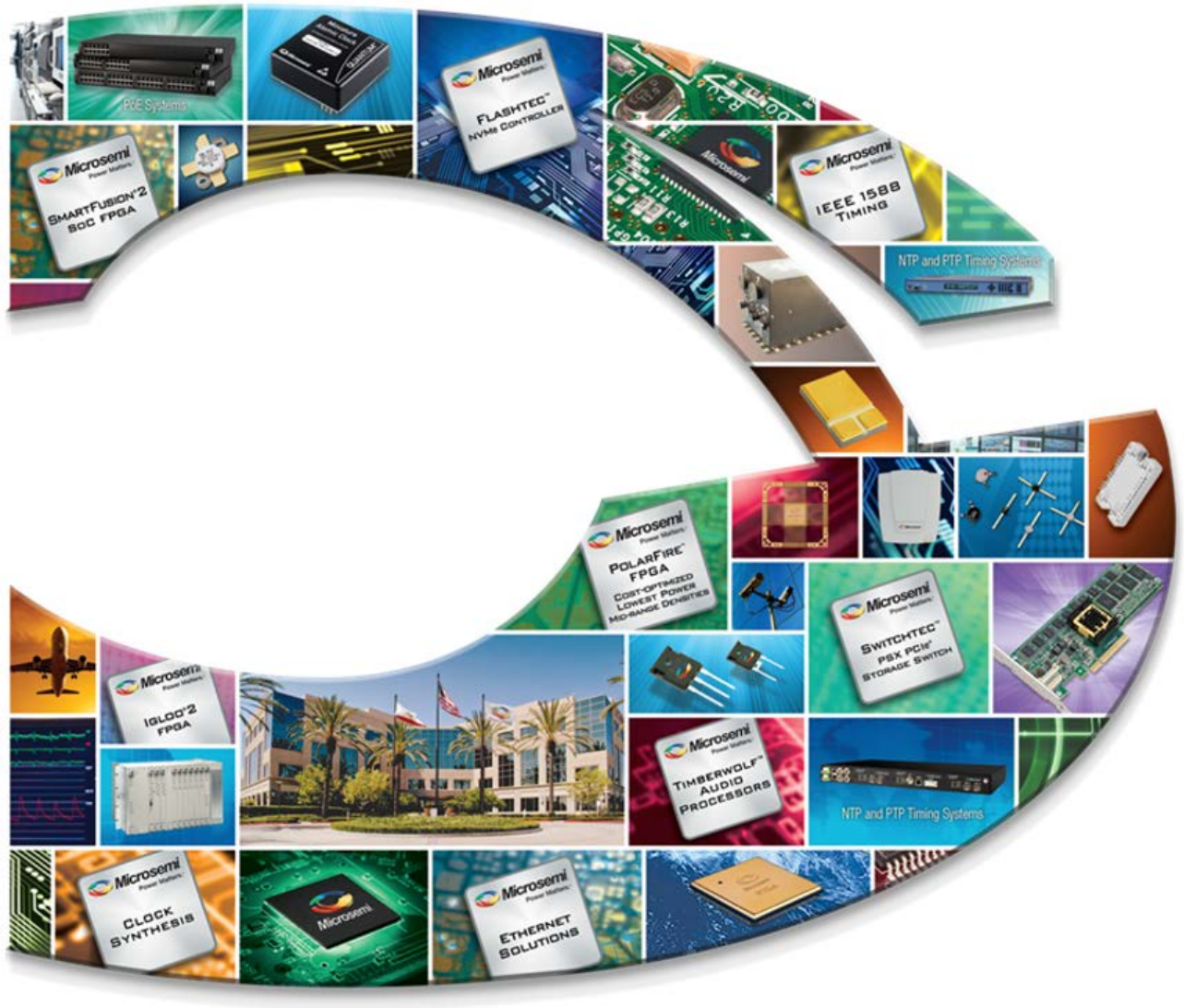
Company Overview



- Leading-Edge Semiconductor Solutions Differentiated by:
  - Performance
  - Reliability
  - Security
  - Power
- Solid Financial Foundation
  - FY2016 Revenue: $1.6B
  - 4800 employees today
- Major Focus Products
  - FPGA and ASIC
  - Timing and OTN
  - Mixed-Signal and RF
  - Switches and PHYS
  - Storage Controllers
  - Discretes and integrated power solutions

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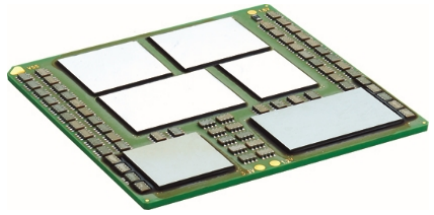
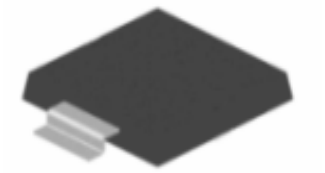
Microsemi Space Pedigree





Extensive Space Heritage

- Developing space solutions for six decades
- Proven track record of innovation, quality, and reliability

Broad Solutions Portfolio

- Power, mixed-signal, and digital, for bus and payload applications

Expanding our Product Portfolio through Continuous Innovation

Partner for the Long Run

- 60 Year space heritage

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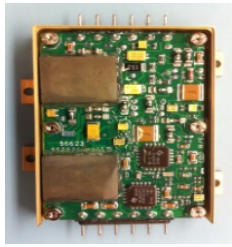
Delivering Comprehensive Space Portfolio

Radiation-Tolerant FPGAs	High Performance, High Density, Low Power TID up to 300 Krad, SEL Immune RTG4 FPGAs up to 300 MHz and 150K LE RTProASIC3, RTAX and RTSX-SU QML Qualified
Rad-Hard Mixed Signal Integrated Circuits	Telemetry and Motor Control Space System Managers High Side Drivers Regulators and PWMs Extensive Custom IC Capability
Space Qualified Oscillators	Ovenized Quartz Oscillators Hybrid Voltage Controlled and Temperature Compensated Crystal Oscillators Cesium Clocks
Rad-Hard Power Solutions	Rad-hard JANS Diodes, Bi-Polar Small Signal Transistors, and MOSFETs Rad-hard Isolated DC-DC Converter Modules Custom Power Supplies 2 W to > 5 KW Linear and POL Hybrids Electromechanical Relays



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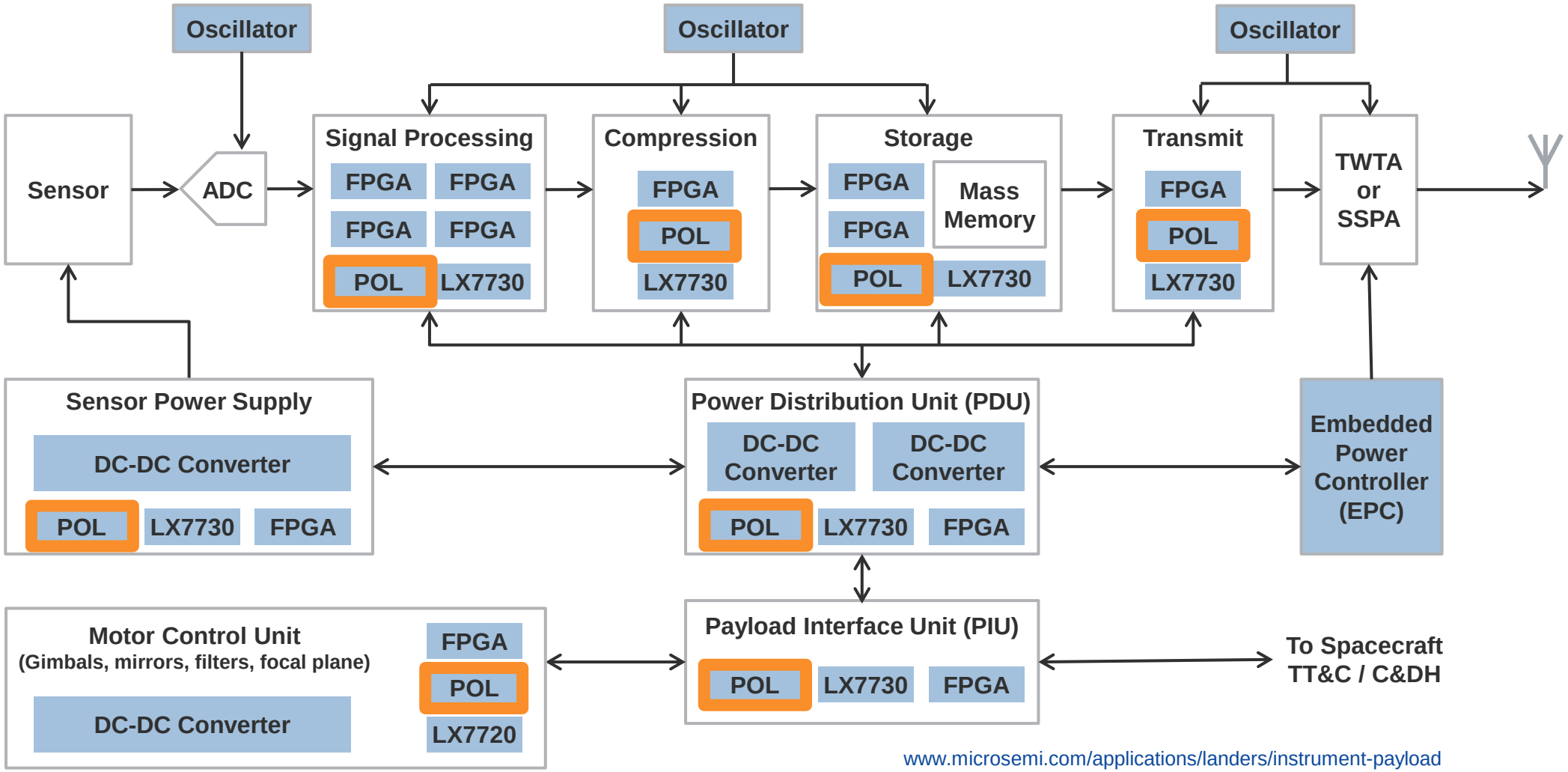
Portfolio Breadth: Example Signal Processing Payload Power

- LDO Regulators and Switchers



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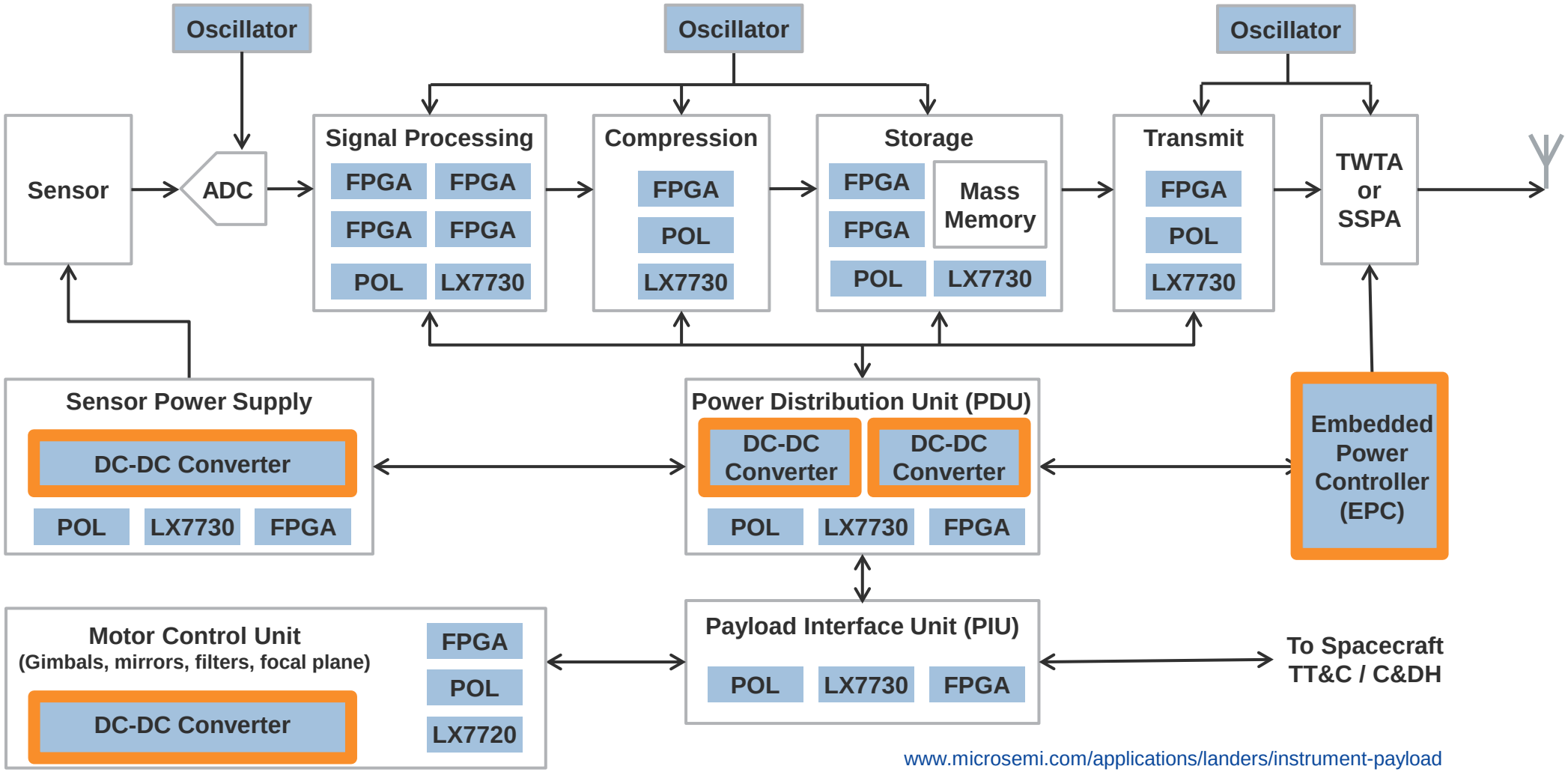
Portfolio Breadth: Example Signal Processing Payload Power

- Integrated Power Solutions and Discretes



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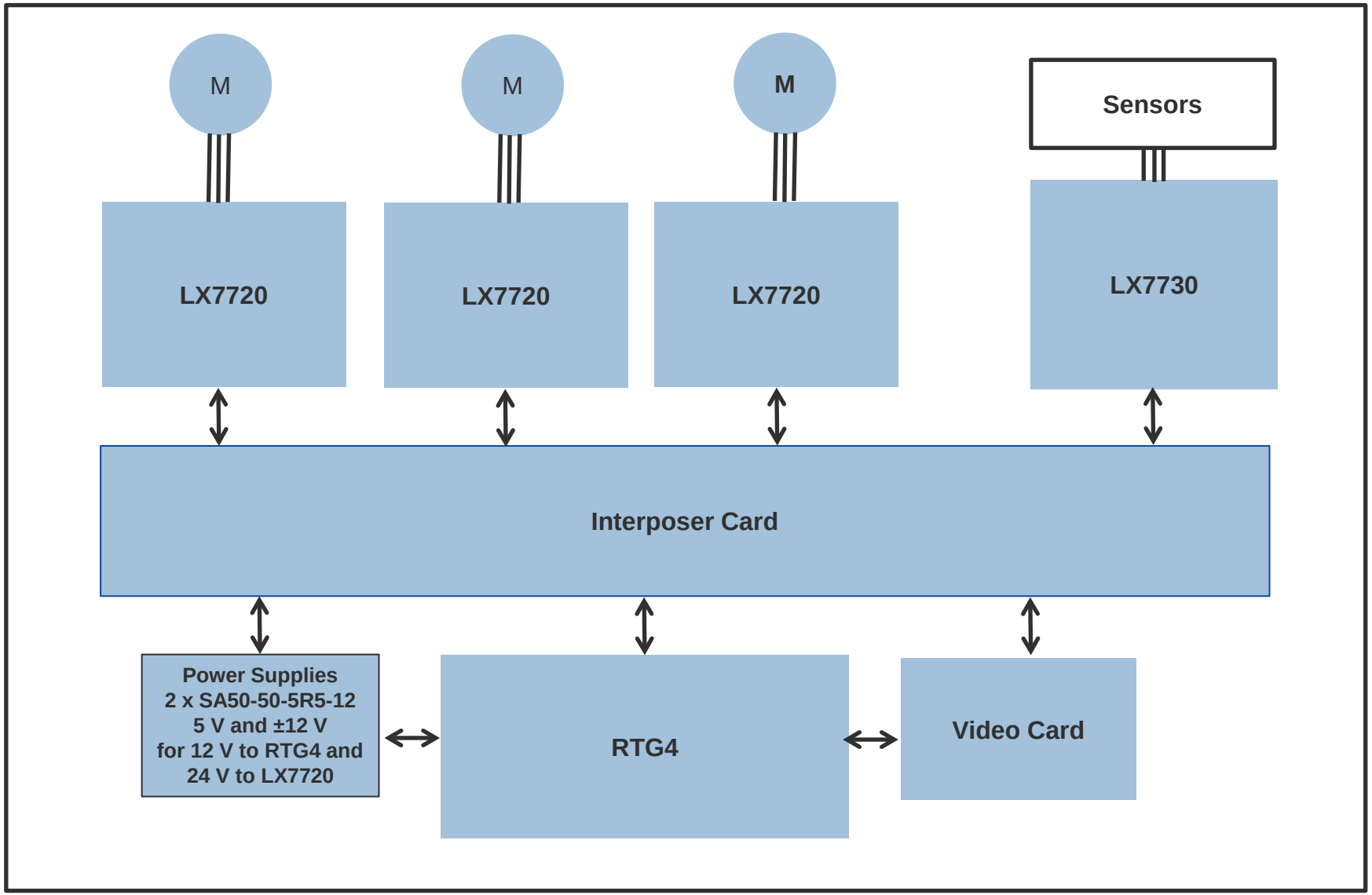
Microsemi Space Solution Reference Platform Concept



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Let’s Remind ourselves of RTG4 Power Requirements

- Core power rail limits
- Power sequencing
- Power estimator
- Decoupling practices

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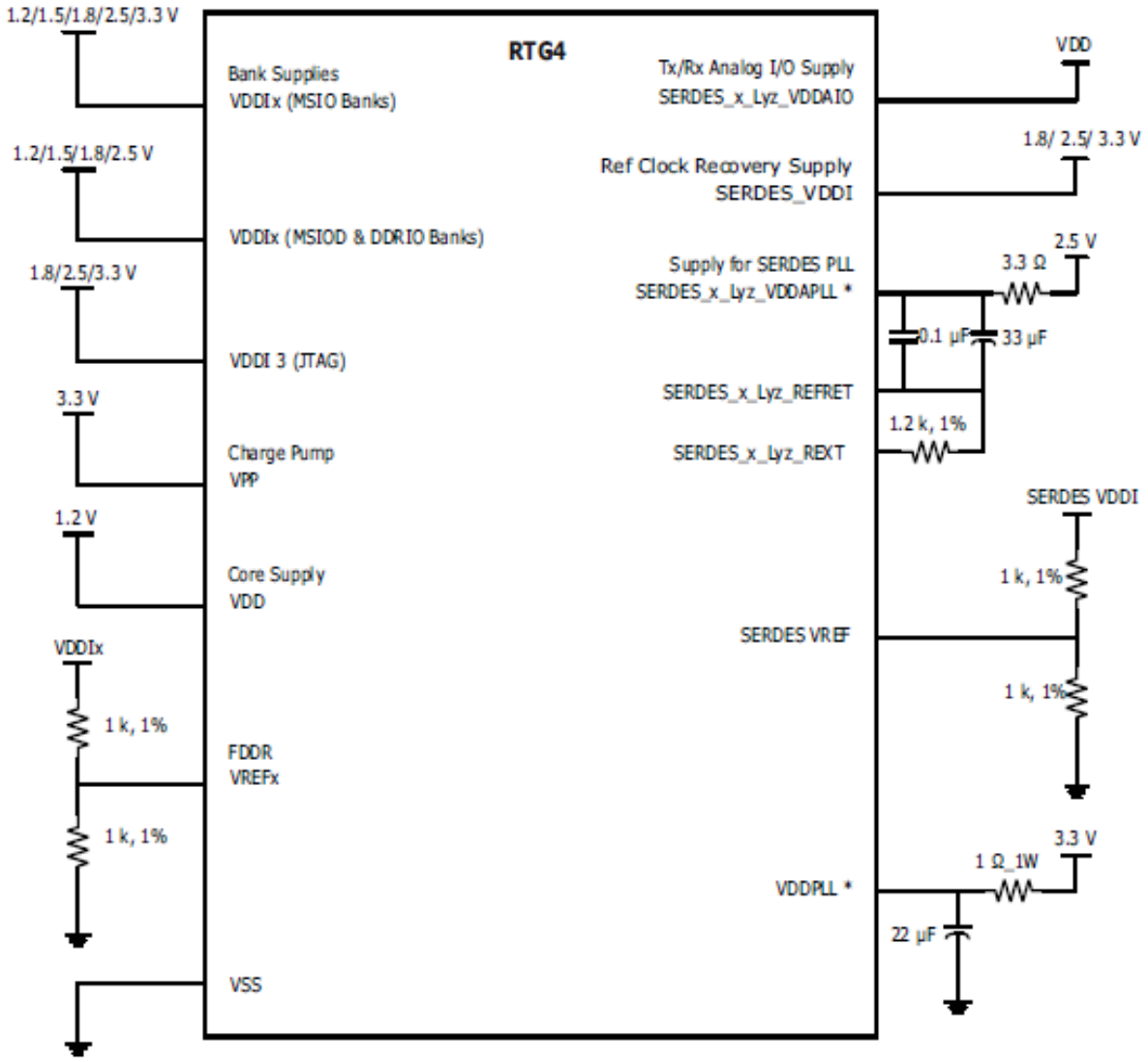
RTG4 Power Supplies- recommended conditions and limits



Supply	Voltage	Description
VDD	1.2 V	Core supply voltage
VPP	3.3 V	Power supply for device charge pumps
VDDPLL	3.3 V	Power for eight corner PLLs, PLLs in SerDes PCIe/PCS blocks, and FDDR PLL
VDDIx	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	Bank supplies
VREFx	0.5 * VDDIx	FDDR reference voltage
SERDES_x_Lyz_VDDAIO	1.2 V	TX/RX analog I/O voltage for SerDes lanes
SERDES_x_Lyz_VDDAPLL	2.5 V	Analog power for SERDES TXPLL and CDRPLL
SERDES_VDDI	1.8 V, 2.5 V, or 3.3 V	Power for SerDes reference clock receiver supply.
SERDES_VREF	0.5 * SERDES_VDDI	External differential receiver reference voltage for SerDes reference clocks

Table 2 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC FPGA core supply voltage. Must always power this pin.	-0.3	1.32	V	

Table 3 • **Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Units
T_J	Operating Junction Temperature	-55	25	125	°C
	Programming Junction Temperature	0	25	85	°C
VDD	DC FPGA core supply voltage. Must always power this pin.	1.14	1.2	1.26	V

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RTG4 Ratings, Power-Up and Power-Down Sequence

POWER-UP SEQUENCE

VDDPLL - NO power-up sequence if the device is held in reset by asserting DEVRST_N until VDDPLL supplies reach their minimum recommended level as shown in the datasheet and guidelines If not the following power-up requirements apply:

- All PLLs are held in reset until VDDPLL supply reaches its minimum recommended level OR.
- VDDPLL must NOT be the last supply to ramp up and must reach its minimum recommended level before the last supply (VDD or VDDIx) starts ramping up.

SERDES_x_Lyz_VDDAIO - NO power-up sequence if SERDES_x_Lyz_VDDAIO supplies are tied to VDD If not:

- SERDES_x_Lyz_VDDAIO and VDD cannot be tied together, SERDES_x_Lyz_VDDAIO must be powered up at the same time as VDD

  All IO must be powered up before the reset is released.

POWER-DOWN SEQUENCE

NO power-down sequence if an external 1-Kohm pull-up or pull-down resistor is used for each critical output which cannot tolerate an output glitch during power-down or DEVRST_N assertion. If a resistor cannot be used, the following requirements apply:

- VDDIx supplies are powered down first all the way to 0V OR.
- VPP is powered down last.
- If VPP or VDD falls below the minimum recommended level, both VPP and VDD must be powered down all the way to 0V before powering back up. Powering down VPP without powering down VDD is not allowed. VPP and VDD can be powered down in any sequence.

For more information, refer to the AC439: Board Design Guidelines for RTG4 FPGA application note.

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Power Supply Decoupling Capacitors

- Proper on-board power supply decoupling is required.
  - Keep decoupling caps close to pin (use 402's where possible on underside).
  - Distribute overall decoupling capacitance around the device perimeter.
  - Use blind vias to remove crosstalk risk and cap surface mount area.
  - Use larger power vias to reduce inductance—especially for high layer count boards.

- Precious metal electrode (PME) decoupling caps within the FPGA package enhance overall PCB decoupling.

- Refer to the AC439 RTG4 Board Design Guidelines application note for capacitor values inside package and recommended external capacitors to be placed on PCB.

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Radiation-Tolerant Power Supplies

- Microsemi provides radiation-tolerant components that can be used to supply power to RTG4 FPGAs.

- Engineers should consider the following when selecting power supply components:

  - Calculate required power of the RTG4 device.

    – PowerCalc spreadsheet, SmartPower tool in Libero design software

  - Select an appropriate radiation-tolerant regulator that can supply the required power and meet all power requirements of RTG4.
    – Radiation-tolerant linear regulator (Microsemi)
    – Radiation-tolerant switching regulator isolated or non-isolated (Microsemi)

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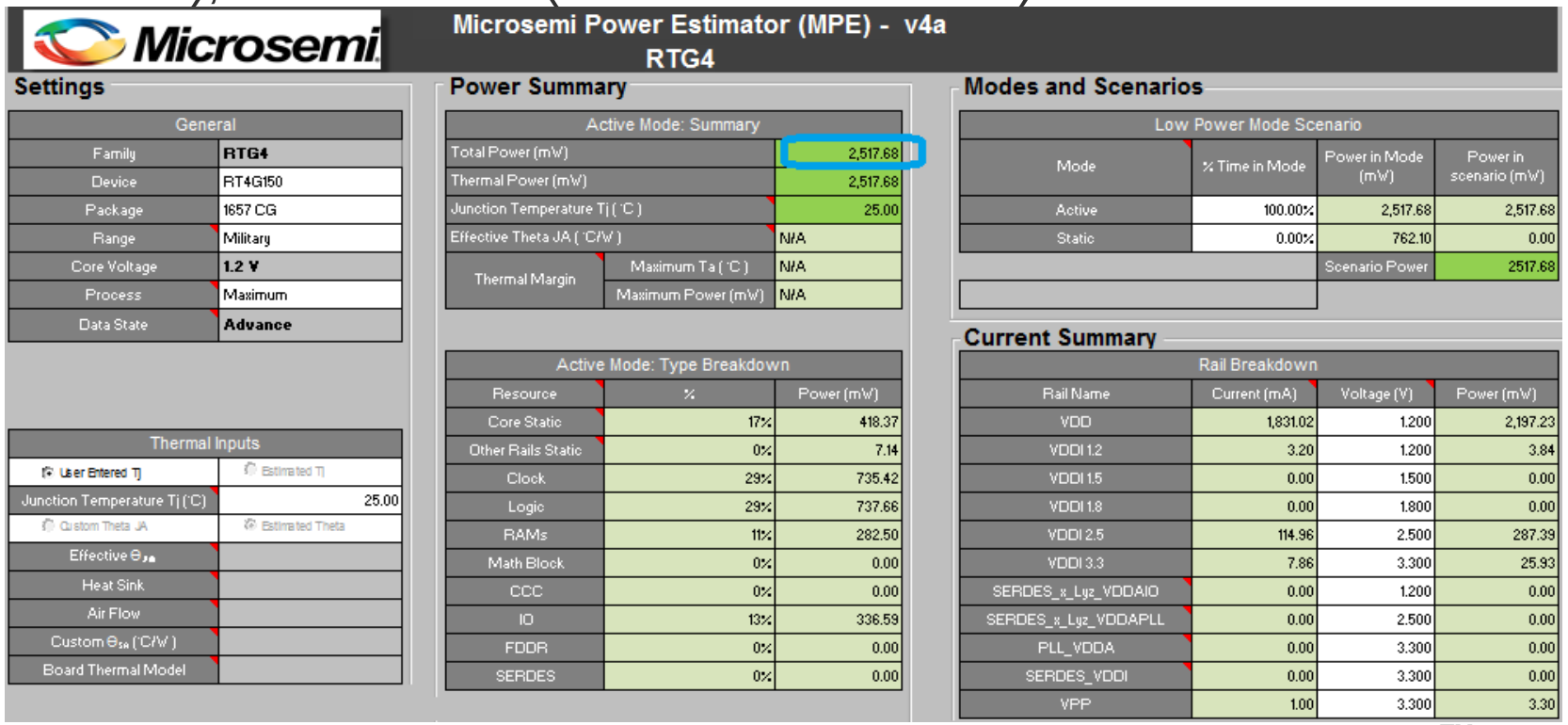
Current Requirements

- Use RTG4 power calculator to estimate power required.
  - Available on Microsemi website: RTG4 Power Calculator.
  - Enter specific details for your design.
  - Example:
    - For 99% utilized RT4G150 total 2.5 W.
    - Two fast clocks (150 MHz to 250 MHz), 2 slow clocks (25 MHz and 50 MHz)
    - 496 I/O (400 LVCMOS, 66 PCI and 32 LVDS)
    - Eight lanes of transceivers (2.5 Gb/s)



Microsemi Power Estimator (MPE) - v4a
RTG4

Settings

General	
Family	RTG4
Device	RT4G150
Package	1657 CG
Range	Military
Core Voltage	1.2 V
Process	Maximum
Data State	Advance

Thermal Inputs	
User Entered Tj	Estimated Tj
Junction Temperature Tj (°C)	25.00
Custom Theta JA	Estimated Theta
Effective Θ_{JA}	
Heat Sink	
Air Flow	
Custom Θ_{SA} (°C/W)	
Board Thermal Model	

Power Summary

Active Mode: Summary		
Total Power (mW)		2,517.68
Thermal Power (mW)		2,517.68
Junction Temperature Tj (°C)		25.00
Effective Theta JA (°C/W)		N/A
Thermal Margin	Maximum Ta (°C)	N/A
	Maximum Power (mW)	N/A

Active Mode: Type Breakdown		
Resource	%	Power (mW)
Core Static	17%	418.37
Other Rails Static	0%	7.14
Clock	29%	735.42
Logic	29%	737.66
RAMs	11%	282.50
Math Block	0%	0.00
CCC	0%	0.00
IO	13%	336.59
FDDR	0%	0.00
SERDES	0%	0.00

Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (mW)	Power in scenario (mW)
Active	100.00%	2,517.68	2,517.68
Static	0.00%	762.10	0.00
		Scenario Power	2517.68

Current Summary

Rail Breakdown			
Rail Name	Current (mA)	Voltage (V)	Power (mW)
VDD	1,831.02	1.200	2,197.23
VDDI 1.2	3.20	1.200	3.84
VDDI 1.5	0.00	1.500	0.00
VDDI 1.8	0.00	1.800	0.00
VDDI 2.5	114.96	2.500	287.39
VDDI 3.3	7.86	3.300	25.93
SERDES_x_Lyz_VDDAIO	0.00	1.200	0.00
SERDES_x_Lyz_VDDAPLL	0.00	2.500	0.00
PLL_VDDA	0.00	3.300	0.00
SERDES_VDDI	0.00	3.300	0.00
VPP	1.00	3.300	3.30

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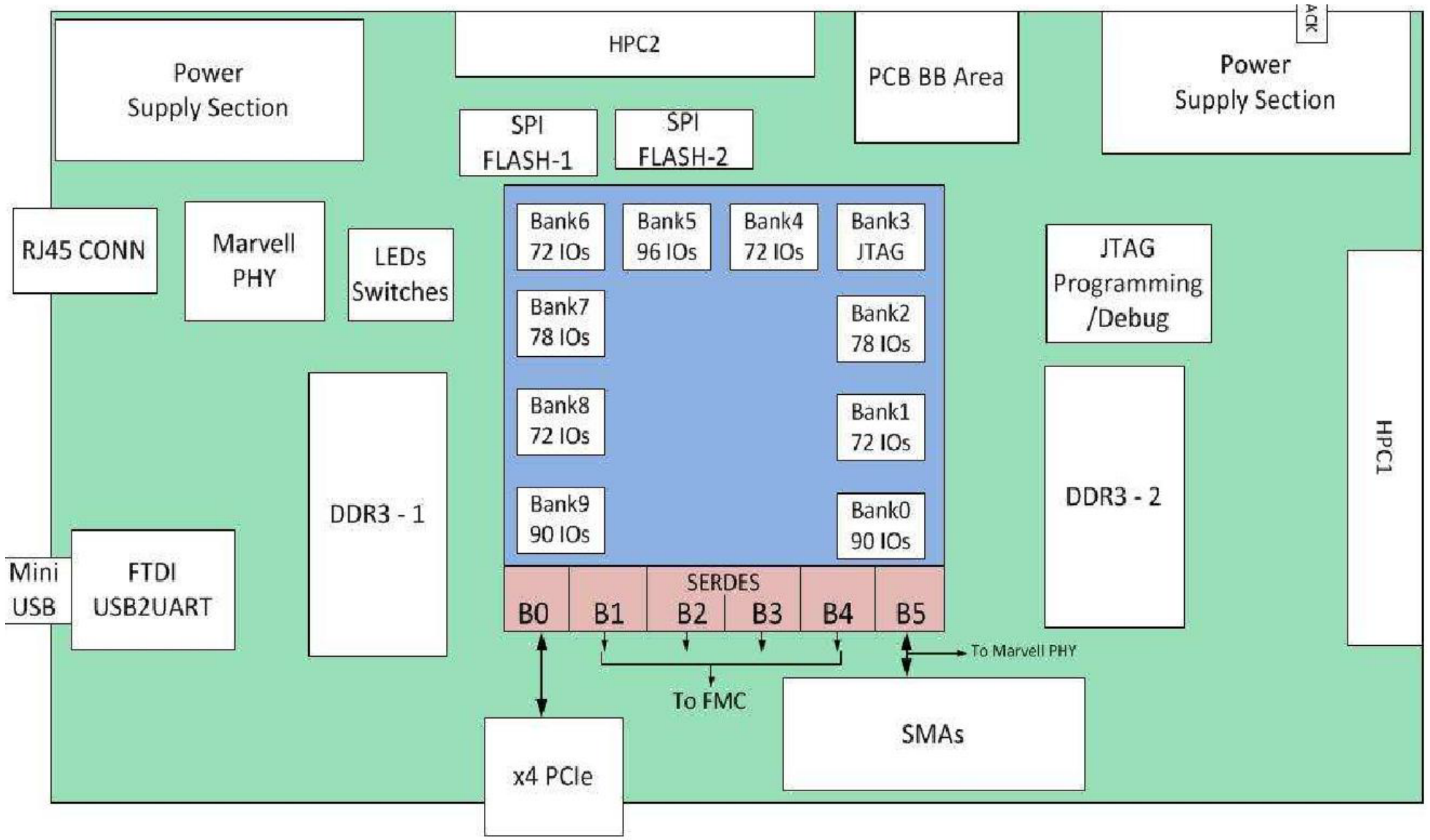
Existing RTG4 Evaluation Board Block Diagram



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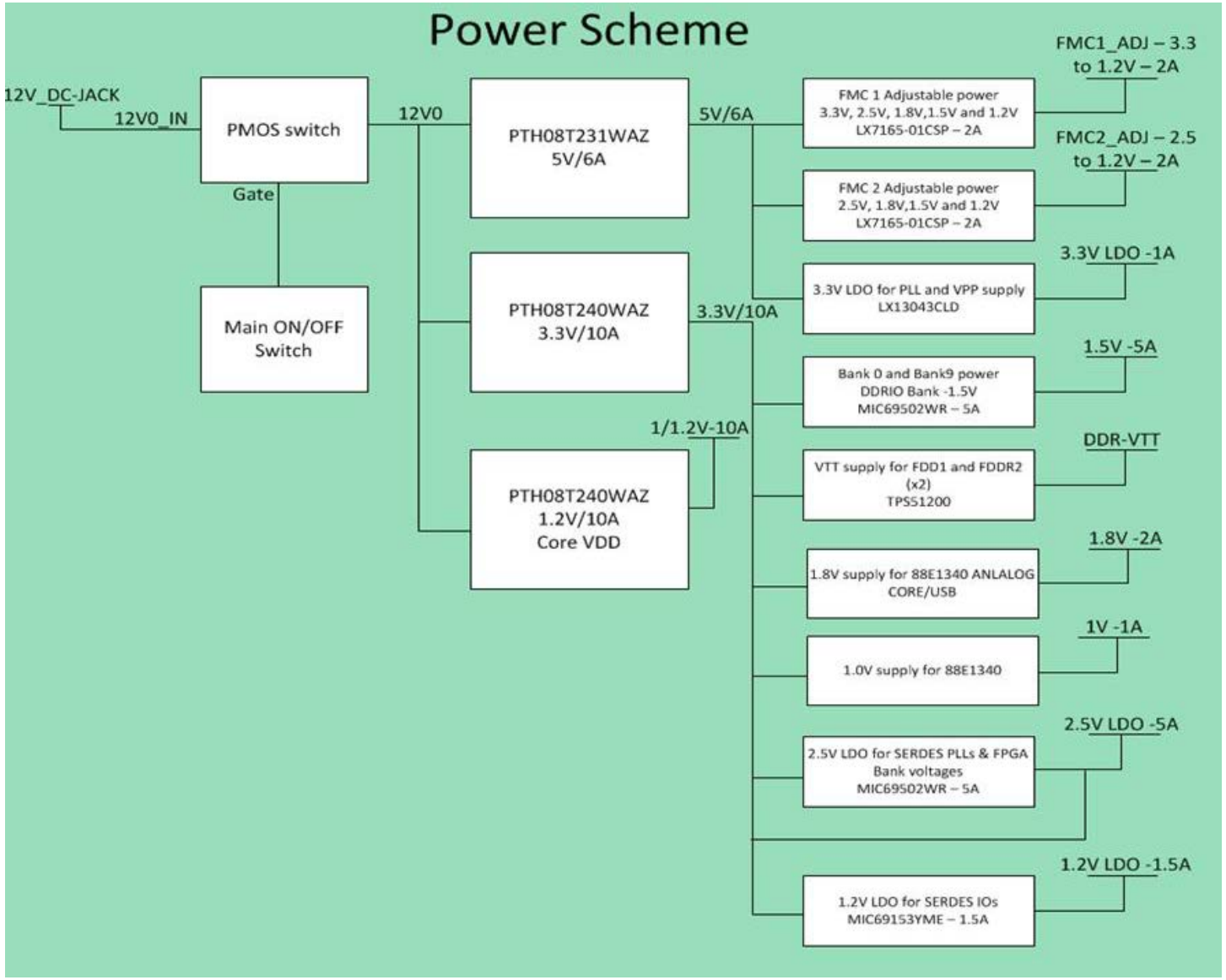
RTG4 Evaluation Board Commercial Non-RH Device Power Scheme



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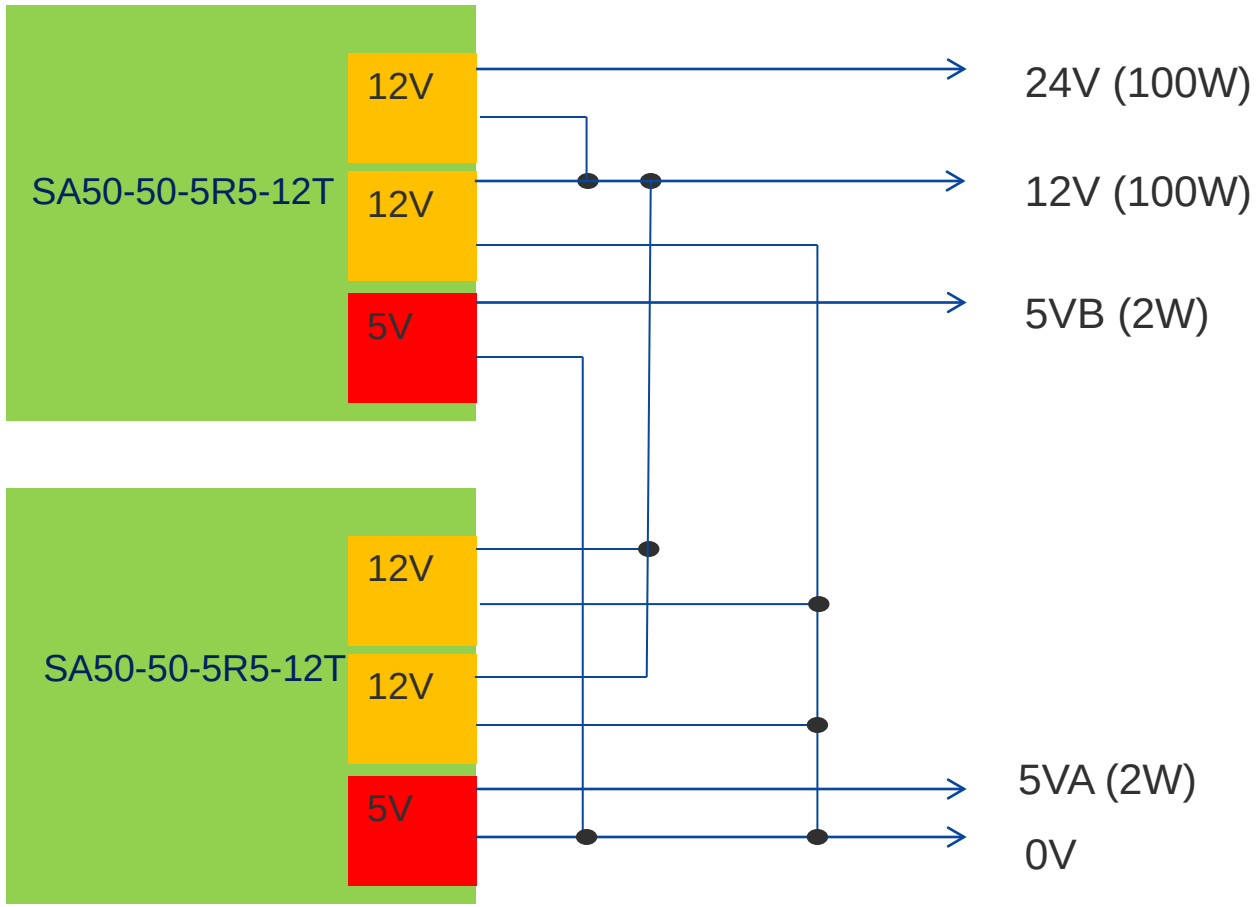
Reference Platform Main Power Configuration example using two SA50 modules



- 2 x 5V rails to be loaded by >2W each (preload or system load)
- 3 x 12V rails connected in parallel for up to 100W
- 1 x 24V rail connected in cascade with 12V bus for up to 100W
- Power will *AUTOMATICALLY AND DYNAMICALLY* distribute amongst the various loads due to the inherent cross regulation characteristic of the SA50-50-5R5-12T

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SA50 Series RH Isolated DC-DC Features—EAR99 cont'd.

Additional Key Features — Flexibility

The SA-50 allows for flexibility in the power system by making use of additional features and characteristics of the design.

Remote Sense Function

The remote sense pin can provide accurate regulation at the point of loading.

- Keep the remote sense terminal connected to a single point and as close as possible to the point where regulation is desired to be maintained.
- Parallel operation - all remote sense pins should be connected together and tied to the remote point to be regulated. Connect the return remote sense return terminals to a single point, as close as possible to the negative load terminal.

Parallel Operation

- Up to five modules may be connected in parallel.
- Current sharing accuracy is 10% at maximum load.

Additional Key Features — Flexibility

Remote Adjust

- The remote adjust pin allows the output voltage to be adjusted plus or minus 10% from the nominal voltage. by use of an external R-ADJUST resistor for the set point for the internal TL1431 voltage reference.

Isolated Sync Input

- The power supply's internal clock may be synchronized to an external signal. The sync input circuit is magnetically isolated from all other circuits and chassis.
- The sync functionality remains the same for a system of paralleled modules and can be applied to all or any one of the modules..

Auxiliary source impedance

- Sharing.

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Demonstrator Unit

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MHP8565xx PoL Performance

The MHP856xx series key performance parameters over the datasheet-specified operating range are shown as follows for the MHP8565A 5 V input version.

Table 2 – ELECTRICAL CHARACTERISTICS (See Note 5)
(T_A = -55°C to +125°C unless otherwise noted)

Parameters / Test Conditions	Symbol	Value			Unit
		Min.	Nom	Max.	
Minimum input Voltage (Note 8)	Vin(min)	4.5			V
Output Voltage Accuracy Vo = 1.21V	Vout	1.19		1.23	V
Post 100K Irradiation, 25°C	Vout	1.17		1.24	V
Line regulation 4.5V < Vin < 5.5V Vo = 1.21V	Kvi	-0.5		+0.5	%
Load regulation 1A < Iout < 2A	Kvo	-1		+1	%
Current Limit Vo = 2.5V	I_{CL}	3.5	5		A
Post 100K Irradiation, 25°C		3.0			
Input Voltage on Enable pin to guarantee shutdown Io = 0A (Note 4)	Vshdn	0.13	0.40	0.60	V

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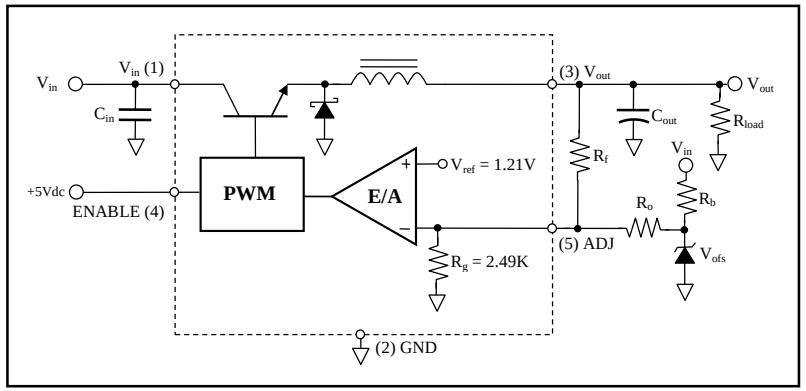
Setting Output Voltage Below 1.21 V for the MHP8565A

- The output voltage may be set either higher than or equal to the internal reference (using a single resistor), or lower than the internal reference using a precision reference and two resistors.
- A DC offset reference source and offset resistor must be added to the feedback circuit below 1.21V. This situation is illustrated as below.
- R_b is the biasing resistance for the reference source—either a temperature-compensated Zener diode (1N829 or equivalent) or a shunt voltage reference integrated circuit (for example, TLC1431 or equivalent).
- V_{ofs} will be dependent upon the input voltage available: a good rule of thumb is to make the offset reference voltage approximately one-half of the nominal input voltage.
- The offset resistance, R_o, provides a fixed DC current to the MHP8565A internal error amplifier.

Feedback Configuration for $V_{out} < V_{ref}$



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Setting Output Voltage Below 1.21 V for the MHP8565A (continued)

- The corresponding output voltage is given by

$$V_{out} = V_{ref} - \left(\frac{(V_{ofs} - V_{ref}) \bullet R_f}{R_o} \right) + \left(\frac{V_{ref} \bullet R_f}{R_g} \right)$$

- Keep V_{out} equal or greater than 1.00 Vdc in order to avoid erratic operation due to the onset of current fold-back limiting and the internal reduction of the switching frequency of the PWM.

- To keep the feedback resistance, R_f, to a reasonable value that the offset resistance, R_o, be kept to a value between 1.00K and 2.49K for V_{ofs}= 2.5 Vdc and between 2.49K and 4.99K for V_{ofs}= 6.2 Vdc.

- Regardless of the offset voltage, the resultant value of R_f should always be kept above 100 ohms to maintain a reasonable output voltage accuracy, and the value of R_o should be adjusted accordingly.

- The output of the MHP8565A is a current source, and not a current sink.. In order to prevent light load instabilities and inaccuracies in situations where $V_{out} < V_{ref}$ it is required that the minimum load provided to the MHP8565A is:

$$R_{load}(\min) = \frac{0.5 \bullet V_{out}}{\left(\frac{(V_{ref} - V_{out})}{R_f} \right)}$$

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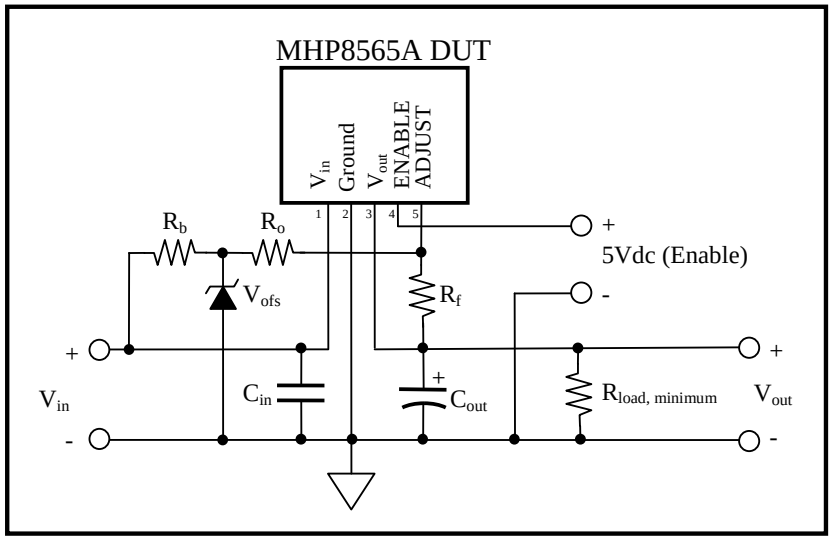
MHP8565A Performance Summary for 1.0 V V_{OUT}

In order to verify the performance of the MHP8565A Single 3.5 Amp POL Regulator Hybrid with the output voltage set to 1.00 Vdc, devices were subjected to parametric evaluation testing with input voltages of 5.0 Vdc nominal and 12.0 Vdc nominal.

The MHP8565A devices were subjected to the following test evaluation circuit configuration during testing:

MHP8565A Test Circuit



C_{in}= 50 uF ceramic, C_{out}= 440 uF tantalum electrolytic, and the remainder of the components are identified versus input voltage as shown in Table I on the next slide.

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MHP8565A Performance Summary for 1.0 V V_{OUT} cont'd.

Table I. Component Values Versus Input Voltage

Component/Value	V_{in}= 5 Vdc	V_{in}= 12 Vdc
Rb	2.20 KΩ	1.10 KΩ
Ro	1.50 KΩ	3.74 KΩ
Rf	562 Ω	249 Ω
Rload, minimum	1.33 KΩ	590 Ω
Vofs	2.50 V	6.2 V

Tests Performed

The following tests identified in Table II were performed on the MHP8565A device in order to observe parametric performance with the output voltage set to 1.00 Vdc.

Table II. MHP8565A Parametric Tests Performed

Test	Conditions
Load regulation	0 A < I_{out} < 5 A, 0.5 A increments
Line regulation	4.5 V < V_{in} < 5.5 V for 5 V input 10.5 V < V_{in} < 13.5 V for 12 V input
Output noise and ripple	0 A < I_{out} < 4 A, 1 A increments
Output transient voltage	1 A to 2 A deviation 1 A to 3 A deviation
Turn-on transient	I_{out} = 0 A I_{out} = 3.0 A

Test Hardware

The MHP8565A samples were tested on the hardware printed circuit boards as shown on the next slide.

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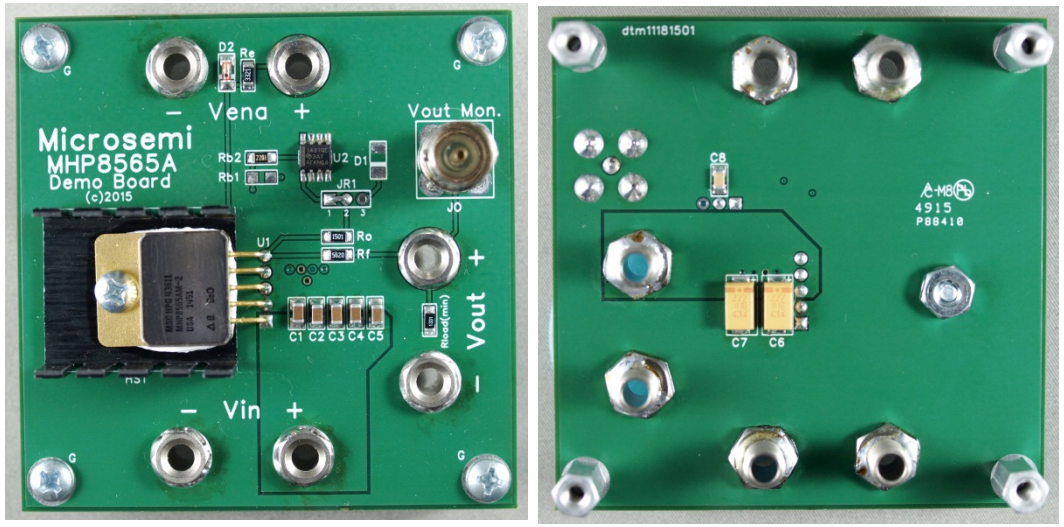
MHP8565A Performance Summary for 1.0 V V_{OUT} cont'd.

MHP8565A Test PCB Hardware



Test Results and Analysis:
Two devices were subjected to the previous parametric tests as detailed in Table II. Serial number 000016 was used for the 5 V input tests and serial number 000012 was used for the 12 V input tests. Both devices were MHP8565AM-2 types.

The following tests were performed:

- Load current regulation
- Line voltage regulation
- Output noise and ripple voltage
- Output transient voltage
- Output turn-on transient voltage event

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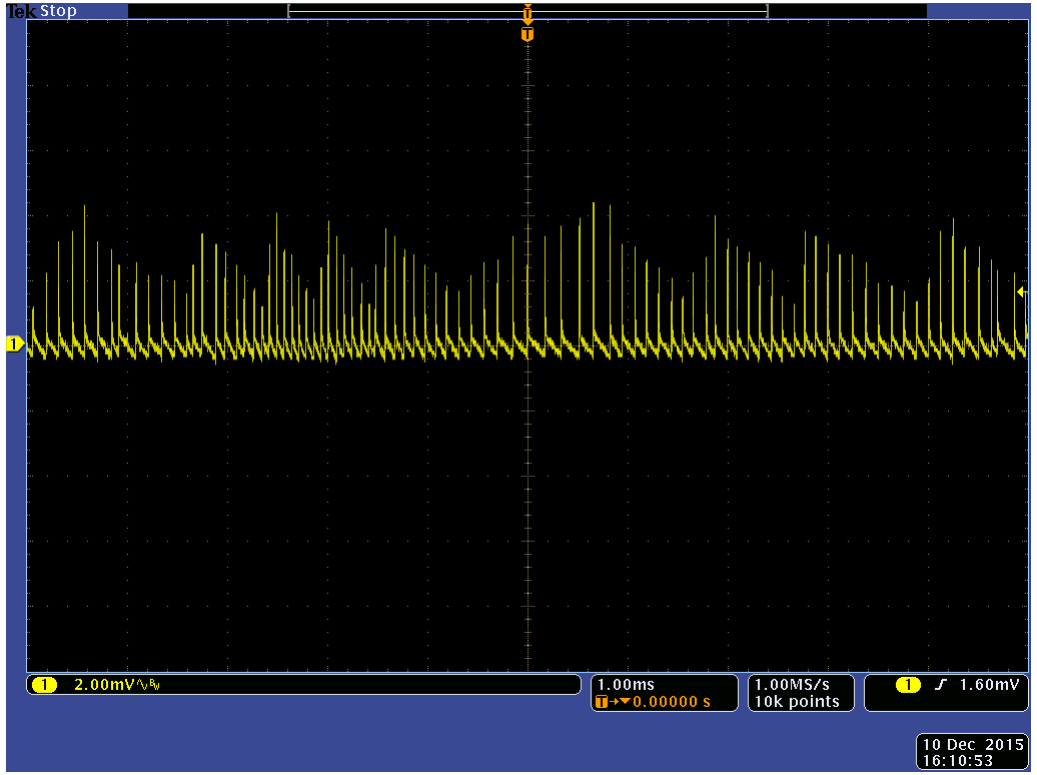
MHP8565A Performance Summary cont'd.

c,) Output Noise and Ripple Voltage

In order to observe the output noise and ripple of the MHP8565A POL, the output was observed with a wide-bandwidth oscilloscope whose bandwidth was limited to 20MHz. The waveforms that were obtained at each output current level are shown in Figure 4 through Figure 8 for the 5V input case and in Figure 10 through Figure 13 for the 12V input case.

Figure 4. *MHP8565A Output Noise and Ripple Voltage, Iout = 0A: Vin=5Vdc.*



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MHP8565A Performance Summary cont'd.

Figure 5. *MHP8565A Output Noise and Ripple Voltage, Iout = 1A: Vin=5Vdc.*

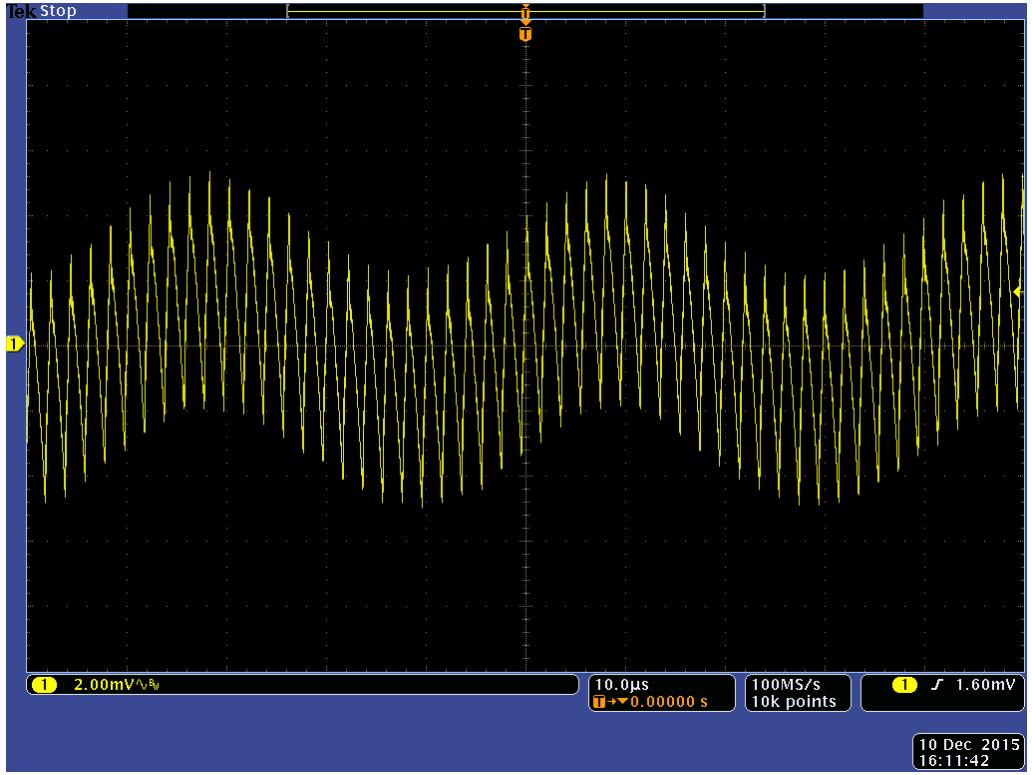
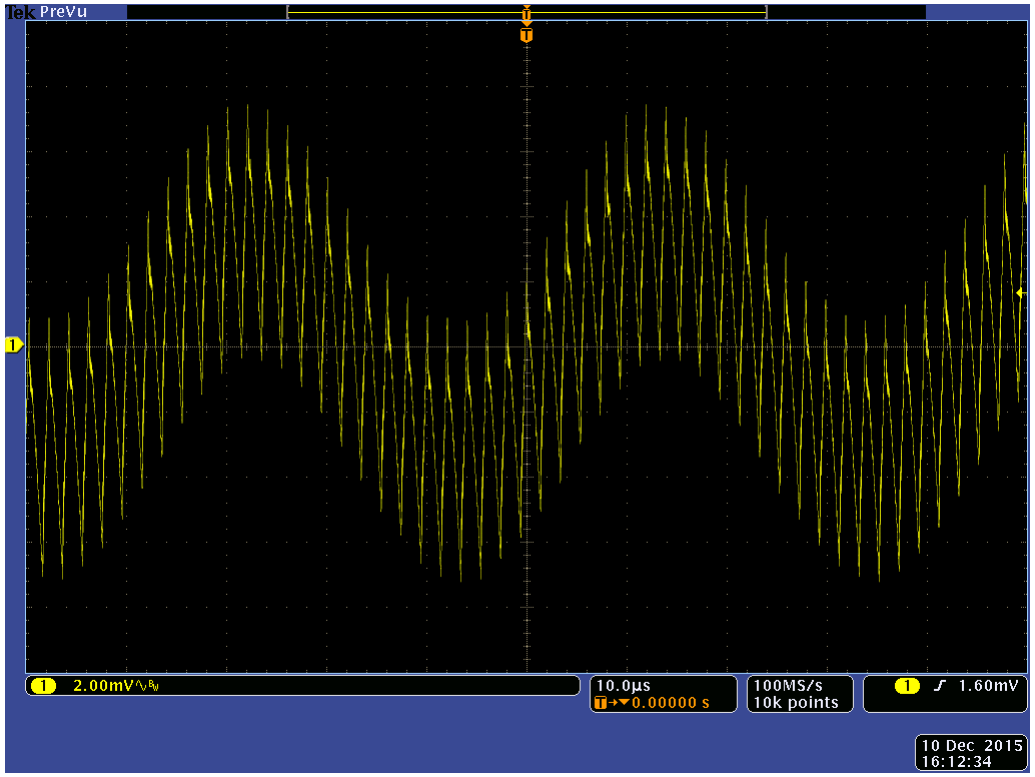


Figure 6. *MHP8565A Output Noise and Ripple Voltage, Iout = 2A: Vin=5Vdc.*



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MHP8565A Performance Summary cont'd.

Figure 7. *MHP8565A Output Noise and Ripple Voltage, Iout = 3A: Vin=5Vdc.*

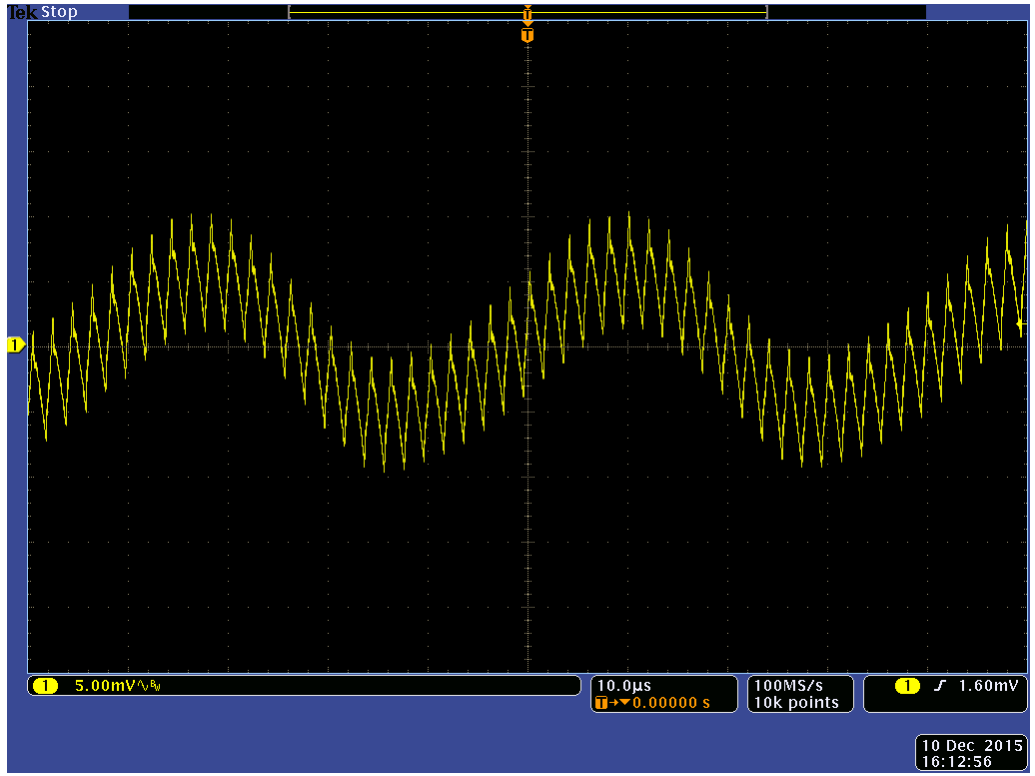
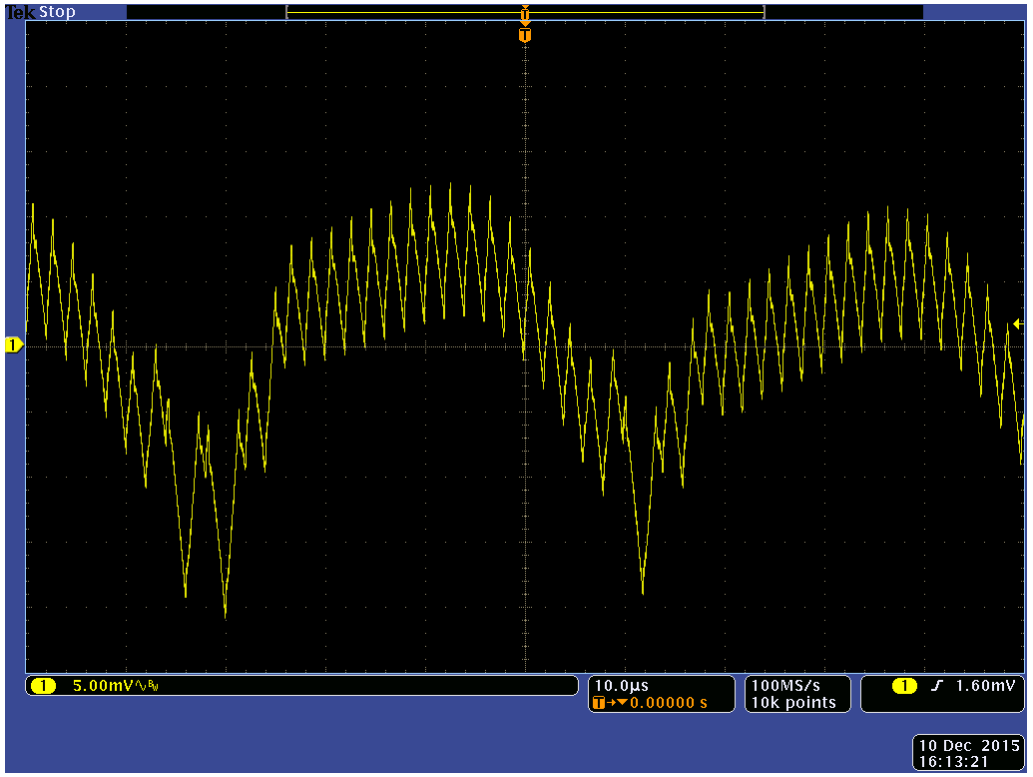


Figure 8. *MHP8565A Output Noise and Ripple Voltage, Iout = 4A: Vin=5Vdc.*



For Vin = 5V the output noise and ripple is 4mVp-p at 0A (no load); 5mV at 1A; 15mV at 2A; 20mV at 3A; and 32.5mV at 4A.

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MHP8565A Performance Summary cont'd.

Figure 9. *MHP8565A Output Noise and Ripple Voltage, Iout = 0A: Vin=12Vdc.*

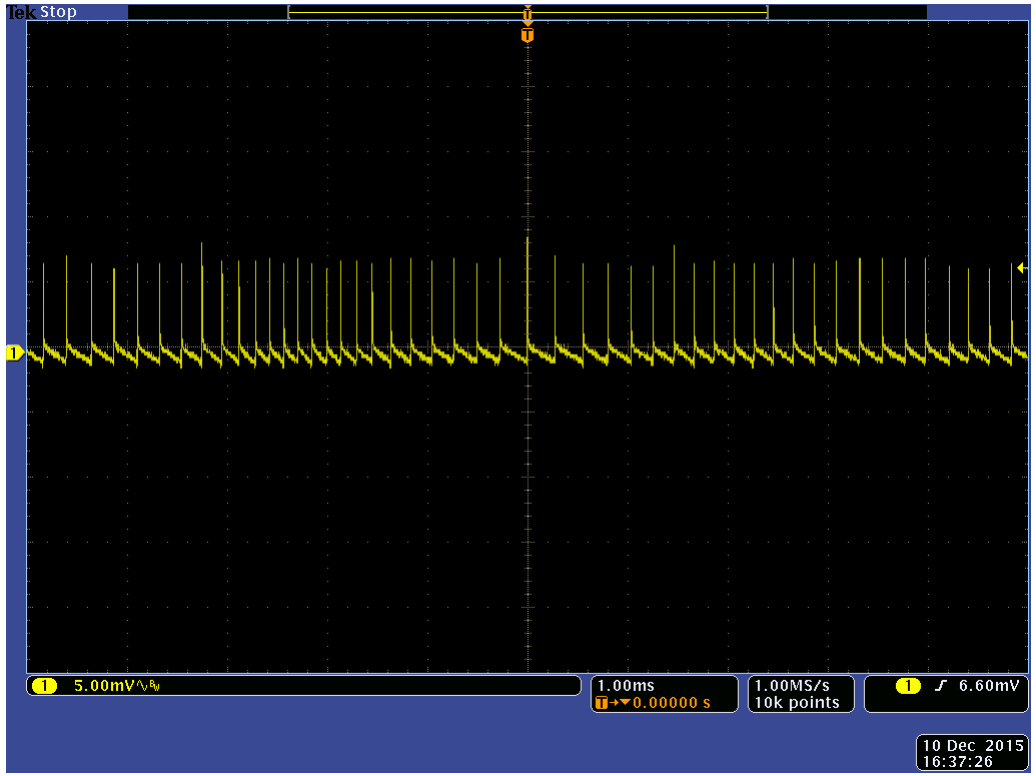
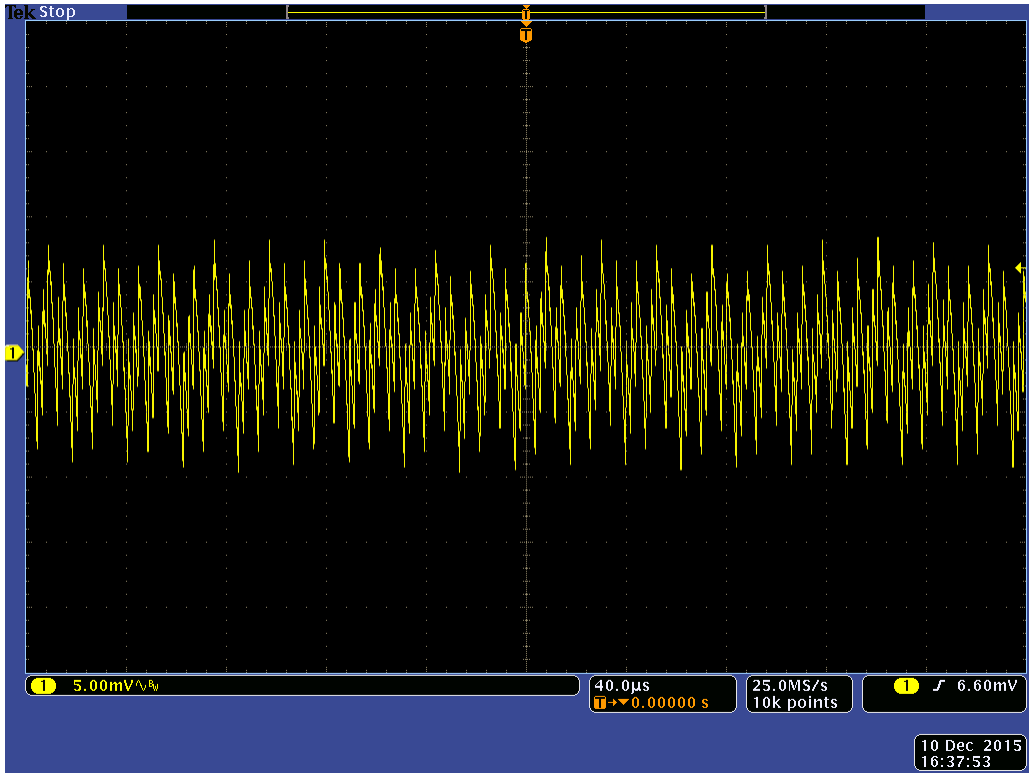


Figure 10. *MHP8565A Output Noise and Ripple Voltage, Iout = 1A: Vin=12Vdc.*



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MHP8565A Performance Summary cont'd.

Figure 11. *MHP8565A Output Noise and Ripple Voltage, Iout = 2A: Vin=12Vdc.*

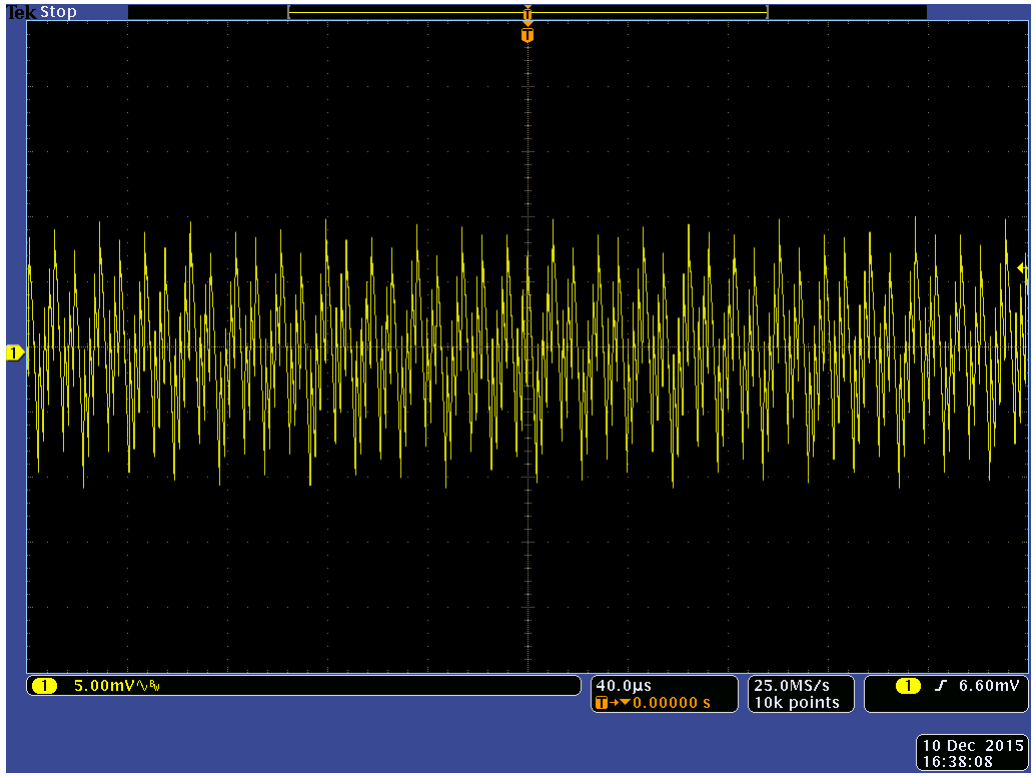
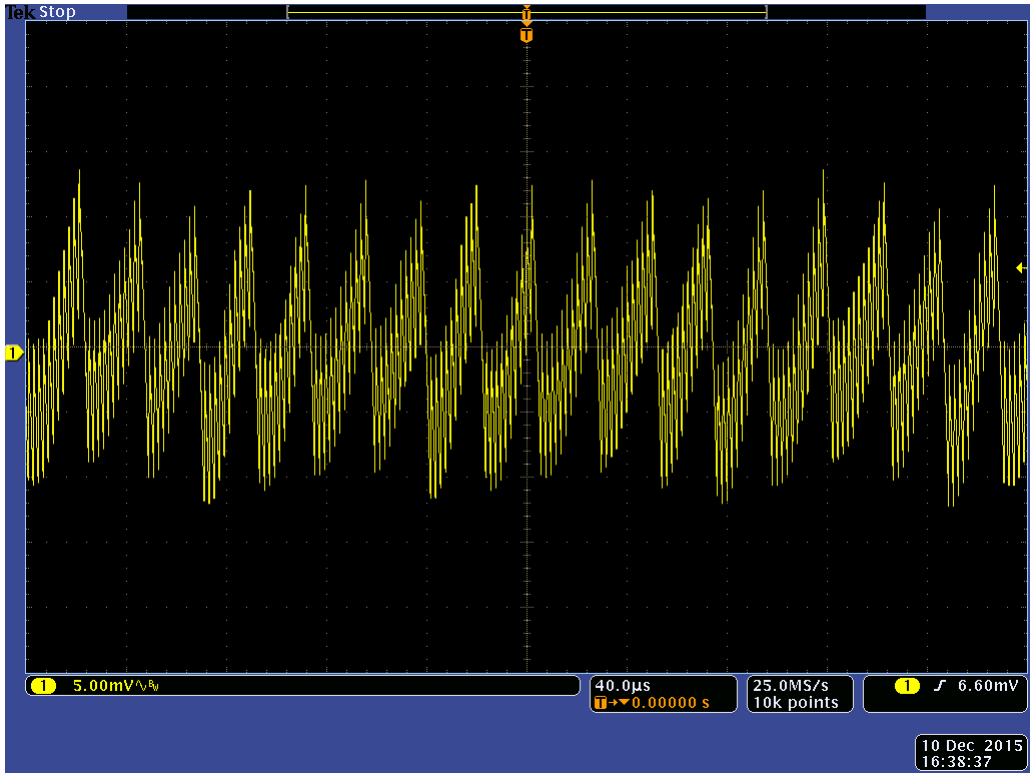


Figure 12. *MHP8565A Output Noise and Ripple Voltage, Iout = 3A: Vin=12Vdc.*



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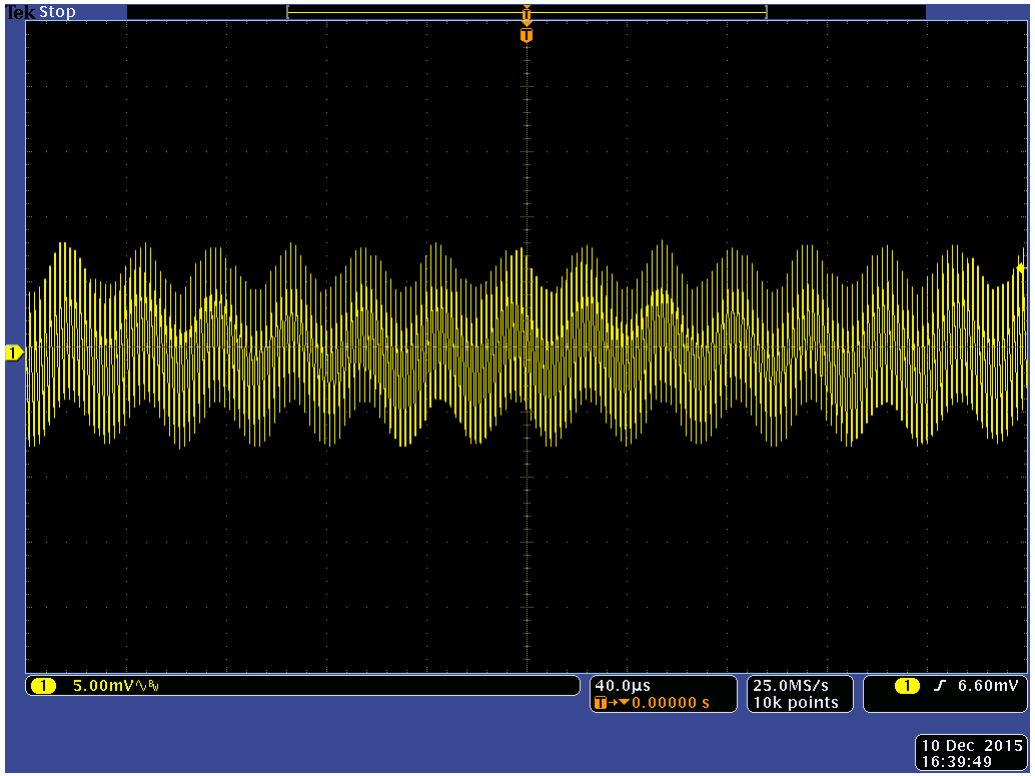
MHP8565A Performance Summary cont'd.

Figure 13. *MHP8565A Output Noise and Ripple Voltage, Iout = 4A: Vin=12Vdc.*



For Vin = 12V the output noise and ripple is 8mVp-p at 0A (no load); 13.5mV at 1A; 20mV at 2A; 24mV at 3A; and 12.5mV at 4A.

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MHP8565A Performance Summary cont'd.

d.) Output Transient Voltage

In order to observe the output transient performance behavior of the MHP8565A POl the output current was set to vary from either 1A-to-2A-to-1A or 1A-to-3A-to-1A as a pulse with 1us rise and fall times and 500us duration at each current level. The output was again monitored with an oscilloscope whose bandwidth was limited to 20MHz.

The output transient performance for Vin = 5Vdc is shown in Figure 14 (1-2A) and Figure 15 (1-3A), and for Vin = 12Vdc is shown in Figure 16 (1-2A) and Figure 17 (1-3A).

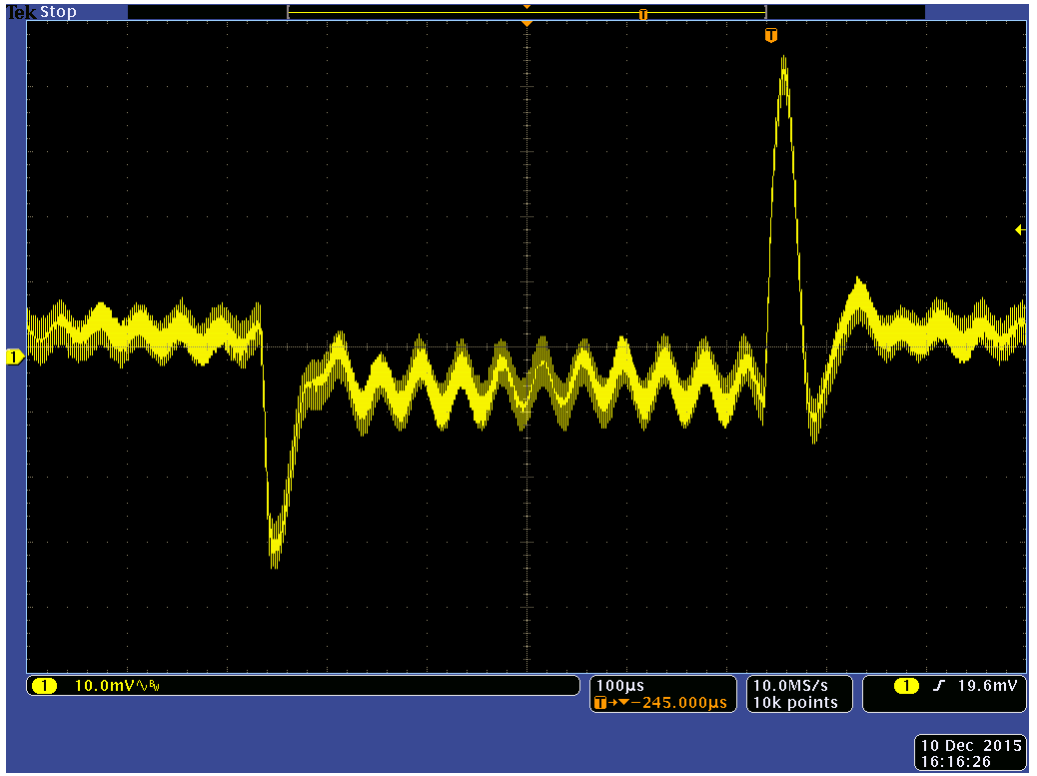

Figure 14. *MHP8565A Output Transient Voltage, Iout =1-2A: Vin=5Vdc.*

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MHP8565A Performance Summary cont'd.

Figure 15. *MHP8565A Output Transient Voltage, Iout =1-3A: Vin=5Vdc.*

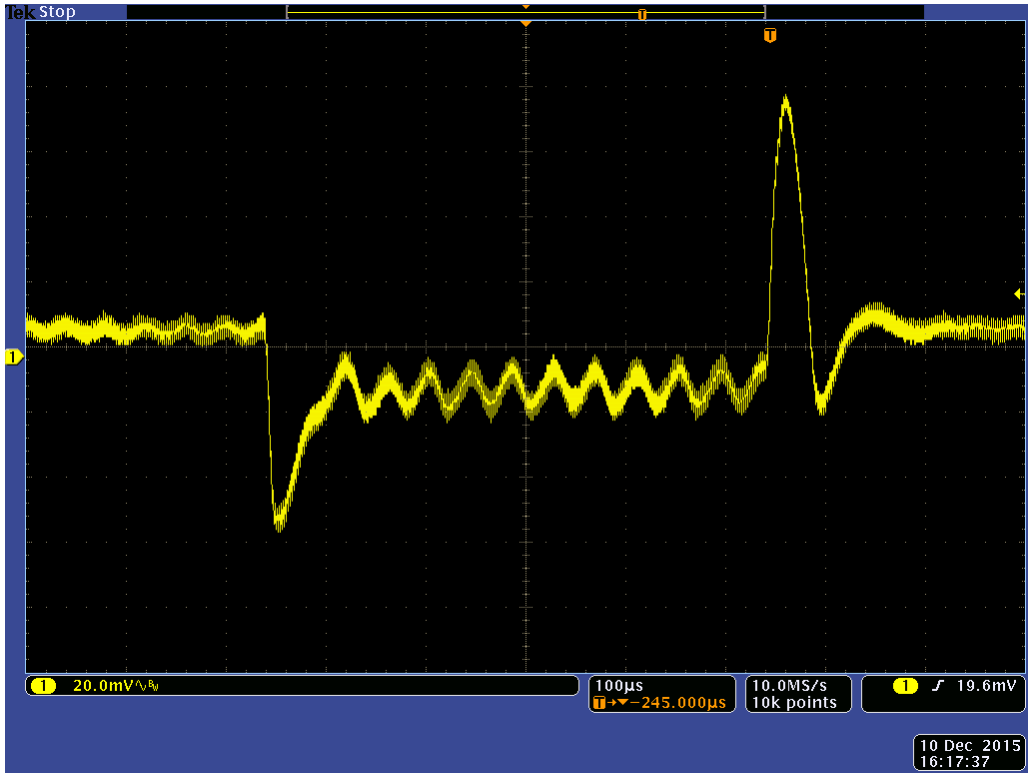
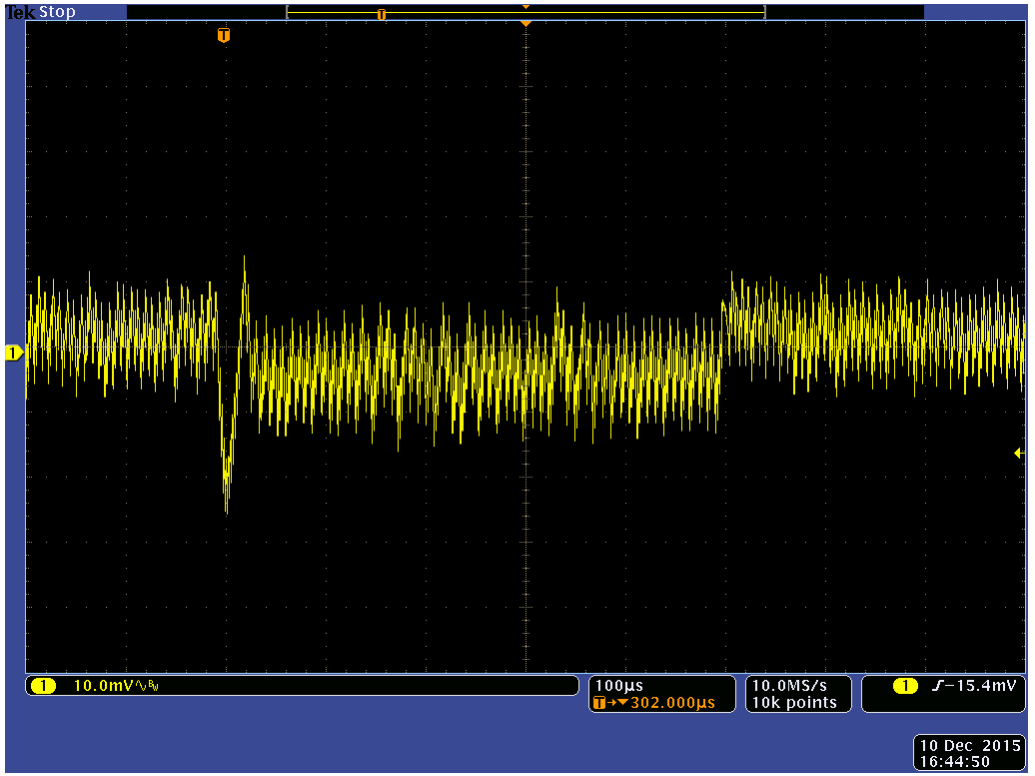


Figure 16. *MHP8565A Output Transient Voltage, Iout =1-2A: Vin=12Vdc.*



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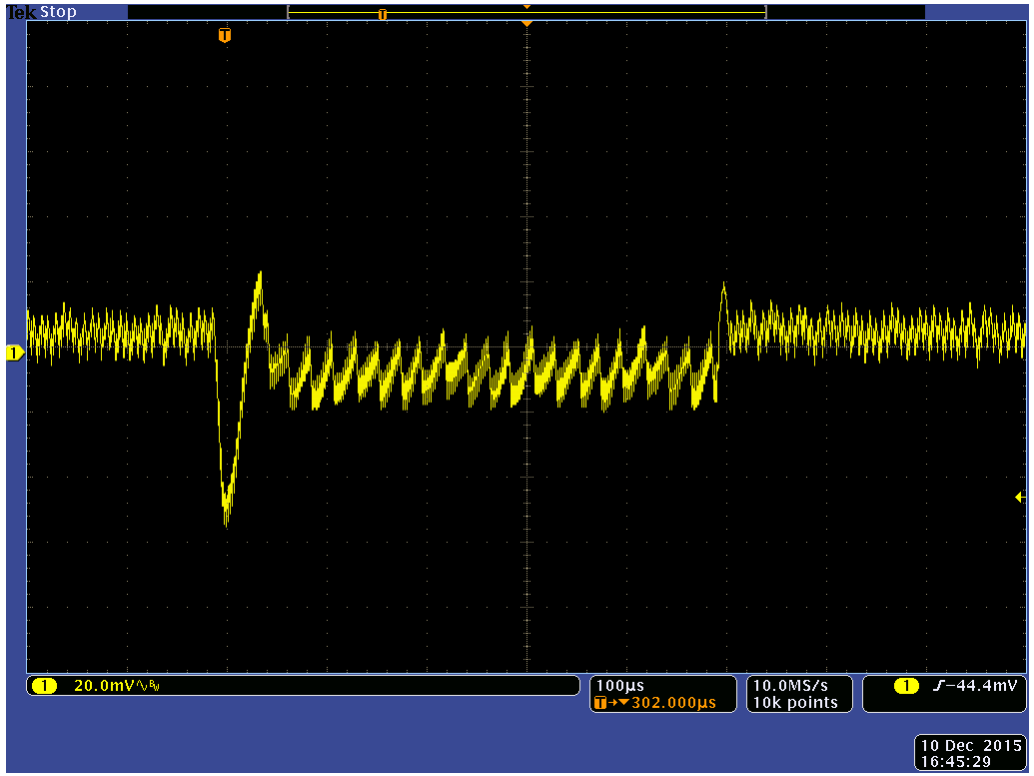
MHP8565A Performance Summary cont'd.

Figure 17. *MHP8565A Output Transient Voltage, Iout =1-3A: Vin=12Vdc.*



For Vin = 5V the output voltage transient is 78mVp-p, and the recovery time to a level less than 1% is 80us for a 1A-to-2A-to-1A current step change; and it is 112mVp-p, and the recovery time to a level less than 1% is 100us for a 1A-to-3A-to-1A current step change.

For Vin = 12V the output voltage transient is 38mVp-p, and the recovery time to a level less than 1% is 50us for a 1A-to-2A-to-1A current step change; and it is 78mVp-p, and the recovery time to a level less than 1% is 75us for a 1A-to-3A-to-1A current step change.

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MHP8565A Performance Summary cont'd.

e.) Output Turn-On Transient Voltage Event

The output voltage turn-on transient event was observed with 0A (no load) and 3.5A (full load) to determine if operation at Vin=1.00Vdc has any deleterious effects on the start-up of the MHP8565A POL.

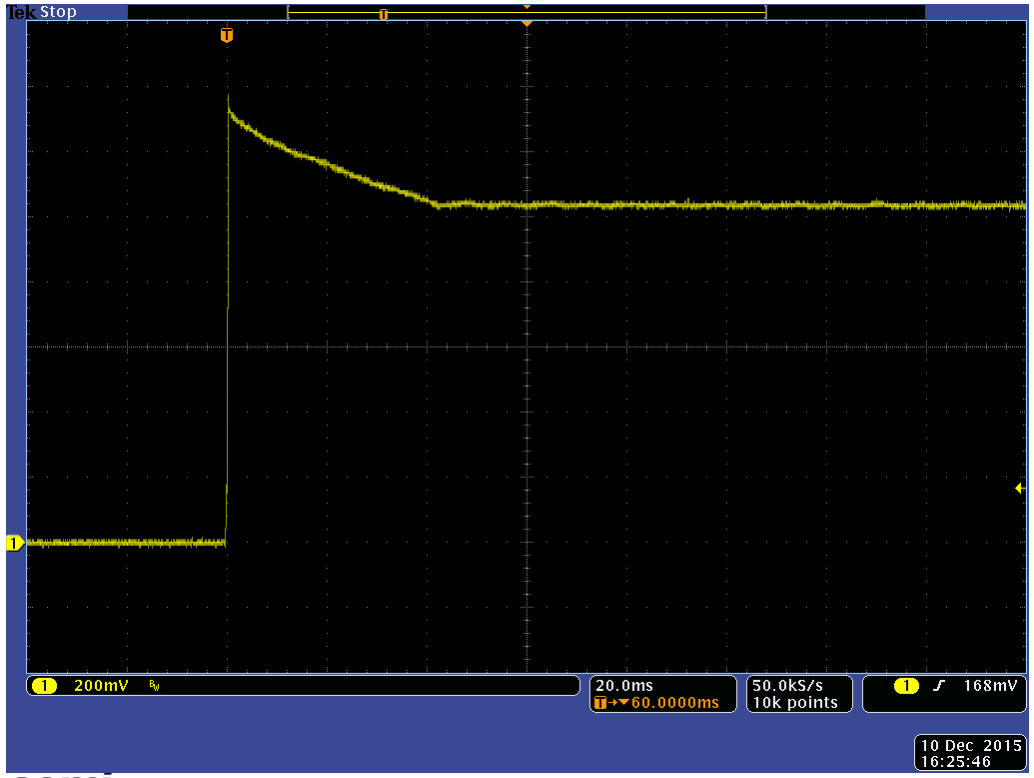

Figure 18. *MHP8565A Output Turn-On Transient Voltage, Iout =0A: Vin=5Vdc.*

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MHP8565A Performance Summary cont'd.

Figure 19. *MHP8565A Output Turn-On Transient Voltage, Iout =3.5A: Vin=5Vdc.*

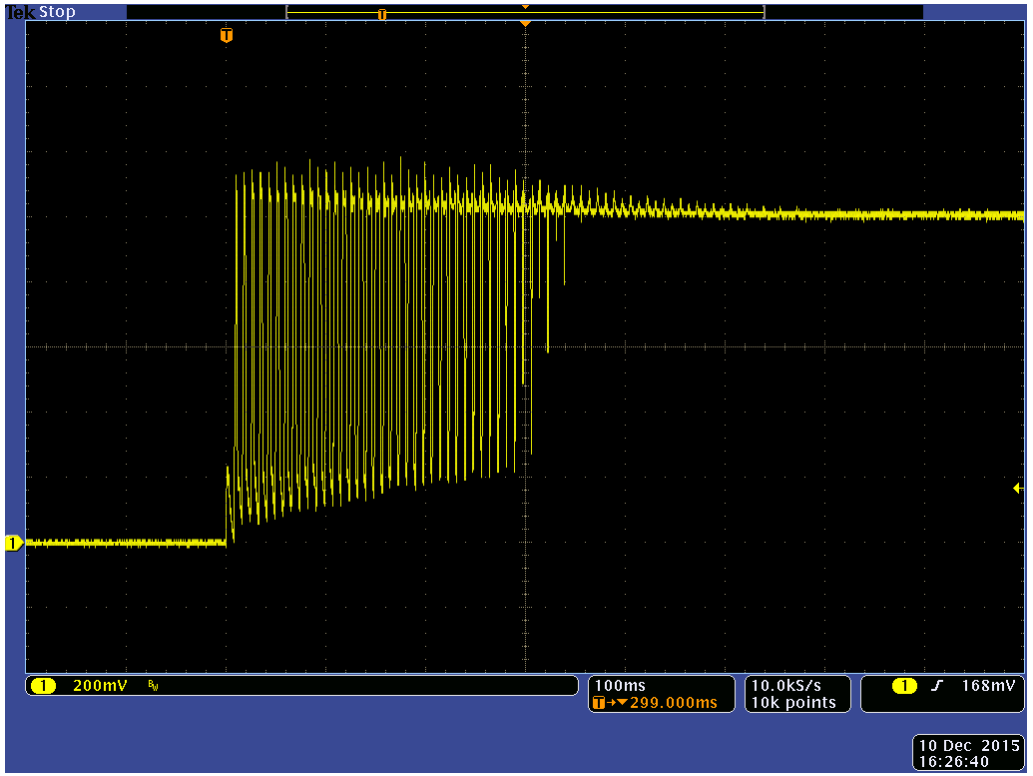
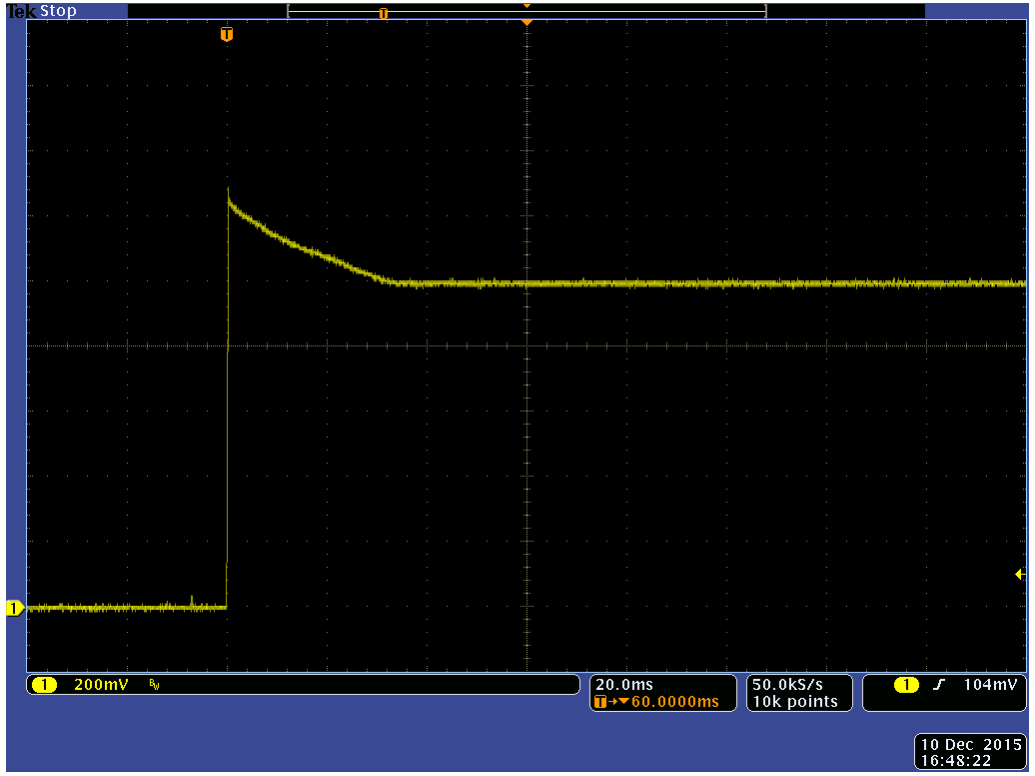


Figure 20. *MHP8565A Output Turn-On Transient Voltage, Iout =0A: Vin=12Vdc.*



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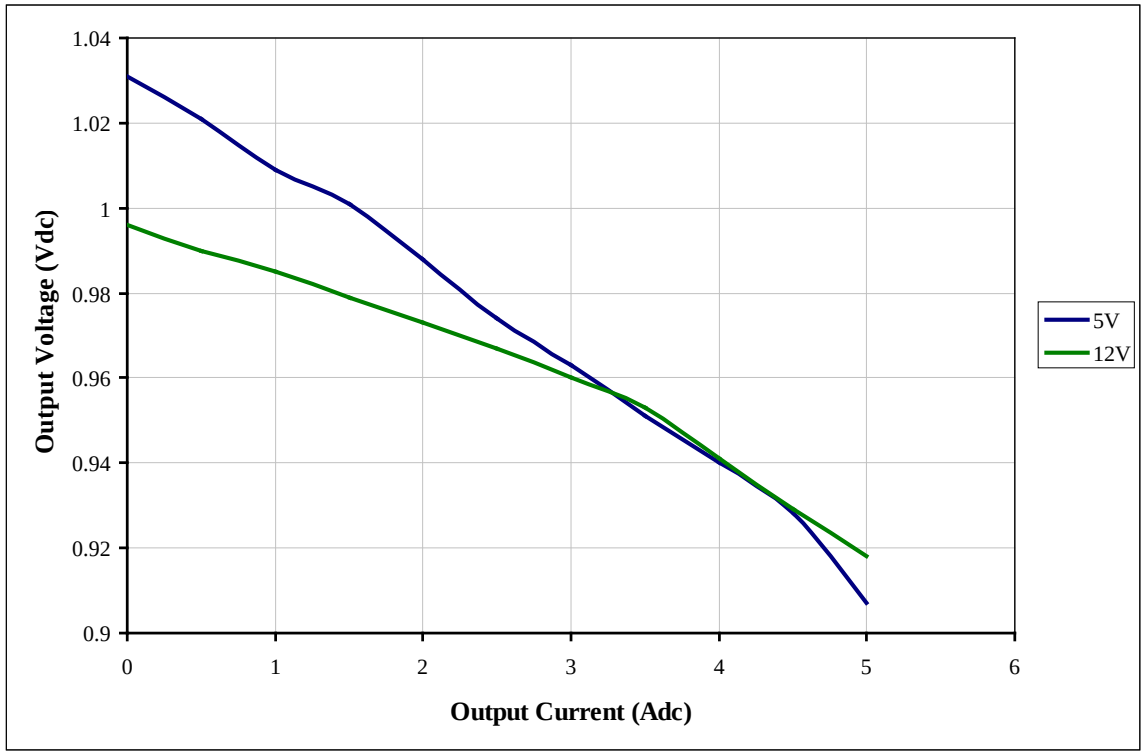
MHP8565A Performance Summary for 1.0V V_{OUT} cont'd.

Load regulation observed over the data sheet specified load current range of 1 to 2A is:
21mV, or 2.1% for 5Vdc input and
12mV, or 1.2% for 12Vdc input.

Load regulation observed over the load current range of 1 to 3.5A is:
58mV, or 5.1% for 5Vdc input and
32mV, or 3.2% for 12Vdc input.

These contrast with the data sheet specified maximum of 1% with Vout of 1.2V

Figure 3. *MHP8565A Vout versus Iout versus Input Voltage.*



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MHP8565A Performance Summary for 1.0V V_{OUT} cont'd.

b.) Line Voltage Regulation

In order to obtain the line voltage regulation performance the input to the MHP8565A POL was set to 4.5V and then 5.5Vdc for the 5V input case and from 10.5V to 13.5V for the 12V input case, with a load current of 2A, and the output voltage was recorded at each extreme.

For the 4.5V input, the output voltage was 1.036Vdc.

For the 5.5V input, the output voltage was 0.958Vdc

This is a deviation of +36/-42mV, or +3.6%/- 4.2%. This contrasts with the data sheet maximum value of +/-0.5% for 1.21V Vout.

For the 10.5V input, the output voltage was 0.974Vdc.

For the 13.5V input, the output voltage was 0.972Vdc

This is a deviation of - 28mV, or – 2.8%.

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MHP8565A Performance Summary for 1.0 V V_{OUT} cont'd.

For the V_{in}= 5 Vdc case:

I_{LOAD} of 0A, 275mV peak V_{OUT} overshoot at turn on for 39 ms until the output returns to within 1% of the regulated value.

I_{LOAD} of 3.5A, 180 mV peak V_{OUT} overshoot at turn-on 700 ms until the output returns to with 1% of the regulated value.

For the V_{in}= 12 Vdc case:

I_{LOAD} of 0 A, 240 mV peak V_{OUT} overshoot at turn-on for 32 ms until the output returns to with 1% of the regulated value.

I_{LOAD} of 3.5 A, 220 mV peak V_{OUT} overshoot at turn-on 150 ms until the output returns to within 1% of the regulated value.

In both cases of V_{in} being 5V or 12V , there is significant pulse activity during the turn-on transient event at the higher load current of 3.5 A, which is indicative of the internal PWM entering a current limit or maximum pulse width limit regime.

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MHP8565A Performance Summary for 1.0 V V_{OUT} cont'd

- The MPH8565A was tested under 5V AND 12V conditions up to and beyond the maximum specified level of 3.5 A.
- All in all, the device works well at the V_{out}= 1.00 Vdc level.
- The line and load regulation performance characteristics were observed to be slightly degraded when operated at V_{in}= 5 Vdc as compared to when the device is operated at V_{in}= 12 Vdc.
- This degradation in performance is only observed at low output currents—at 1 A and below. Above the 1 A level, both the line and load regulation track quite well between the 5 Vdc and 12 Vdc input voltage cases.
- All the remainder of the parametric performance for the device yields excellent results, and exceptional ripple and noise, and output transient performance were obtained for the MHP8565A with its output voltage set to 1.00 Vdc.
- Accordingly, there is absolutely no performance reason not to apply the MHP8565A POL hybrid regulator at output voltages of 1.00 Vdc, and the end-user can anticipate the same performance as when the device is configured to provide output voltages either equal to or greater than the internal 1.21 Vdc band gap reference potential.

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Paralleling MHP8564S—EAR99 I_{OUT} Post-100K Irradiation, 25 ℃

Features

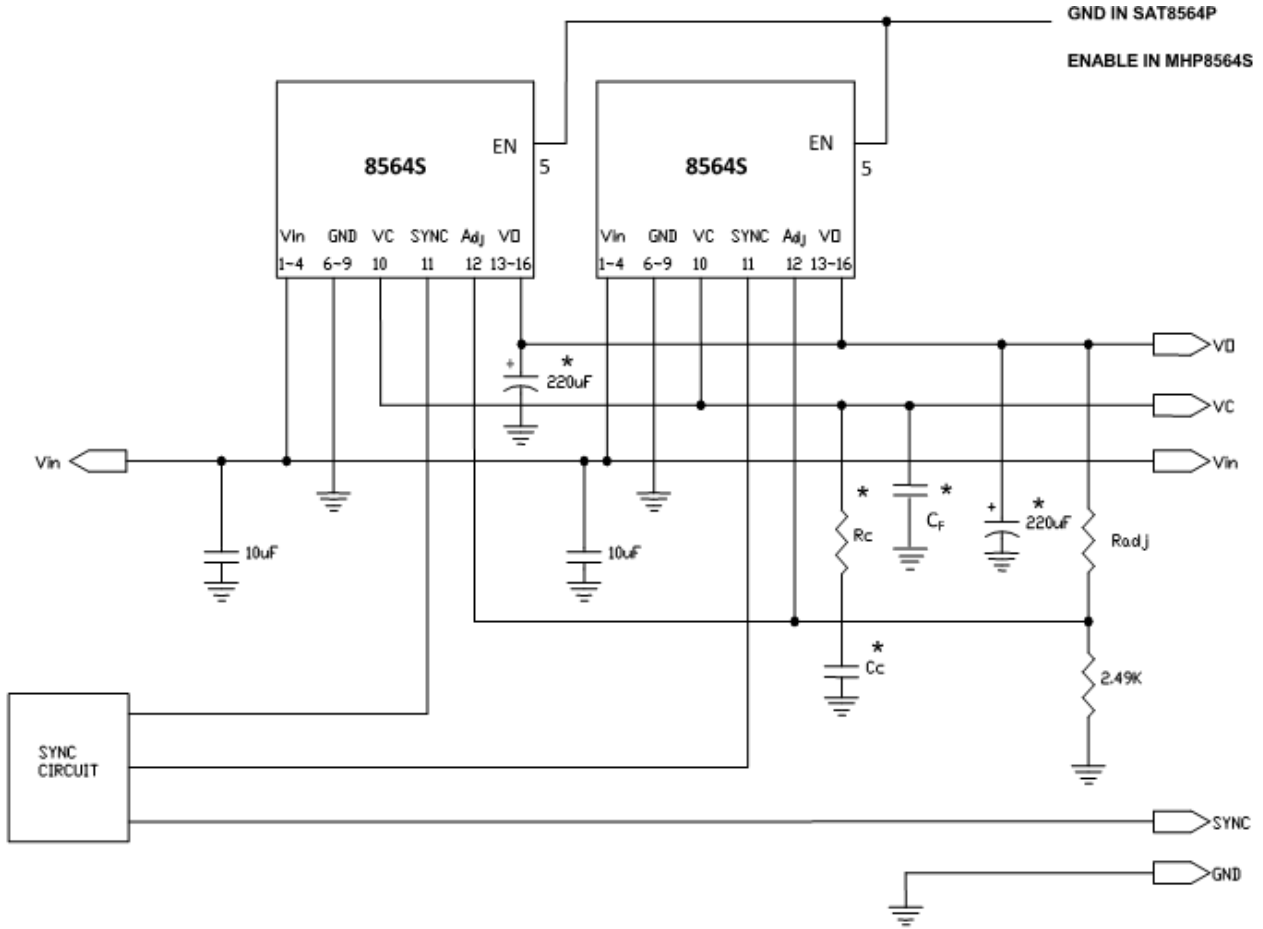
- Vc's are hooked together and connected by a common cap to ground.
- Tolerances in each device reference currents mean that small offset currents flow between devices.
- The loop regulates the output voltage somewhere between the minimum and maximum reference of the devices being used.
- Switch current matching between devices is better than 300 mA.
- There is no current hogging due to the negative temp coefficient of Vc to switch current gm (transconductance).
- Compensation techniques are described in the device datasheet and application manual.

Table 6 – Parallelable Configuration – 8564S

PIN #	DESCRIPTION
1 - 4	Vin
5	Enable
6 - 9	GND
10	Vcomp
11	Sync
12	Adjust
13 - 16	Vout

16 Pin Flat Pack (MHP8564)

Block Diagram



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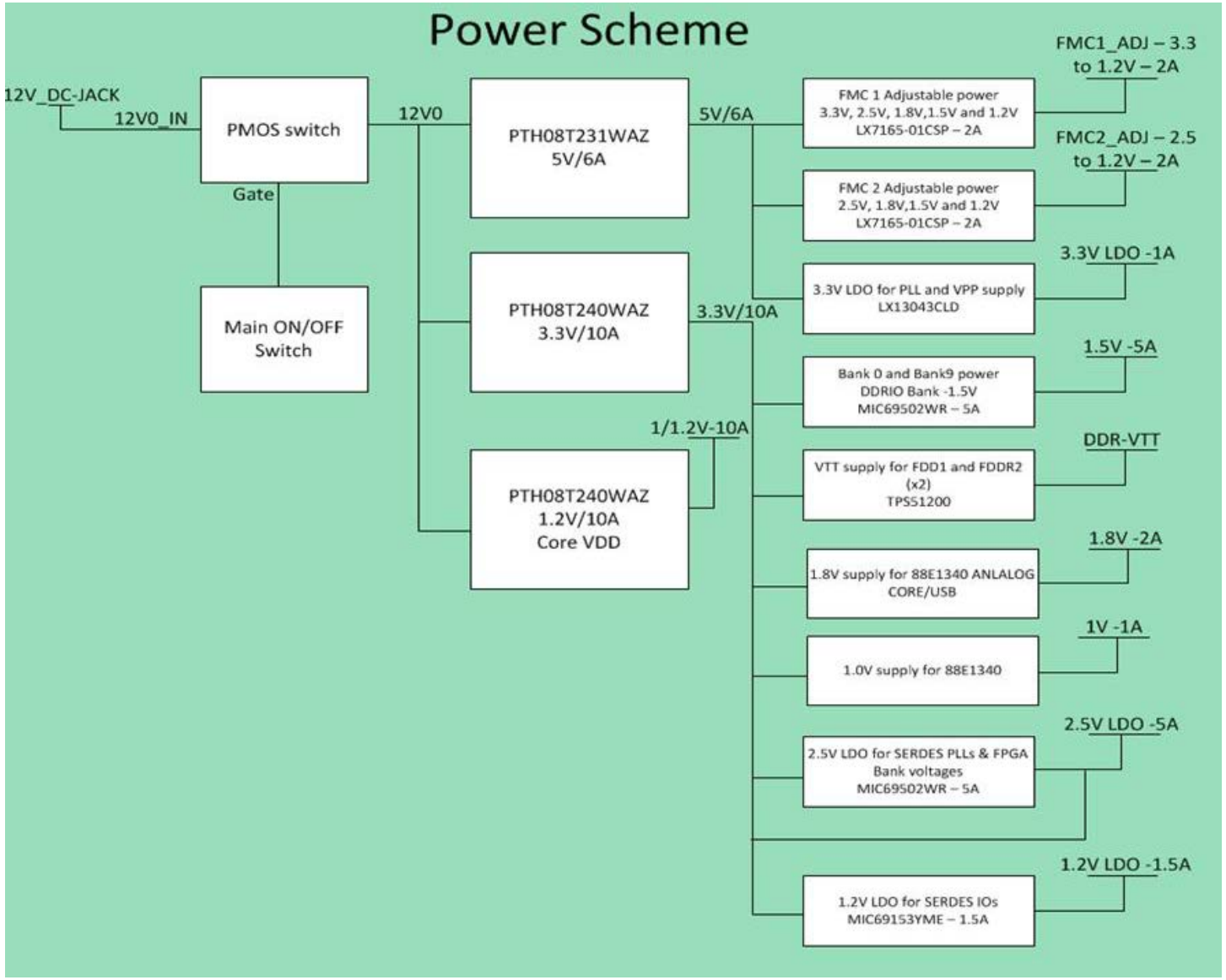
Reminder - RTG4 Evaluation Board Commercial Non-RH Device Power Scheme



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Alternate Power Distribution Schemes

- Existing RTG4 Design
  - Total Power Loss of System –
    - 50% Io 26.59W
    - 100% Io 47.53W

- Proposed RTG4 Enhanced utilizing RH components 1 x SA50, 3 x MHP8564/5
  - SA50 supplying the 5V instead of the main 5V PoL and potential to also supply 12V if needed.
  - MHP8564/5 from 5.0V to 3.3V at 1.5A to 3A sweet spot for this device's efficiency.
  - Total Power Loss of system
    - 50% Io 25.36W
    - 100% Io 48.74W
  - Note loose 1 Main 5V Rail PoL hence overall efficiency is similar BUT RH components are used.

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Summary

- 60 Years of Space Heritage.
- Widest discrete product portfolio of any space component manufacturer.
- Largest Screening facilities of any supplier WW with 10’s Million $ investment.
- Flexible isolated DC-DC and PoL.
- Over 95% of components are EAR99.
- Standard, Semi-custom and custom solutions.
- Future Power solutions:
  - New - SB30 Isolated Point of Load
  - MHP5061 3.0 - 6.3 V_{in}, 6 A, Synchronous Hybrid Point of Load DC-DC Converter
- Committed to providing cost effective total systems solutions, e.g. Space Reference Platform.
- Support when you need it.
- Aiming to be Your Preferred Partner

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Thank You

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