

Video DC MIPI
Rev A

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Project Name:		
Video DC MIPI		
Rev	Part Number:	
A	MICROSEMI DVP-100-000485-001	PACTRON:305-PD-16-0880
Originator:		
GHURU KUMARAVELU		
Size	Date:	
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The schematic diagram illustrates the Video DC MIPI interface circuit, showing connections between the LCD Module and the Video DC MIPI module. The circuit is divided into four main functional blocks:

- SIGNAL CONNECTOR:** This block shows the connection between the LCD Module (J1) and the Video DC MIPI module. It includes a 3P3V power supply connected to the LCD Module via a 4.7uF capacitor (C141) and a 0.1uF capacitor (C140). The LCD Module is connected to the Video DC MIPI module via a 1-102618-0 connector. The Video DC MIPI module is connected to the LCD Module via a 1-102618-0 connector. The Video DC MIPI module is connected to the LCD Module via a 1-102618-0 connector.
- CLOCK SYNTHESIZER:** This block shows the connection between the PLL_1V8 power supply and the Video DC MIPI module. It includes a 4.7K resistor (R29) connected to the PLL_1V8 power supply. The Video DC MIPI module is connected to the PLL_1V8 power supply via a 4.7K resistor (R29). The Video DC MIPI module is connected to the PLL_1V8 power supply via a 4.7K resistor (R29).
- POWER CONNECTOR:** This block shows the connection between the 12P0V power supply and the Video DC MIPI module. It includes a 0.1uF capacitor (C142) and a 4.7uF capacitor (C143) connected to the 12P0V power supply. The Video DC MIPI module is connected to the 12P0V power supply via a 0.1uF capacitor (C142) and a 4.7uF capacitor (C143).
- LEVEL TRANSLATOR:** This block shows the connection between the VADJ power supply and the Video DC MIPI module. It includes a 0.1uF capacitor (C817) and a 0.1uF capacitor (C818) connected to the VADJ power supply. The Video DC MIPI module is connected to the VADJ power supply via a 0.1uF capacitor (C817) and a 0.1uF capacitor (C818).

The Video DC MIPI module is connected to the LCD Module via a 1-102618-0 connector. The Video DC MIPI module is connected to the LCD Module via a 1-102618-0 connector. The Video DC MIPI module is connected to the LCD Module via a 1-102618-0 connector.

TO FMC

Microsemi

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The schematic diagram illustrates the Video DC MIPI interface circuit, divided into four main functional blocks:

- SIGNAL CONNECTOR:** This block shows the connection between the LCD Module and the FMC. It features a 24-pin connector (J1) with signals for FMC_RxIN0P_LA09_P, FMC_RxIN0N_LA09_N, FMC_RxIN1P_LA02_P, FMC_RxIN1N_LA02_N, FMC_RxIN2P_LA03_P, FMC_RxIN2N_LA03_N, FMC_RxIN3P_LA04_P, FMC_RxIN3N_LA04_N, and LT_RL_UD. The signals are connected to the LCD Module pins 1 through 24.
- CLOCK SYNTHESIZER:** This block shows the connection between the PLL_1V8 and the CDCE913PWR clock synthesizer. The PLL_1V8 is connected to the VDD pin of the CDCE913PWR. The CDCE913PWR is connected to the VDDOUT_1 and VDDOUT_2 pins. The XIN/CLK pin is connected to the XIN pin of the CDCE913PWR. The XOUT pin is connected to the XOUT pin of the CDCE913PWR. The VCTRL pin is connected to the VCTRL pin of the CDCE913PWR. The GND_1 and GND_2 pins are connected to the GND pin of the CDCE913PWR.
- POWER CONNECTOR:** This block shows the connection between the 12P0V power source and the LT_VBR and LT_XSTABY signals. The 12P0V is connected to the LT_VBR and LT_XSTABY pins. The LT_VBR and LT_XSTABY pins are connected to the LT_VBR and LT_XSTABY pins of the LT_VBR and LT_XSTABY signals.
- LEVEL TRANSLATOR:** This block shows the connection between the VADJ and the TXS0104EPWR level translator. The VADJ is connected to the VCCA and VCCB pins of the TXS0104EPWR. The TXS0104EPWR is connected to the LT_RL_UD, LT_SELLVDS, LT_XSTABY, and LT_VBR signals. The TXS0104EPWR is also connected to the VADJ and the 3P3V power source.

The diagram includes a title block with the following information:

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The Microsemi logo is also present in the bottom right corner of the diagram.

The schematic diagram illustrates the Video DC MIPI interface circuit, organized into four main functional blocks:

- SIGNAL CONNECTOR:** This block shows the connection between the LCD Module (J1) and the system. It includes 3P3V power inputs with decoupling capacitors C141 (4.7uF) and C140 (0.1uF). The connector pins are connected to various signals, including FMC_RxIN0P_LA09_P, FMC_RxIN0N_LA09_N, FMC_RxIN1P_LA02_P, FMC_RxIN1N_LA02_N, FMC_RxIN2P_LA03_P, FMC_RxIN2N_LA03_N, FMC_RxIN3P_LA04_P, FMC_RxIN3N_LA04_N, and LT_RL_UD. The connector is labeled 1-102618-0.
- CLOCK SYNTHESIZER:** This block features a CDCE913PWR clock synthesizer (U3). It is powered by PLL_1V8 and VDDOUT_1/VDDOUT_2. The synthesizer's input is connected to a 27.000MHz crystal (Y2) via a 4.7K resistor (R29). The output (XOUT) is connected to the FMC_V_CLK0_M2C_P and FMC_HDMI_RX_CLK0_M2C_N signals. The synthesizer also has control pins for S0, S1/SDA, S2/SCL, and VCTRL.
- POWER CONNECTOR:** This block shows the connection between the LCD Module (J2) and the system. It includes 12P0V power inputs with decoupling capacitors C142 (0.1uF) and C143 (4.7uF). The connector pins are connected to LT_VBR and LT_XSTABY signals. The connector is labeled 0901301206.
- LEVEL TRANSLATOR:** This block features a TXS0104EPWR level translator (U56). It is powered by VCCB and VCCA. The translator's input is connected to the FMC_RL_UD_LA16_P, FMC_SELLVDS_LA16_N, FMC_XSTABY_LA08_P, and FMC_VBR_LA08_N signals. The output is connected to the LT_RL_UD, LT_SELLVDS, LT_XSTABY, and LT_VBR signals. The translator also has control pins for NC_1, NC_2, OE, and GND.

The diagram also includes a detailed view of the power and ground connections for the PLL_1V8 and VDDOUT_1/VDDOUT_2 rails, showing decoupling capacitors (C42, C43, C44, C45, C46, C47, C48, C49) and ferrite beads (FB10, FB11).

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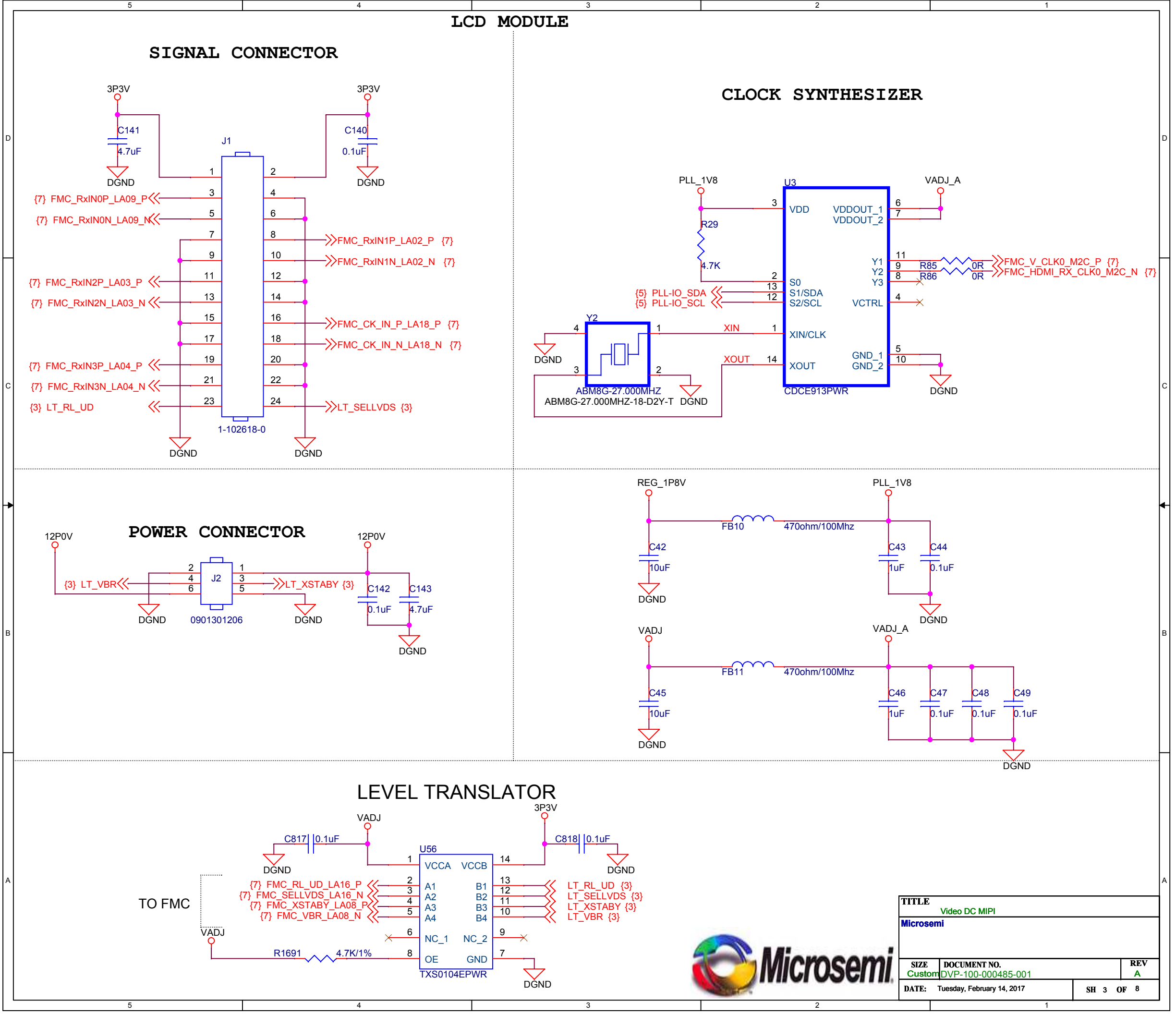
The schematic diagram illustrates the Video DC MIPI interface circuit, divided into four main functional blocks:

- SIGNAL CONNECTOR:** This block shows the connection between the LCD Module and the FMC. It features a 24-pin connector (J1) with signals for FMC_RxIN0P_LA09_P, FMC_RxIN0N_LA09_N, FMC_RxIN1P_LA02_P, FMC_RxIN1N_LA02_N, FMC_RxIN2P_LA03_P, FMC_RxIN2N_LA03_N, FMC_RxIN3P_LA04_P, FMC_RxIN3N_LA04_N, and LT_RL_UD. The signals are connected to the LCD Module pins 1 through 24.
- CLOCK SYNTHESIZER:** This block shows the connection between the PLL_1V8 and the CDCE913PWR clock synthesizer. The PLL_1V8 is connected to the VDD pin of the CDCE913PWR. The CDCE913PWR is connected to the VDDOUT_1 and VDDOUT_2 pins. The XIN/CLK pin is connected to the XIN pin of the CDCE913PWR. The XOUT pin is connected to the XOUT pin of the CDCE913PWR. The VCTRL pin is connected to the VCTRL pin of the CDCE913PWR. The GND_1 and GND_2 pins are connected to the GND pin of the CDCE913PWR.
- POWER CONNECTOR:** This block shows the connection between the 12P0V power source and the LT_VBR and LT_XSTABY signals. The 12P0V is connected to the LT_VBR and LT_XSTABY pins. The LT_VBR and LT_XSTABY pins are connected to the LT_VBR and LT_XSTABY pins of the LT_VBR and LT_XSTABY signals.
- LEVEL TRANSLATOR:** This block shows the connection between the VADJ and the TXS0104EPWR level translator. The VADJ is connected to the VCCA and VCCB pins of the TXS0104EPWR. The TXS0104EPWR is connected to the LT_RL_UD, LT_SELLVDS, LT_XSTABY, and LT_VBR signals. The TXS0104EPWR is also connected to the VADJ and the 3P3V power source.

The diagram includes a title block with the following information:

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The Microsemi logo is also present in the bottom right corner of the diagram.

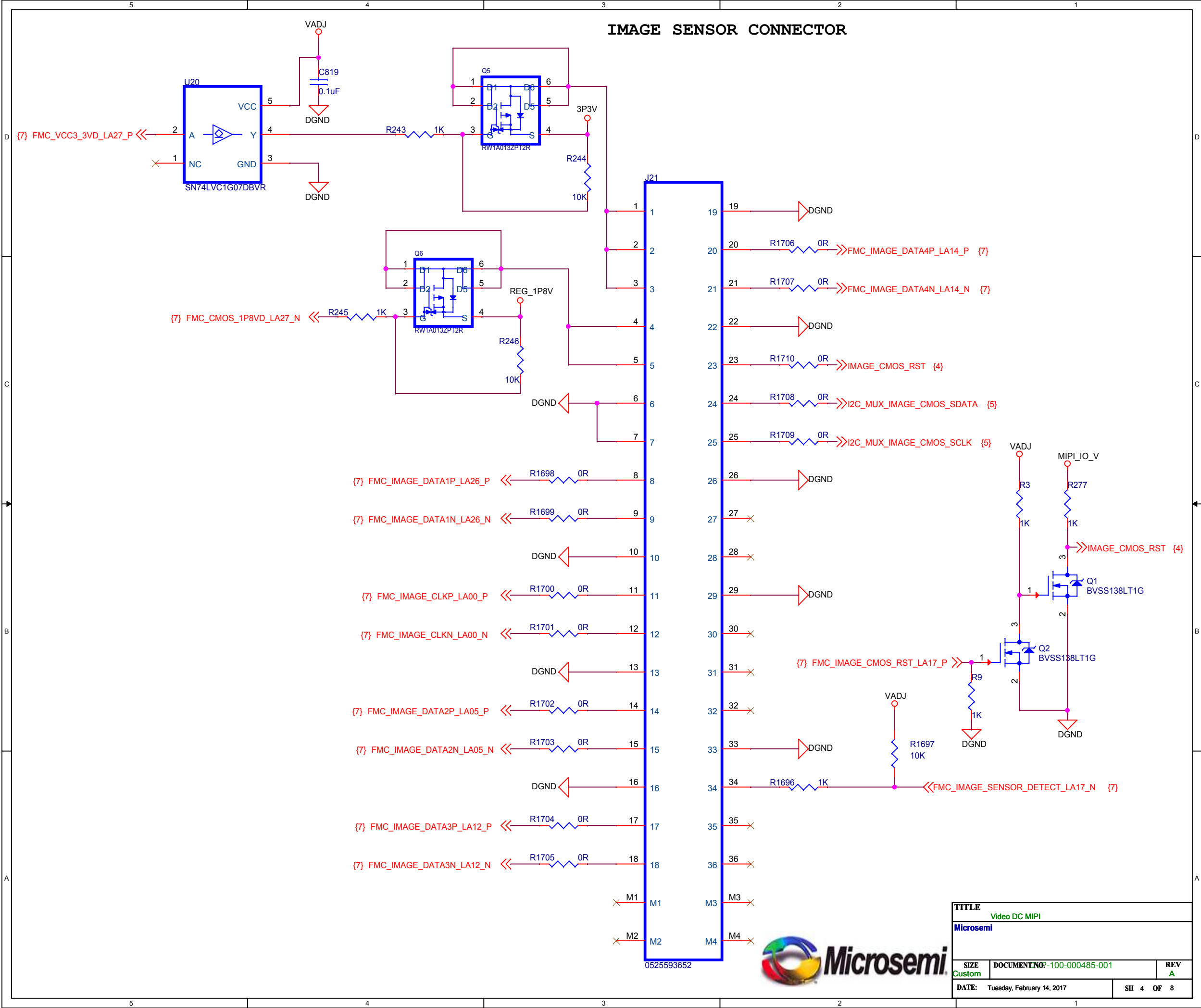


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- SIGNAL CONNECTOR:** This block shows the connection between the LCD Module and the FMC. It features a 24-pin connector (J1) with signals for FMC_RxIN0P_LA09_P, FMC_RxIN0N_LA09_N, FMC_RxIN1P_LA02_P, FMC_RxIN1N_LA02_N, FMC_RxIN2P_LA03_P, FMC_RxIN2N_LA03_N, FMC_RxIN3P_LA04_P, FMC_RxIN3N_LA04_N, and LT_RL_UD. The signals are connected to the LCD Module pins 1 through 24.
- CLOCK SYNTHESIZER:** This block shows the connection between the PLL_1V8 and the CDCE913PWR clock synthesizer. The PLL_1V8 is connected to the VDD pin of the CDCE913PWR. The CDCE913PWR is connected to the VDDOUT_1 and VDDOUT_2 pins. The XIN/CLK pin is connected to the XIN pin of the CDCE913PWR. The XOUT pin is connected to the XOUT pin of the CDCE913PWR. The VCTRL pin is connected to the VCTRL pin of the CDCE913PWR. The GND_1 and GND_2 pins are connected to the GND pin of the CDCE913PWR.
- POWER CONNECTOR:** This block shows the connection between the 12P0V power source and the LT_VBR and LT_XSTABY signals. The 12P0V is connected to the LT_VBR and LT_XSTABY pins. The LT_VBR and LT_XSTABY pins are connected to the LT_VBR and LT_XSTABY pins of the LT_VBR and LT_XSTABY signals.
- LEVEL TRANSLATOR:** This block shows the connection between the VDD and the TXS0104EPWR level translator. The VDD is connected to the VCCA and VCCB pins of the TXS0104EPWR. The TXS0104EPWR is connected to the VCCA and VCCB pins. The TXS0104EPWR is connected to the VCCA and VCCB pins. The TXS0104EPWR is connected to the VCCA and VCCB pins.

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I2C EXPANSION

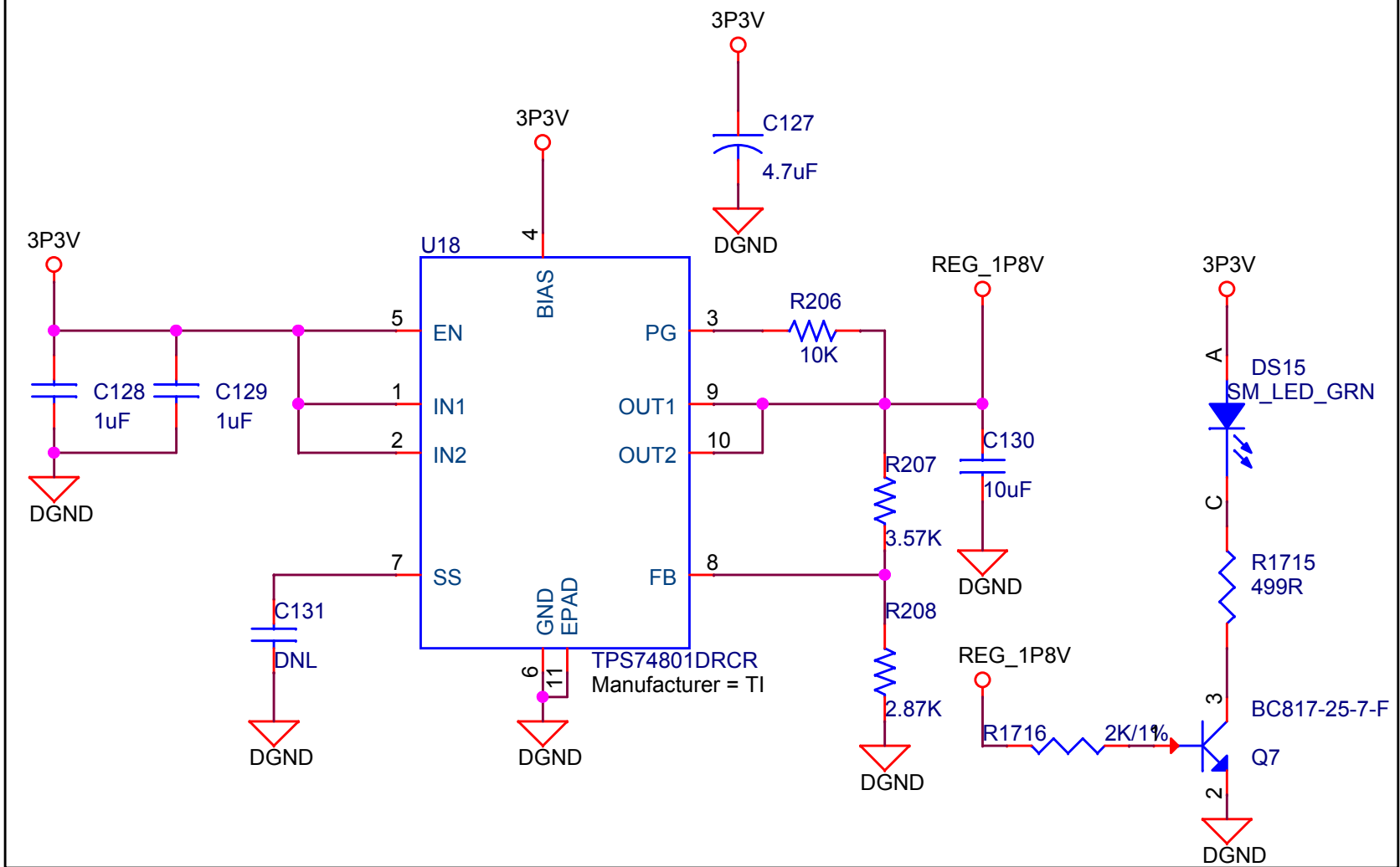


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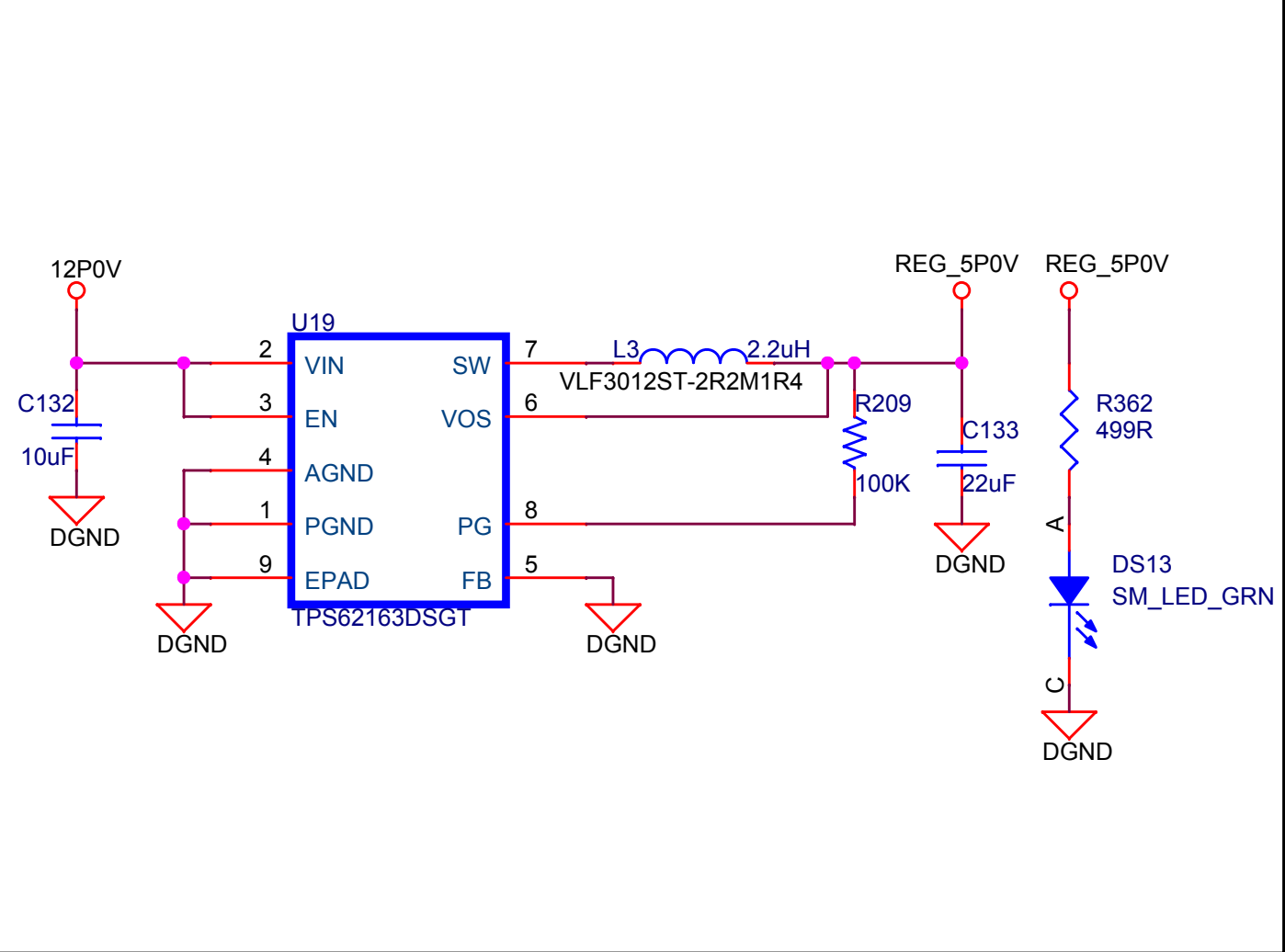


POWER REGULATORS

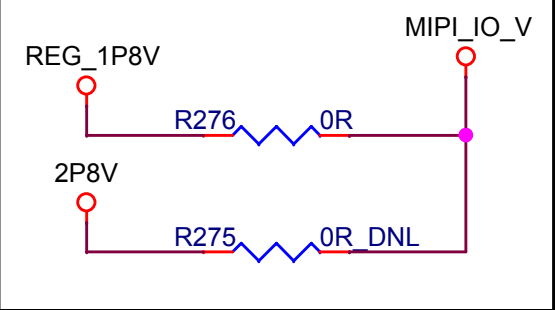
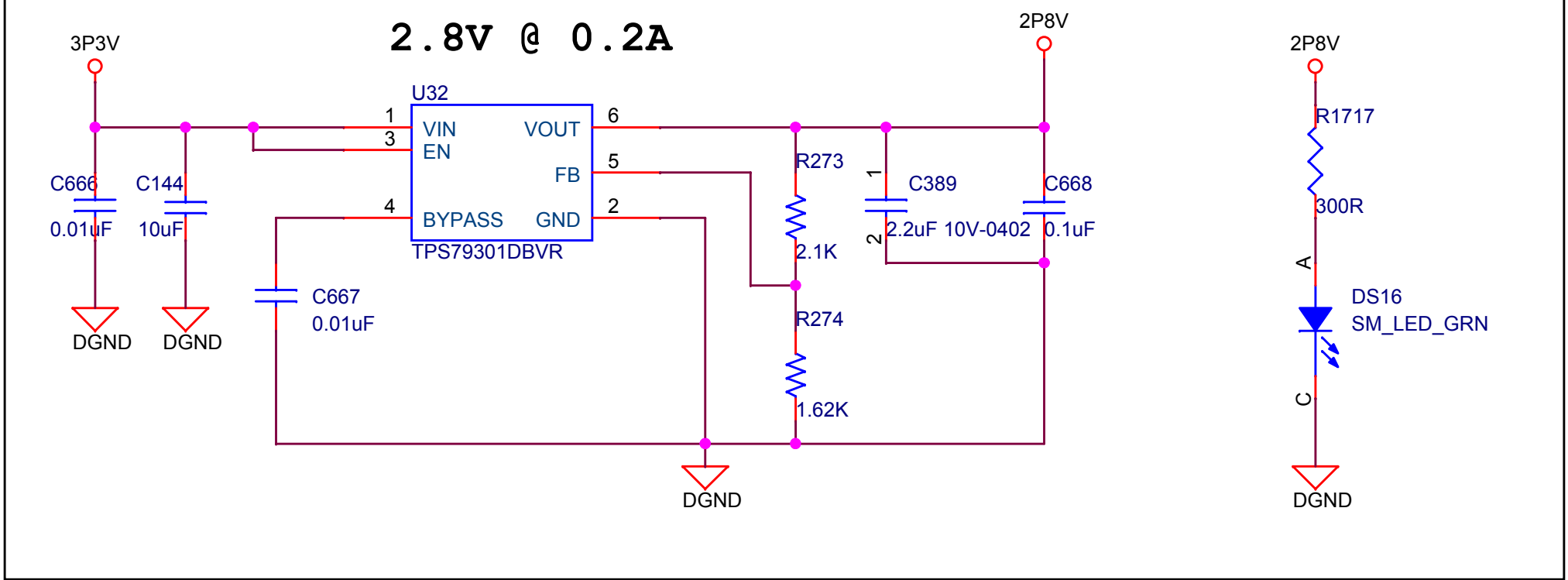
1.8V @ 1.5A



5.0V @ 1.0A

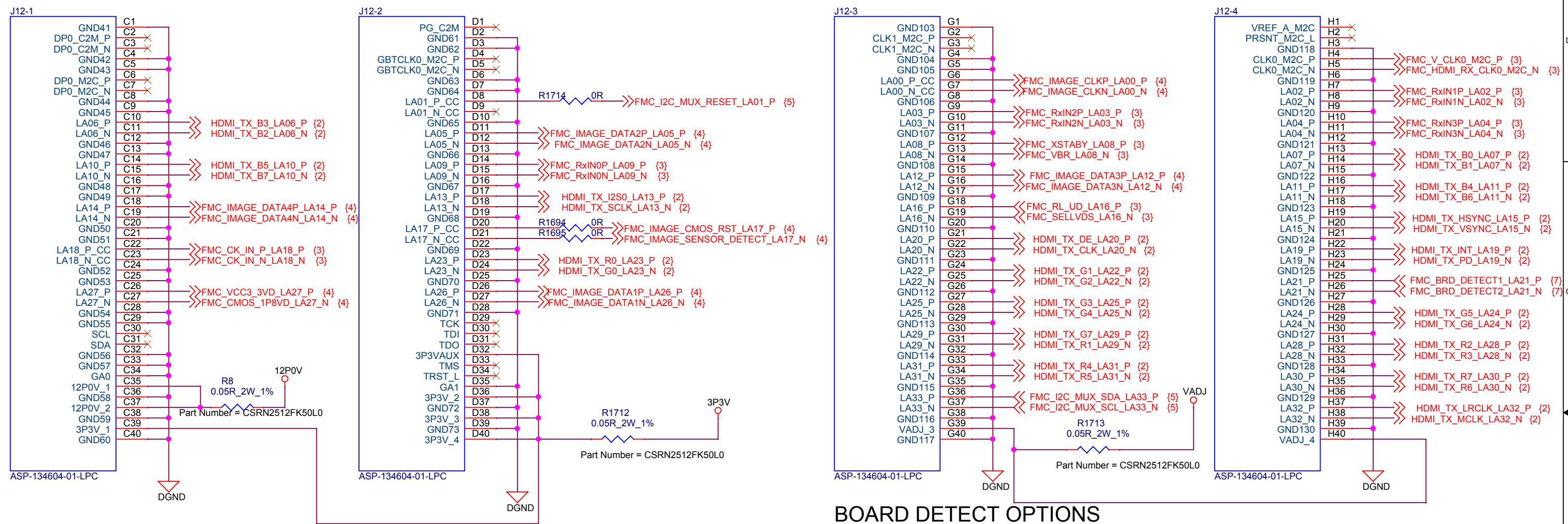


2.8V @ 0.2A

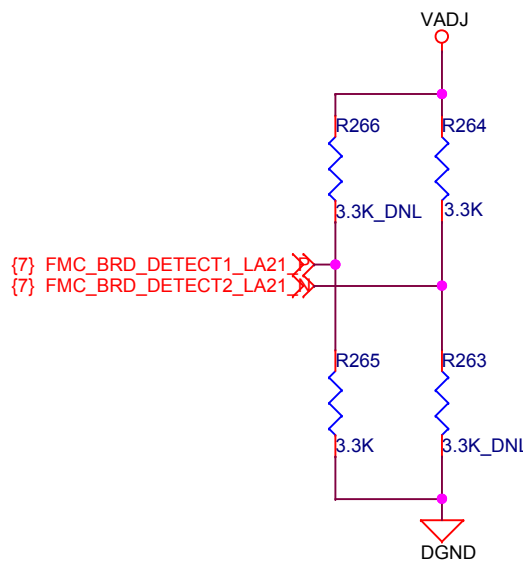
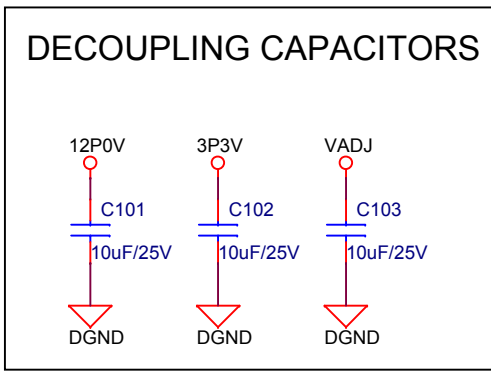
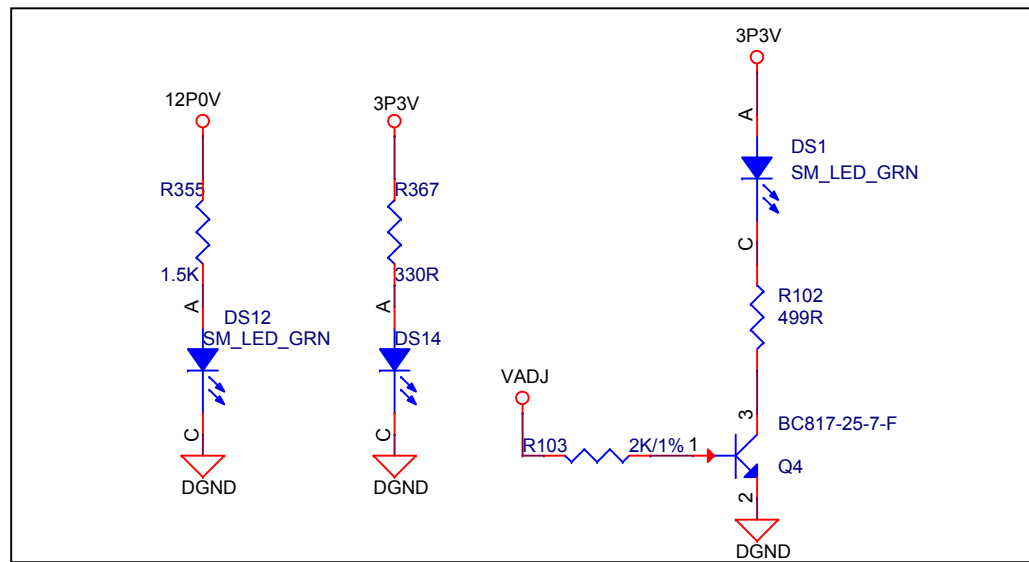


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FMC CONNECTOR-LPC MALE



BOARD DETECT OPTIONS



	FMC_BRD_DETECT1	FMC_BRD_DETECT2
MIPI SENSOR BOARD	0	1



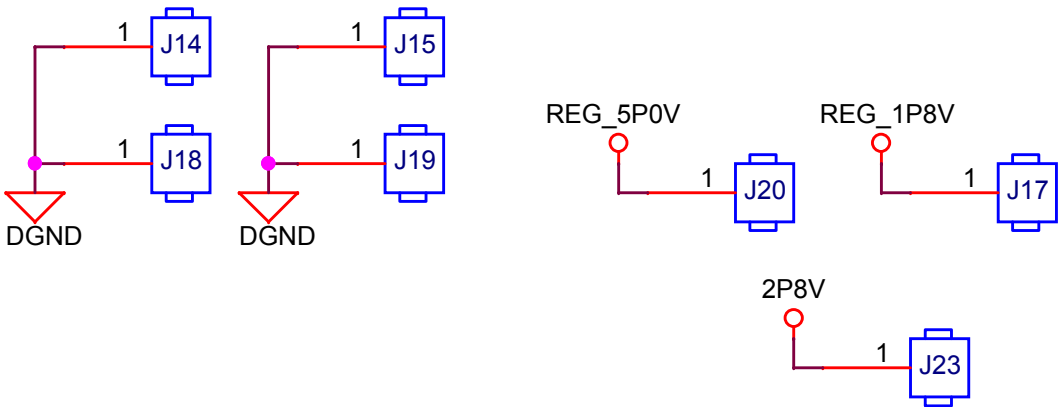
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MECHANICALS

BOARD MOUNTING HOLES



TEST POINTS



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