TU0565
Tutorial
Low Power RTG4 FPGA

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

The following is a summary of the changes made in this revision.

- Updated the document for Libero SoC v2021.2.
- Updated Figure 3 on page 5, Figure 10 on page 9, Figure 11 on page 10, Figure 14 on page 11, Figure 16 on page 13, and Figure 26 on page 16.
- Replaced Table 2 on page 12.
- Updated Table 4 on page 18 and Table 5 on page 21.

1.2 Revision 3.0

The following is a summary of the changes made in this revision.

- Renamed section Generating the Programming File and Programming the Board to Setting Up the Demo Design, page 17.
- Added section Programming the Device, page 18.
- Added Appendix 1: Programming the Device Using FlashPro Express, page 22.
- Added Appendix 2: Running the TCL Script, page 25.
- Removed the references to Libero version numbers.

1.3 Revision 2.0

Updated the document for Libero SoC v11.9 SP1.

1.4 Revision 1.0

The first publication of this document.

2 Low Power RTG4 FPGA

RTG4™ FPGAs are designed to meet the need of low power. RTG4 devices exhibit lower power consumption in static and dynamic modes. The static mode is achieved by powering-down the fabric CCC. This tutorial describes how to:

- Measure the total dynamic power using Microsemi Power Estimator and SmartPower.
- Measure the total dynamic power on the board.
- Measure the total static power using Power Estimator and SmartPower.
- Measure the total static power on the board.

The following functionalities are described in the subsequent sections:

- Creating a New Project Using Libero® System-on-Chip (SoC)
- Creating the SmartDesign
- Importing and Deriving Constraint Files
- Generating Power Report using Smart Power Tool
- Obtaining Resource Utilization Report
- Generating the Programming File and Programming the Board
- Measuring On-Board Power
- Measuring the Low Power Using Power Estimator Tool

2.1 Design Requirements

The following table lists the design requirements to run the low power RTG4 FPGAs tutorial.

Table 1 • **Design Requirements**

Requirement	Version
Hardware	
RTG4 FPGA Development Kit: • 12 V adapter • USB A to mini-B cable	Rev B or later
Host PC or laptop	64-bit Windows 7 and 10
Multimeter/DVM	Any
Software	
Libero SoC	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this reference design.
FlashPro Express	

Note: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

2.2 Prerequisites

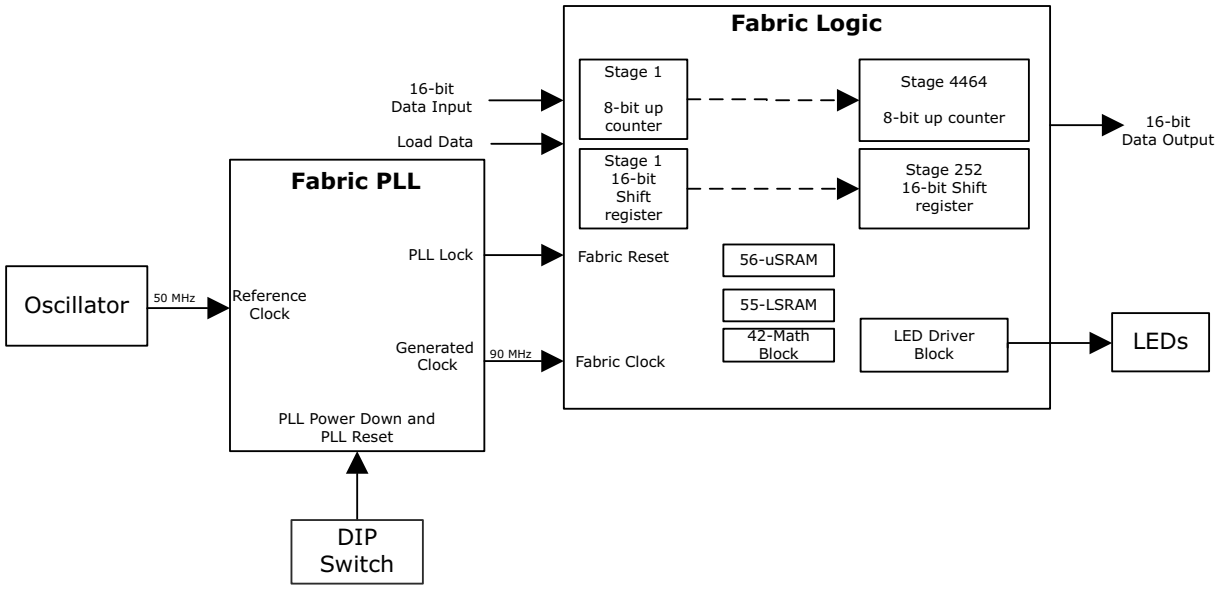
1. Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location: *https://www.microsemi.com/product-directory/design-resources/1750-libero-soc*
2. Download and extract the design files from the following link:
   http://soc.microsemi.com/download/rsc/?f=rtg4_tu0565_df
   The design file consists of Libero SoC project, VHDL files, RTG4 power estimator, and programming files (*.job). Refer to the `Readme.txt` file included in the design file for the directory structure and description.

2.3 Demo Design

The low power design file consists of a 50 MHz oscillator, a fabric CCC (FCCC), and a fabric logic block. The FCCC is configured to provide an 90 MHz clock to the fabric logic. The 50 MHz oscillator is the reference clock source for FCCC. The lock signal is used as the reset signal to the fabric logic. The fabric logic has 4464 stages of 8-bit loadable up-counters, 252 stages of 16-bit shift registers, 55 LSRAM blocks, 56 µSRAM blocks, and 42 math blocks. It also has an LED driver block, which is connected to a set of LEDs to monitor the state of the fabric while entering and exiting low power mode.

The following figure illustrates the block diagram of the design.

Figure 1 • **Design Block Diagram**



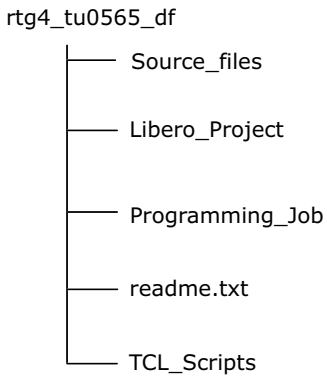
2.3.1 Introduction

The demo design includes:

- Libero_Project
- Programming_Job
- Source files
- Readme file
- TCL_Scripts

The following figure illustrates the top-level structure of the design files. For further details, refer to the `Readme.txt` file.

Figure 2 • **Design Files Top-Level Structure**



2.3.2 Extracting the Design Files

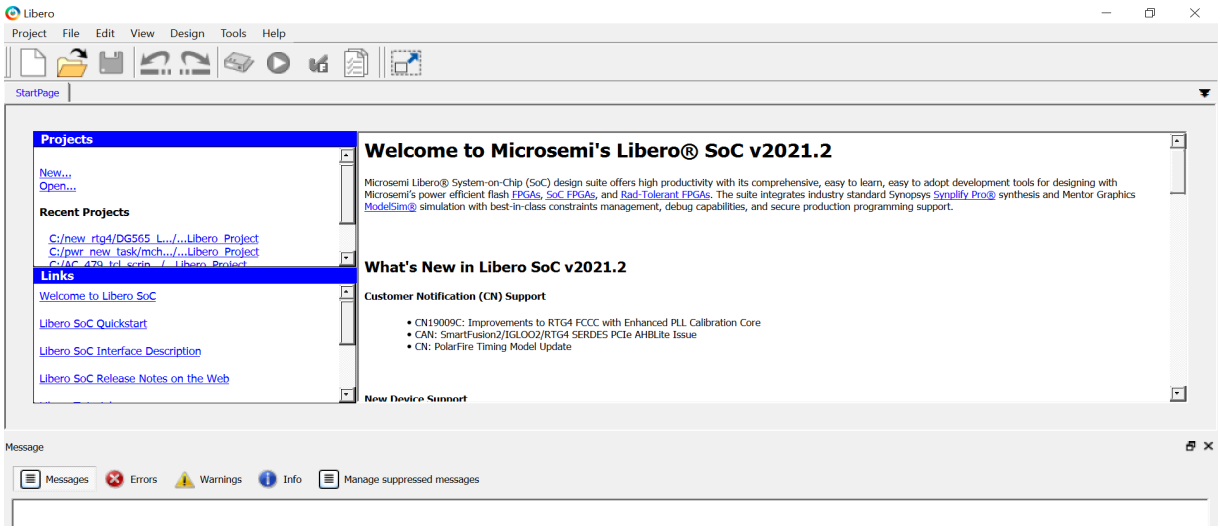
Extract the `rtg4_tu0565_df.zip` file to the <C:\ or D:\>Microsemi_prj folder in the local system. Verify that all files are in the directory, as mentioned in the `Readme.txt` file.

2.4 Creating a New Project Using Libero SoC

This section describes how to create a new project using Libero SoC.

1. Go to **Start** > **Programs** > **Microsemi** > **Libero SoC v(xx.x)** SP1> **Libero SoC v(xx.x) SP1**. The **Libero SoC Project Manager** window is displayed, as shown in the following figure.

Figure 3 • **Libero SoC Project Manager**

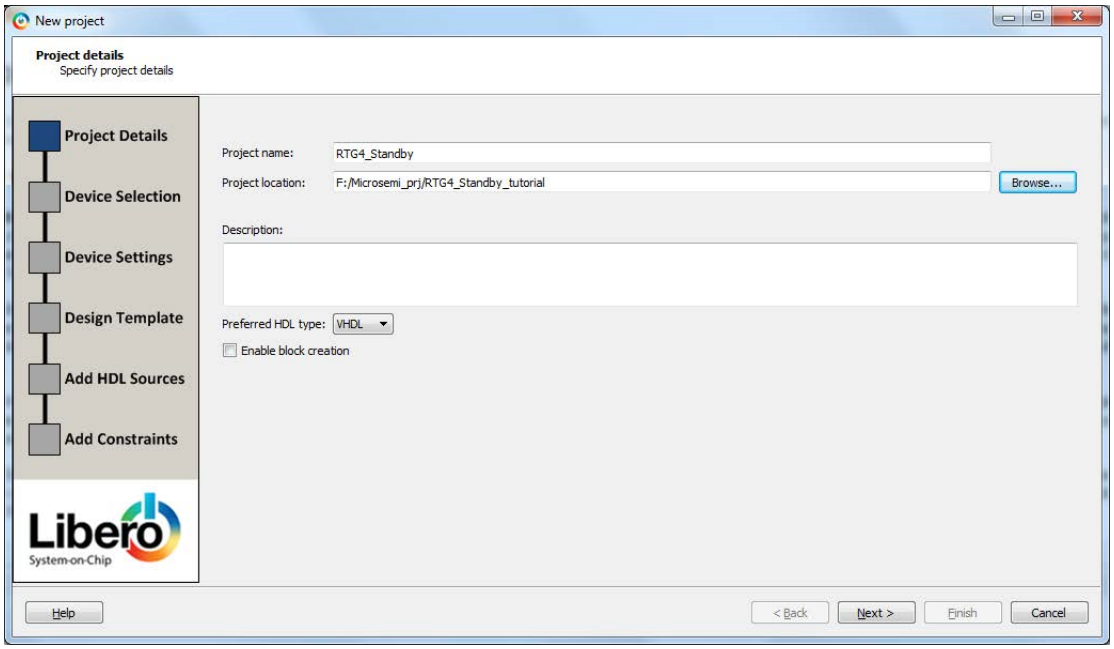


2. Create a new project using one of the following options:
   - Click **New...** in the **Projects** panel on the **Start Page**.
   - In the Libero SoC menu, go to **Project > New Project**.

The **New Project-Project Details** window is displayed, as shown in Figure 4 on page 6.

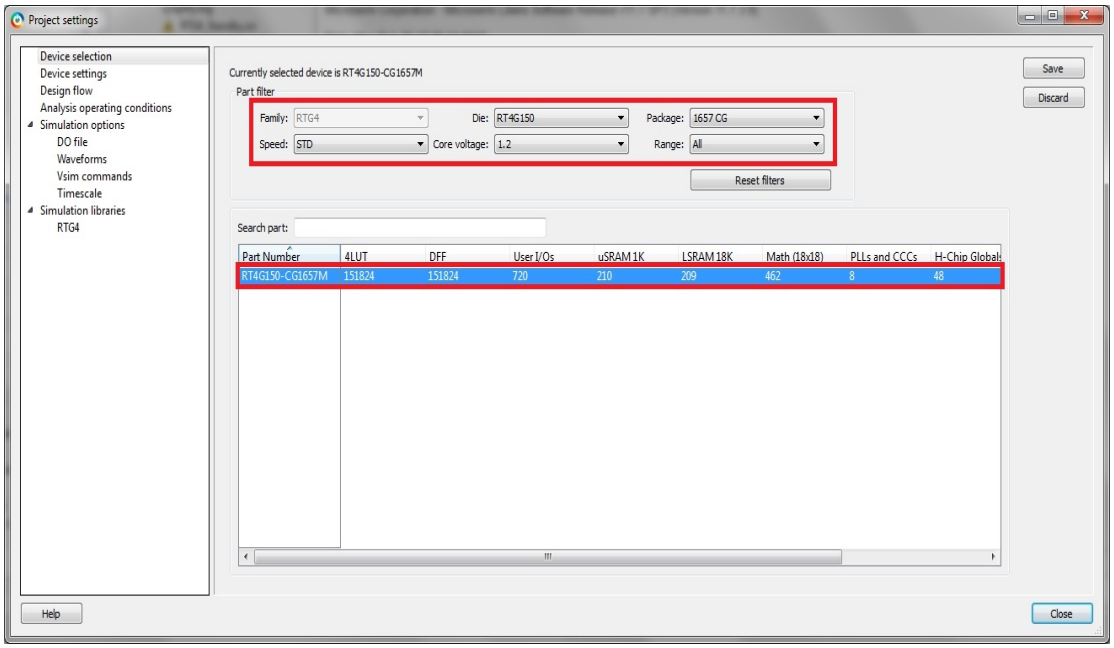
3. Enter the following information in the **New Project - Project Details** window.
   - **Project name**: RTG4_Standby
   - **Project location**: <C:\ or D:\>Microsemi_prj\RTG4_Low_Power_tutorial
   - **Preferred HDL type**: VHDL
   - **Enable block creation**: Not selected

Figure 4 • **New Project - Project Details**



4. Click **Next**. The **New Project - Device Selection** window is displayed.
5. Select the following values from the drop-down lists under **Part filter.**
   - **Family**: RTG4
   - **Die**: RT4G150
   - **Package**: 1657 CG
   - **Speed**: STD
   - **Core voltage**: 1.2
   - **Range**: MIL

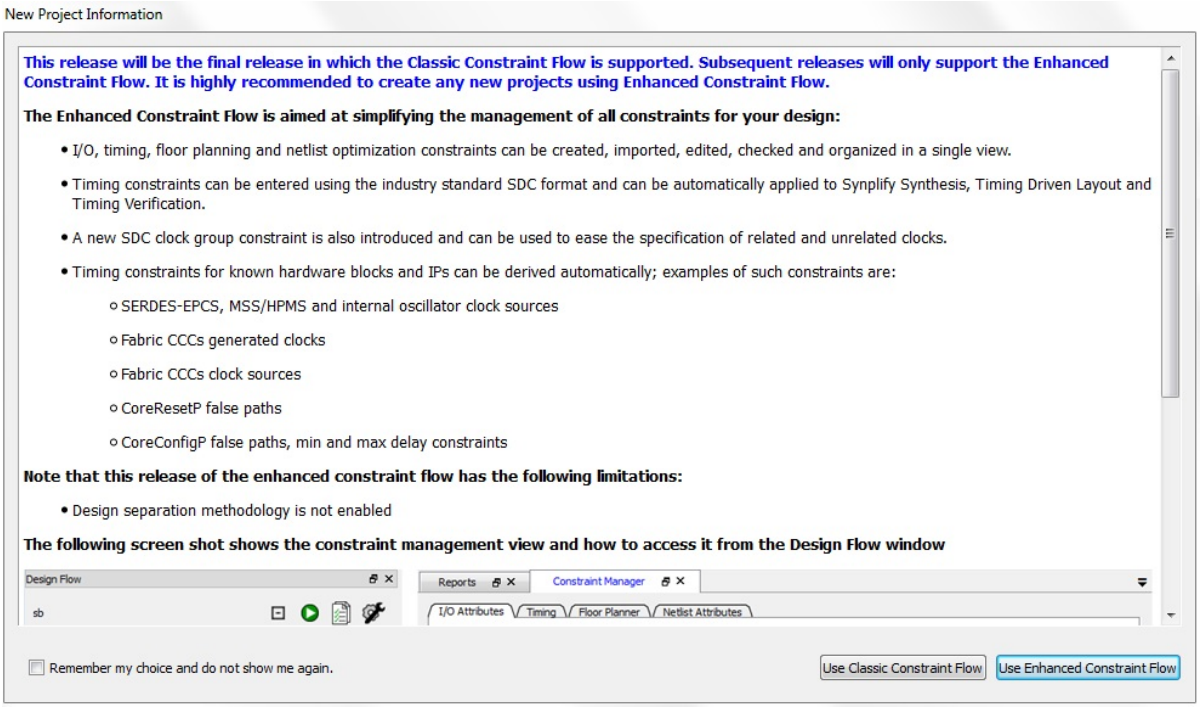
Figure 5 • **New Project - Device Selection**



6. Select the **RT4G150-CG1657M** device from the list and the associated supported details for various features are listed in the respective columns.

7. Click **Finish**. The **New Project Information** window is displayed.
8. Click **Use Enhanced Constraint Flow** in the **New Project Information** window. The **Design Flow** window is displayed.

Figure 6 • **New Project Information**

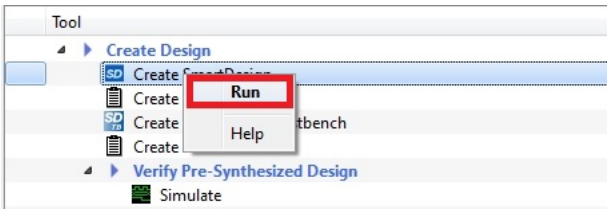


2.5 Creating the SmartDesign

This section describes how to create SmartDesign and generate the SmartDesign component.

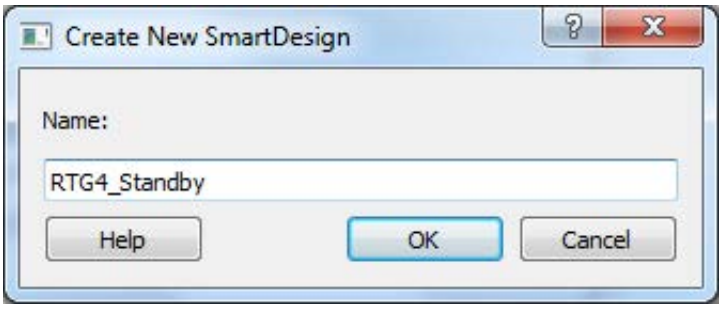
1. In the **Design Flow** window, expand **Create Design**, as shown in the following figure.
2. Right-click **Create SmartDesign** and click **Run**. The **Create New SmartDesign** dialog box is displayed.

Figure 7 • **Creating SmartDesign**



3. Enter the **Name** as **RTG4_Standby** and click **OK**. A new SmartDesign canvas is displayed.

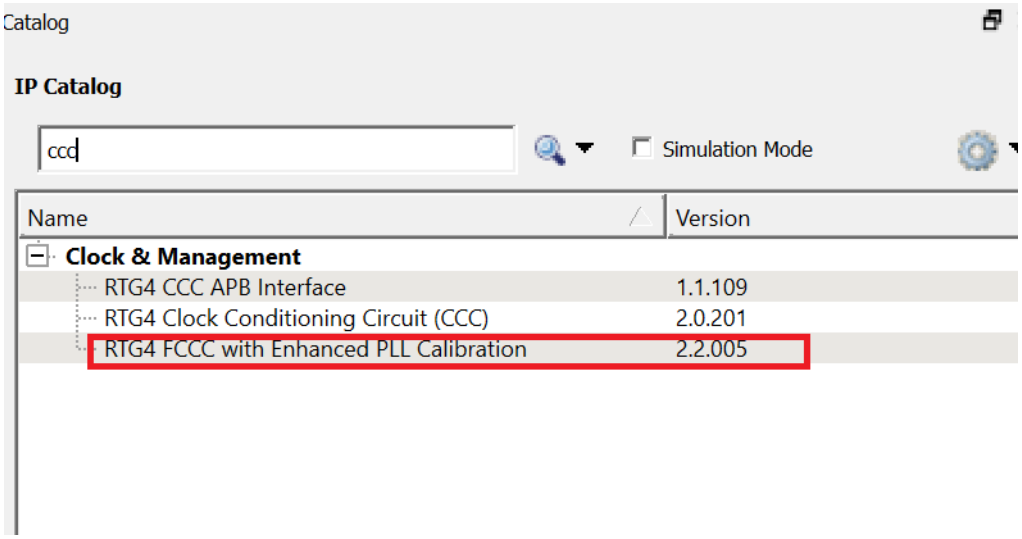
Figure 8 • **Creating New SmartDesign**



Now you can add different macros and IP cores to the SmartDesign canvas as required for your design.

4. Click **Catalog** tab and expand **Clock & Management** to add an RTG4FCCCECALIB to the canvas, as shown in the following figure.

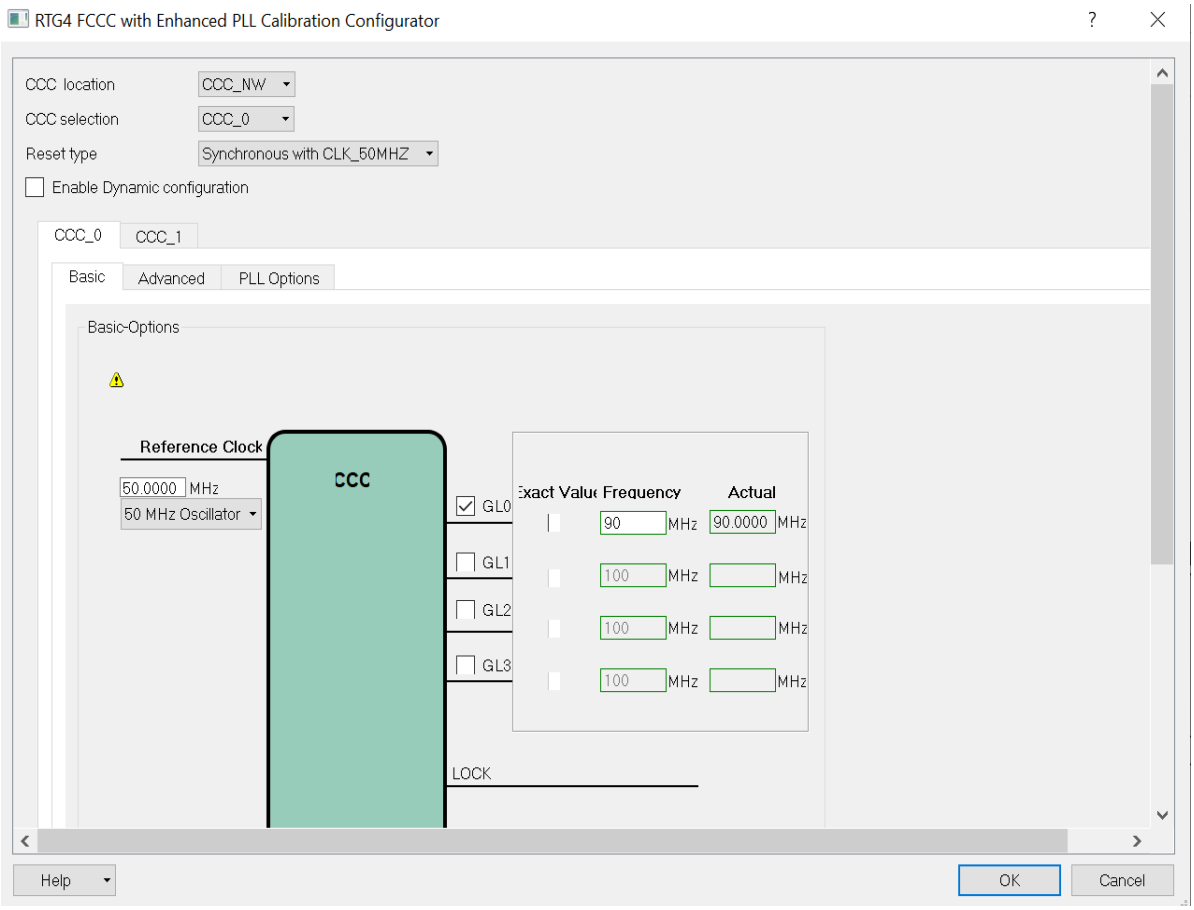
Figure 9 • **Clock and Management**



5. Drag and drop the **RTG4FCCCECALIB** to the SmartDesign canvas.

6. Double-click the **RTG4FCCCECALIB** component in the SmartDesign canvas. The **RTG4FCCCECALIB Configurator** window is displayed, as shown in the following figure.

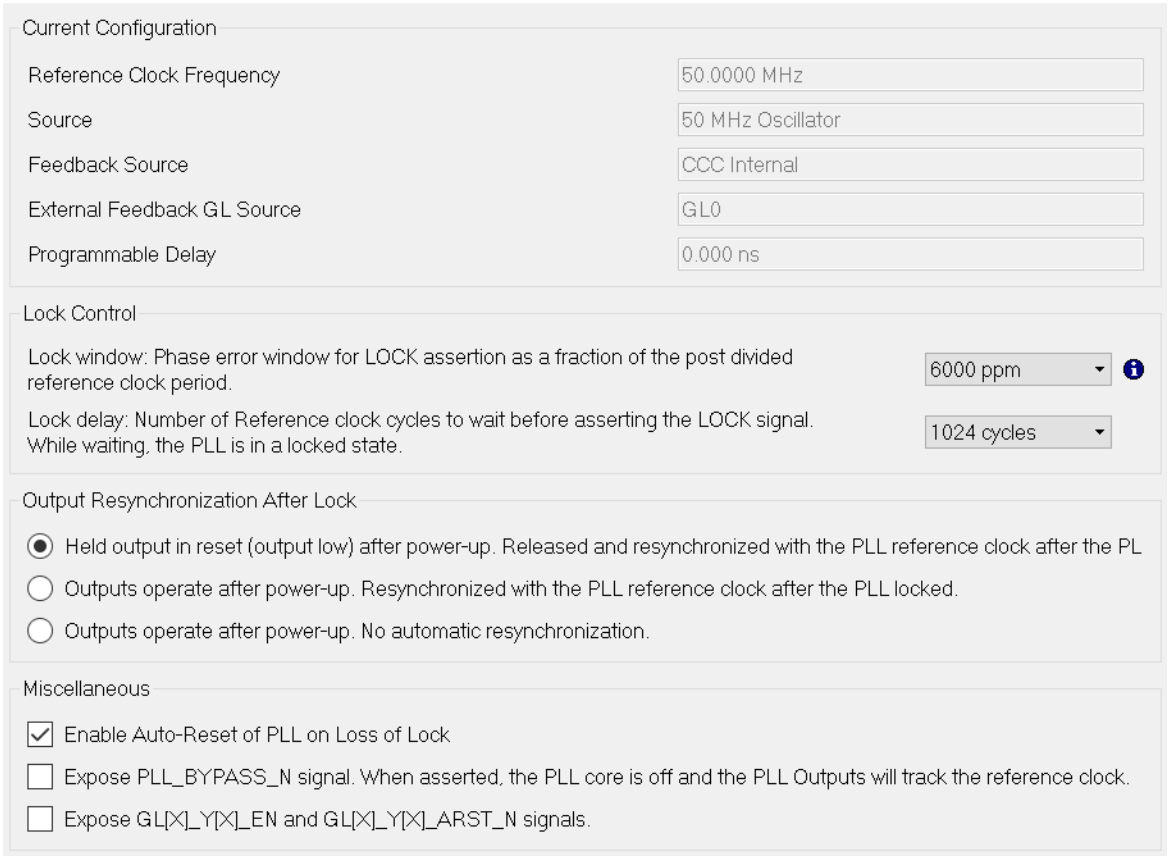
Figure 10 • **Configuring Fabric CCC**



Note: This design uses an FCCC to generate a 90 MHz internal clock for the fabric. The FCCC reference clock is the 50 MHz oscillator.

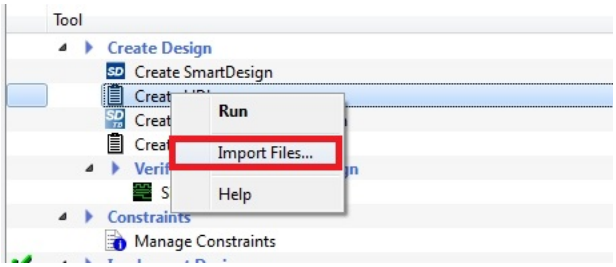
7. Click **PLL Options** tab, select the **Expose PLL_ARST_N and PLL_POWERDOWN_N signals** check box, as shown in the following figure.

Figure 11 • **Configuring PLL Power-Down Signals**



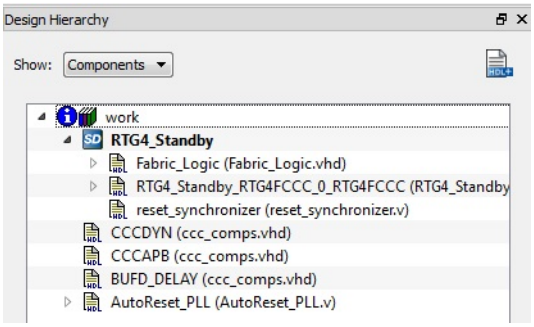
8. Click **OK**.
9. Click **IP Catalog** tab and expand **Macro Library** and select the **RCOSC_50MHZ** macro, which is the 50 MHz oscillator macro.
10. Drag and drop the **RCOSC_50MHZ** component to the SmartDesign canvas.
11. Right-click **Create HDL** under **Create Design** in the **Design Flow** tab and click **Import File...** to import the source files for the user fabric logic, as shown in the following figure.

Figure 12 • **Importing HDL Source Files**



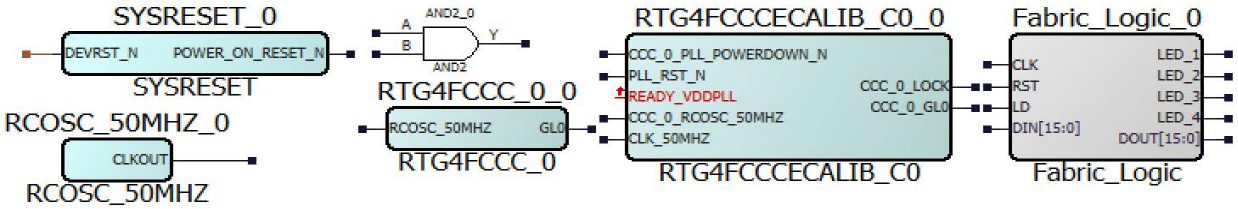
12. Browse to `<Download folder > \rtg4_tu0565_df\Source_files\VHDL` and select all the VHDL files available in the folder, and click **Open**. The files are listed in the **Design Hierarchy** tab, as shown in the following figure.

Figure 13 • **Listing the Imported Files in the Design Hierarchy Tab**



13. Drag and drop the **Fabric_Logic** and the reset_synchronizer_0 component from **Design Hierarchy** into the **SmartDesign** canvas, as shown in the following figure.

Figure 14 • **Adding Components into SmartDesign Canvas**



2.5.1 Connecting Components and Generating SmartDesign

The SmartDesign tool in Libero SoC has a connection mode that allows components to be connected using a drag and drop mechanism.

To connect the components:

1. Switch to connection mode in SmartDesign by clicking **Connection Mode** option in toolbar, as shown in the following figure.

Figure 15 • **SmartDesign Canvas Connection Mode**

2. To connect ports in the SmartDesign canvas, drag and drop the **CLKOUT** of the **RCOSC_50MHZ_0** component to the **RCOSC_50MHZ** port of the **RTG4FCCC_0** component. You can also connect the ports by selecting the ports while holding down the Ctrl key on your keyboard, right-clicking any of the selected ports, and click **Connect**.
3. Connect other components in the SmartDesign canvas as listed in the following table.

Table 2 • **Connections in Canvas**

From	To
SYSRESET_0: POWER_ON_RESET_N	AND2_0: B
AND2_0: Y	RTG4FCCCECALIB_C0: PLL_POWERDOWN_N; RTG4FCCCECALIB_C0: PLL_ARST_N
RTG4FCCC_0_0: GL_0	RTG4FCCCECALIB_C0: CLK_50MHz
RCOSC_50MHz_0: CLKOUT	RTG4FCCCECALIB_C0: CCC_0_RCOSC_50MHz
RTG4FCCCECALIB_C0: GL0	Fabric_Logic_0: CLK
RTG4FCCCECALIB_C0: LOCK	Fabric_Logic_0: RST

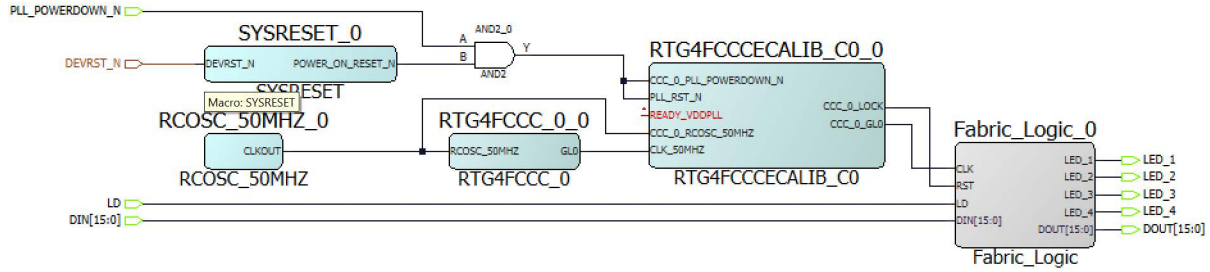
4. To exit from **Connection Mode**, disable the **Release Connection** mode by clicking the button in SmartDesign canvas.

5. Right-click any of the following ports and click **Promote to Top Level** to promote the ports:
   - AND2_0: ASYSRESET_0: DEVRST_N
   - Fabric_Logic_0: LD
   - Fabric_Logic_0: DIN[15:0]
   - Fabric_Logic_0: DOUT[15:0]
   - Fabric_Logic_0: LED_1
   - Fabric_Logic_0: LED_2
   - Fabric_Logic_0: LED_3
   - Fabric_Logic_0: LED_4

The SmartDesign canvas appears as shown in Figure 16 on page 13.

6. Drag and drop the components to the required location or right-click the **Auto Arrange** icon on the toolbar to improve the appearance of the canvas.

Figure 16 • **SmartDesign Canvas**



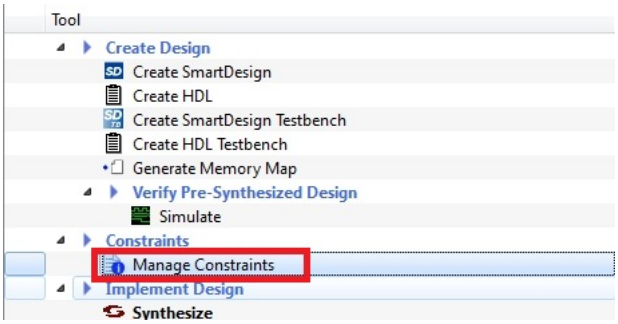
7. Go to **File** > **Save RTG4_Standby** to save the design.
8. Generate the design by selecting **SmartDesign** > **Generate Component**. A message appears in the Libero log window, confirming the successful generation of the low power RTG4 FPGAs design.
9. Go to **File** > **Close RTG4_Standby** to close the design.

2.6 Importing and Deriving Constraint Files

This section describes how to import a physical design constraint (PDC) file to assign I/O attributes and pins for the layout and how to derive timing constraints to meet the timing requirements.

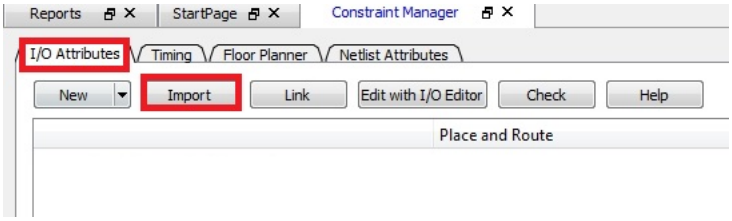
1. In the **Design Flow** tab, expand **Constraints** and click **Manage Constraints**, as shown in the following figure. The **Constraint Manager** window is displayed.

Figure 17 • **Manage Constraints**



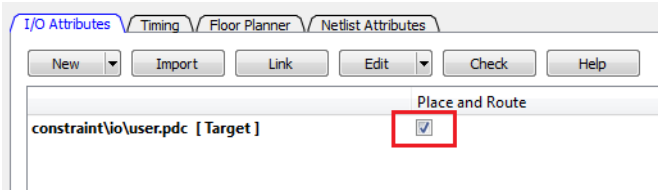
2. In the **Constraint Manager** window, click the **I/O Attributes** tab and click **Import** to import the *.PDC file, as shown in the following figure.

Figure 18 • **Import Constraints**



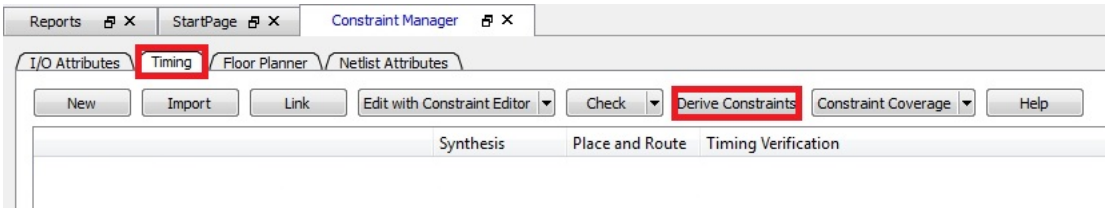
3. Select the Place and Route checkbox to use the imported PDC file during place and route.

Figure 19 • **Selecting the Place and Route Check Box**



4. Browse to the location <Download folder>RTG4_Low_Power_tutorial\Source_files in your local system, select the `user.pdc` file, and click **Open**. The PDC file is imported for this design.
5. Click **Timing** tab and click **Derive Constrains**, as shown in the following figure.

Figure 20 • **Derive Constraints**



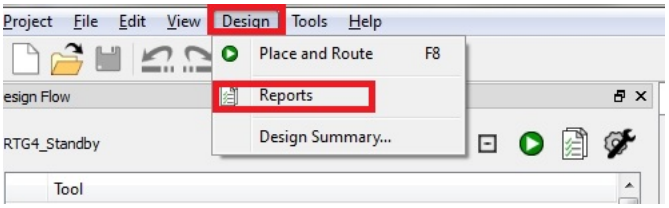
6. Press **Yes**, when asked to associate the derived constraints (*.SDC) files to Synthesis; place and route; timing; and verification tools. The timing constrains are derived for the design.
7. Run **Synthesis** from Libero Design Flow.
8. Run Place and Route from Libero Design flow.

2.7 Generating Resource Utilization Report

This section describes how to generate the resource utilization report for the design. Resource utilization report shows the used resources out of total resources available in this design.

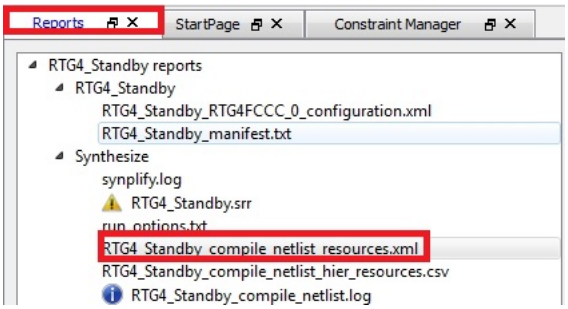
1. Click **Design** from the menu bar and click **Reports**, as shown in the following figure. The **Project Reports** window is displayed.

Figure 21 • **Opening Reports**



2. Click **RTG4_Standby_compile_netlist_resources.xml** under **Synthesize**, as shown in the following figure.

Figure 22 • **Resource Utilization Report**



The **Resource Usage** report shows the strategies of **Type**, **Used**, **Total**, and **Percentage**.

Figure 23 • **Resource Usage**

Resource Usage

Type	Used	Total	Percentage
4LUT	85957	151824	56.62
DFF	81031	151824	53.37
I/O Register	0	2160	0.00
User I/O	38	720	5.28
-- Single-ended I/O	38	720	5.28
-- Differential I/O Pairs	0	360	0.00
RAM64x18	56	210	26.67
RAM1K18	55	209	26.32
MACC	42	462	9.09
H-Chip Globals	4	48	8.33
CCC	1	8	12.50
RCOSC_50MHZ	1	1	100.00
SERDESIF Blocks	0	6	0.00
FDDR	0	2	0.00
GRESET	1	1	100.00

Figure 24 • **I/O Resource Usage**

I/O Function

Type	w/o register	w/ register	w/ DDR register
Input I/O	18	0	0
Output I/O	20	0	0
Bidirectional I/O	0	0	0
Differential Input I/O Pairs	0	0	0
Differential Output I/O Pairs	0	0	0

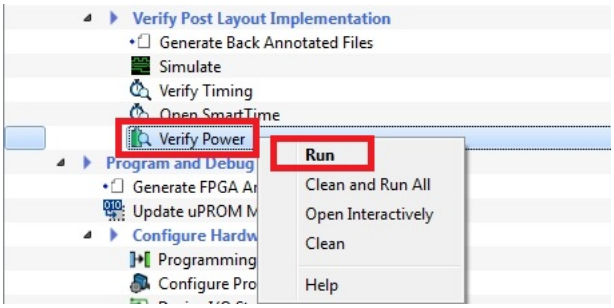
Note: These values must be entered in the Power Estimator Excel sheet to measure the total power.

2.8 Generating Power Report Using Smart Power Tool

This section describes how to generate the power report for the design. Power report includes total power, static power, dynamic power, and power breakdown by rail, by clock, and by type.

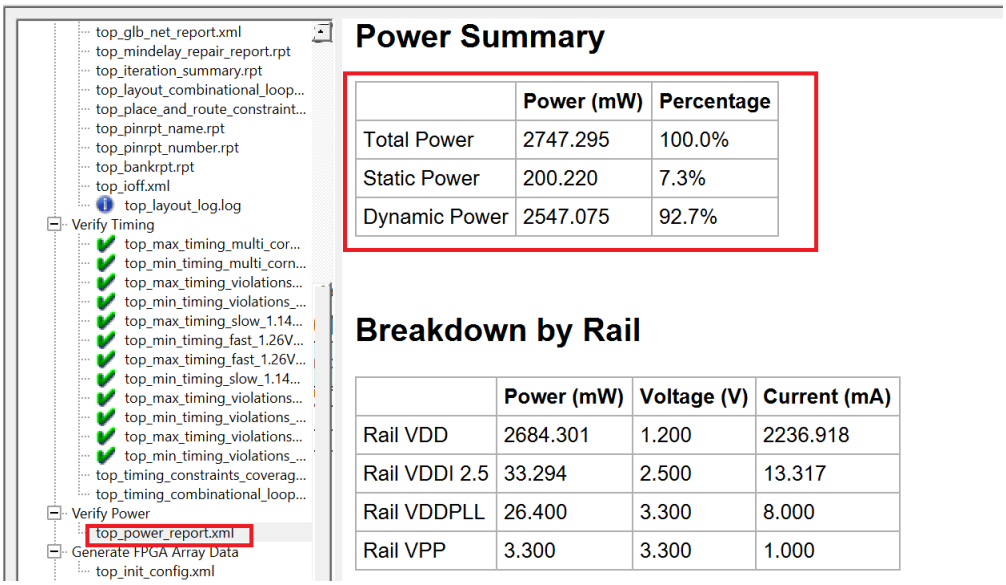
- On the **Design Flow** tab, expand **Implement Design**, right-click **Verify Power** and select **Run**, as shown in the following figure. It runs **Synthesize** and **Place and Route**.

Figure 25 • **Power Report**



The following figure shows a sample generated power report.

Figure 26 • **Generated Power Report**



2.9 Setting Up the Demo Design

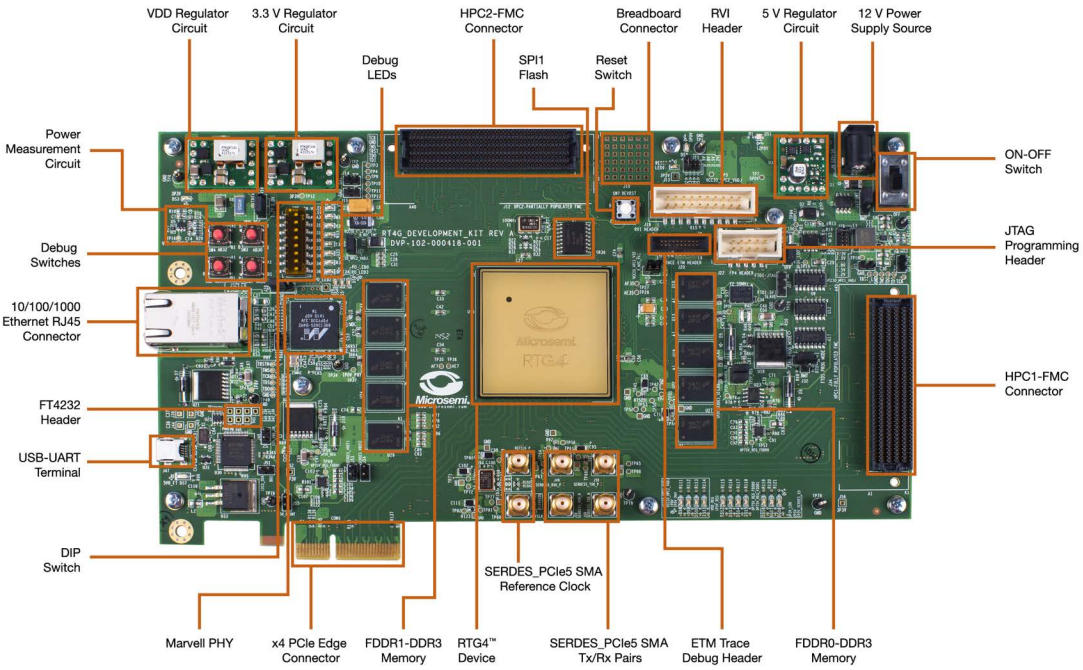
This demo design uses the RTG4 Development Kit board. Figure 27 shows the RTG4 Development Kit board. The following steps describe how to set up the demo design:

1. Connect the power supply cable to the **J9** connector on the board.
2. Connect the USB A to mini B cable to **J47** connector on the board.
3. Connect the jumpers to the RTG4 Development Kit board, as listed in the following table.

Table 3 • **Jumper Settings**

Jumper	Settings
J16	2-3 installed
J17	1-2 installed
J19	1-2 installed
J21	1-2 installed
J23	1-2 installed
J26	1-2 installed
J27	1-2 installed
J28	1-2 installed
J32	1-2 installed
J33	1-2 installed
	3-4 installed

Figure 27 • **RTG4 Development Kit Board**



2.10 Programming the Device

To program the RTG4 Development Kit with the job file provided as part of the design files using FlashPro Express software, refer to Appendix 1: Programming the Device Using FlashPro Express, page 22.

2.11 Power Measurement

2.11.1 On-Board Power Measurement

For applications that require current measurement, a high-precision operational amplifier circuitry (U5 with gain 5) is provided on the board to measure the output voltage at test point TP16.

The following steps describe how to measure the core power:

1. Measure the output voltage (V) at **TP16**.
2. Measure the core voltage (V) at **TP14**.
   Therefore, the consumed core power is calculated using the following formula:
   P = V (TP14) × V (TP16) × 4
   Multimeter or DVM is used to measure the output voltage and core voltage.
3. Connect the positive terminal of a standard digital voltmeter (DVM)/multimeter to **TP16** and the negative terminal to **TP8**. Note the digital voltmeter/multimeter reading.
4. Connect the positive terminal of a standard digital voltmeter (DVM)/multimeter to **TP14** and the negative terminal to **TP8**. Note the digital voltmeter/multimeter reading.
5. Calculate the power values using the equations.

2.11.1.1 Total Core Power (Dynamic and Static)

To calculate total power:

1. Reset the board by pressing and releasing the **Reset** button (that is, **SW7 DEVRST**).
2. Observe the pattern of LEDs 1, 2, 3, and 4 after resetting the board.
3. If LEDs blink, measure the power else change the position of DIP slide switch (PIN: SW5-1, DIP switch) and measure the power.

2.11.1.2 Static Power

To calculate static power:

1. Observe the pattern of LEDs 1, 2, 3, and 4.
2. If LEDs blink, change the position of DIP slide switch (PIN: SW5-1, DIP switch).
3. Measure the power.

The following table lists the power measurements on the board:

Table 4 • **Power Measurements**

Measurement	V (TP16) (mV)	V (TP14) (mV)	Power (mW) = V(TP16) × V (TP14) × 4
Total Power	598	1201	2872
Static Power	70	1206	337

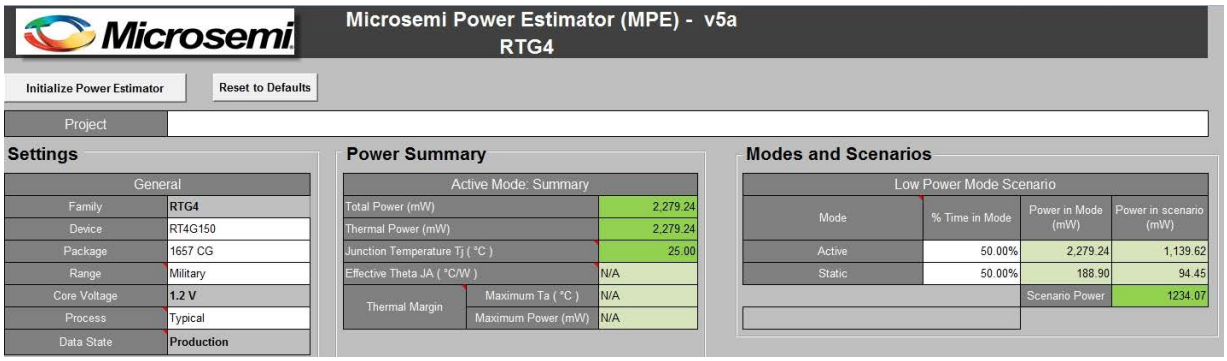
2.11.2 Measuring Power Using Power Estimator Tool

The following steps describe how to use power estimator to calculate total power, dynamic power, and static power.

1. Download the **Power Estimator** spreadsheet and user guide from:
   - *RTG4 Power Estimator*
   - *RTG4 Power Estimator User Guide*
2. Or open the power estimator spreadsheet from `<Download folder>\Source_file\RTG4_power_calculator.xls` and go to the **Summary** worksheet that provides the device settings and power summary.

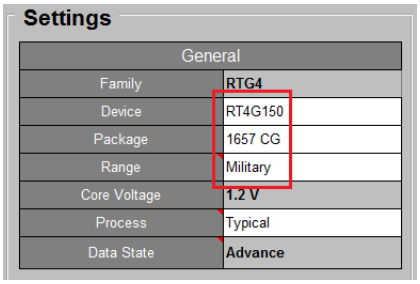
3. Reset the RTG4_power_calculator by pressing **Reset** to **Defaults**, as shown in the following figure.

Figure 28 • **Reset to Defaults**



4. Change the device settings by selecting from the respective drop-down lists, as shown in the following figure:
   - **Device**: RT4G150
   - **Package**: 1657 CG
   - **Range**: Military

Figure 29 • **Settings Section in the Device Settings and Summary Worksheet**



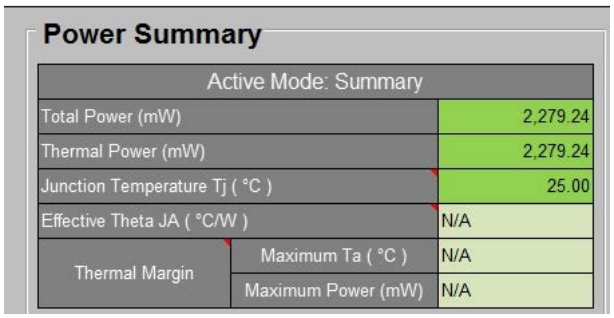
Refer to Generating Resource Utilization Report, page 14 for getting resource utilization for punching values to power estimator.

5. Click **Clock** worksheet and enter the following information in the sheet.
   - **Name**: System
   - **Clock Frequency (MHz)**: 90
   - **Fanout**: Number of DFF in the resource utilization report
   - **Global Enable Rate**:100
6. Click **Logic** worksheet and enter the following information in the sheet.
   - **Name**: System
   - **Clock Frequency (MHz)**: 90
   - **Number of Registers**: Number of DFF in the resource utilization report
   - **Number of LUTs**: Number of LUTs in the resource utilization report
   - **Fanout**: 3
   - **Toggle Rate**: 12.5
7. Click **LSRAM** worksheet and enter the following information in the sheet.
   - **Name**: System
   - **Number of LSRAM Blocks**: Number of LSRAM blocks in the resource utilization report

- PORT A and B
  - **Clock Frequency (MHz)**: 90
  - **Write Rate**: 12.5%
  - **Enable Rate**: 12.5%

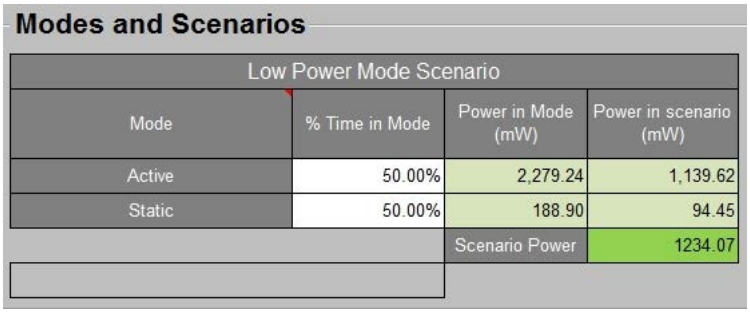
8. Click **uSRAM** worksheet and enter the following information in the sheet.
    - **Name**: System
    - **Number of uSRAM Blocks**: Number of uSRAM blocks in the resource utilization report
- PORT A and B
    - **Read Clock Frequency (MHz)**: 90
    - **EnableRate**:12.5%
- PORT C
    - **Write Clock Frequency (MHz)**: 90
    - **Enable Rate**: 12.5%
9. Click **Math Block** worksheet and enter the following information in the sheet.
    - **Name**: System
    - **Clock Frequency (MHz)**: 90
    - **Number of Math Blocks**: Number of math blocks in the resource utilization report
    - **Data Toggle Rate**: 12.5%
10. Click **I/O** worksheet and enter the following information in the sheet.
    - **Name**: System
    - **Bank Type**: MSIO
    - **I/O Standard**: LVCMOS25
    - **I/P Pins**: Refer Resource Utilization Report.
    - **O/P Pins**: Refer Resource Utilization Report.
    - **Bidir Pins**: Refer Resource Utilization Report.
    - **ODT**: No_ODT
    - **Output Drive (mA)**: 2
    - **Output Load (pF)**: 5
    - **Clock (MHz)**: 90
    - **Data Rate**: Data
    - **Toggle Rate**: 12.5%
    - **Output Enable**: 50%
11. Click **CCC** worksheet and enter the following information in the sheet.
    - **Name**: system
    - **Reference Clock Frequency (MHz)**: 50
    - **PLL Output Clock Frequency (MHz)**: 90
    - **Output1 Frequency (MHz)**: 90
12. Click **Summary** worksheet to get the total power. The **Power Summary** section is populated with the total power consumed during active mode, as shown in the following figure.

Figure 30 • **Power Summary**



The **Modes and Scenarios** section displays the total power in both active, as well as static modes as shown in the following figure.

Figure 31 • **Modes and Scenarios**



13. Close the **Power Estimator**.

2.11.2.1 Summary of Power Measurement

Based on different methods of power measurement, the values of total power, dynamic, and static power are shown in the following table.

Table 5 • **Summary of Power Measurement**

Power Measurement Method	Total Power (mw)	Dynamic (mw)	Static Power (mw)
Power Estimator	2535.70	2387.6	148.08
Smart Power	2747.295	2547.075	200.220
On Board	2872	2535	337

2.12 Conclusion

This tutorial demonstrates the low power capability of RTG4 FPGAs. PLL power-down signal can be used for switching between normal and standby mode. The smart power tool in Libero SoC and the power estimator tool provide initial power values of the design, and the power values are aligned with the on-board power.

3 Appendix 1: Programming the Device Using FlashPro Express

This section describes how to program the RTG4 device with the programming job file using FlashPro Express.

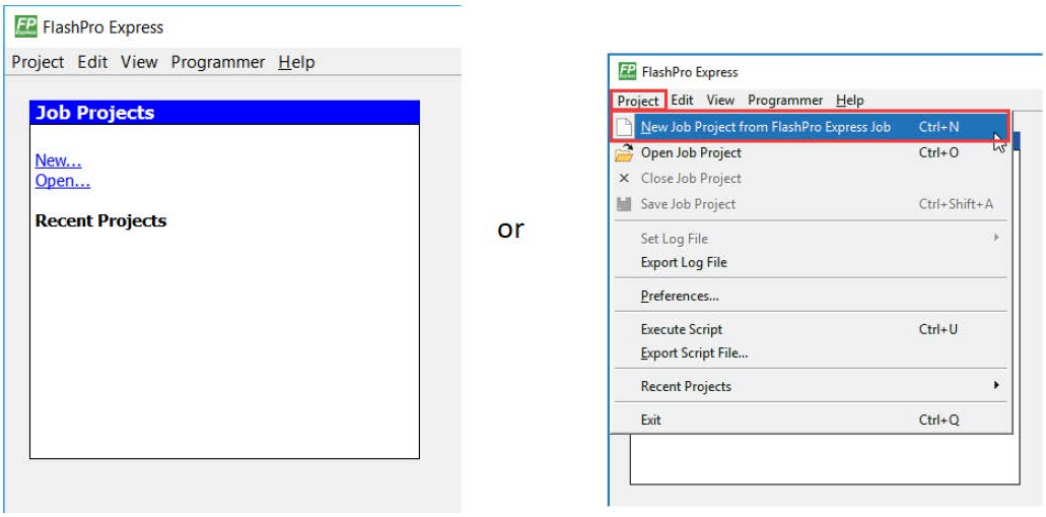
To program the device, perform the following steps:

1. Ensure that the jumper settings on the board are the same as those listed in *Table 3 of UG0617: RTG4 Development Kit User Guide*.
2. Optionally, jumper **J32** can be set to connect pins 2-3 when using an external FlashPro4, FlashPro5, or FlashPro6 programmer instead of the default jumper setting to use the embedded FlashPro5.

Note: The power supply switch, **SW6** must be switched **OFF** while making the jumper connections.

3. Connect the power supply cable to the **J9** connector on the board.
4. Power **ON** the power supply switch **SW6**.
5. If using the embedded FlashPro5, connect the USB cable to connector **J47** and the host PC. Alternatively, if using an external programmer, connect the ribbon cable to the JTAG header **J22** and connect the programmer to the host PC.
6. On the host PC, launch the **FlashPro Express** software.
7. Click **New** or select **New Job Project from FlashPro Express Job** from **Project** menu to create a new job project, as shown in the following figure.

Figure 32 • **FlashPro Express Job Project**



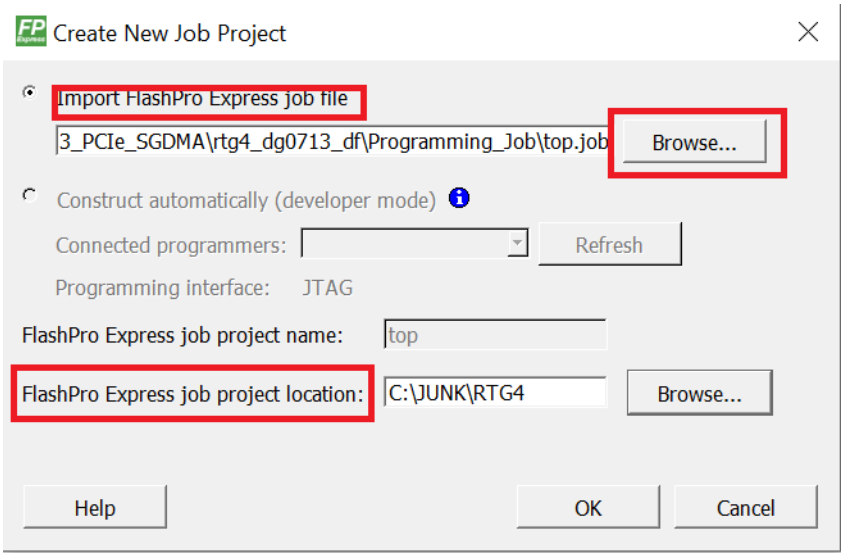
8. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:

- **Programming job file:** Click **Browse**, and navigate to the location where the .job file is located and select the file. The default location is:

  `<download_folder>\rtg4_tu0565_df\Programming_Job`

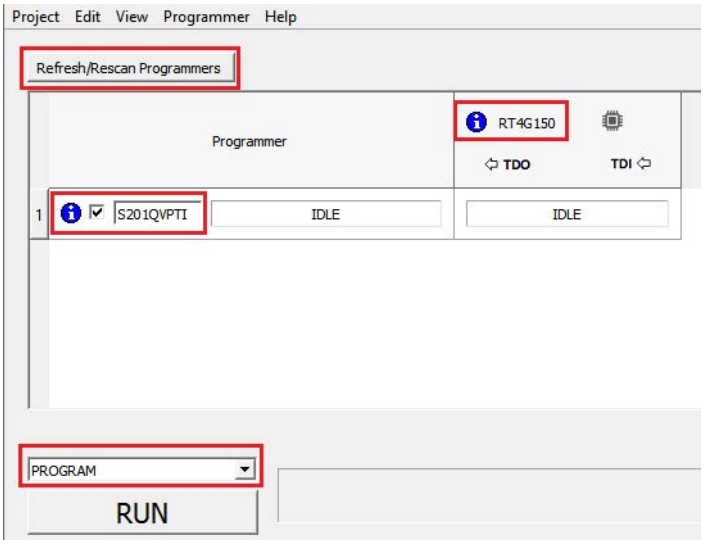
- **FlashPro Express job project location:** Click **Browse** and navigate to the desired FlashPro Express project location.

Figure 33 • **New Job Project from FlashPro Express Job**



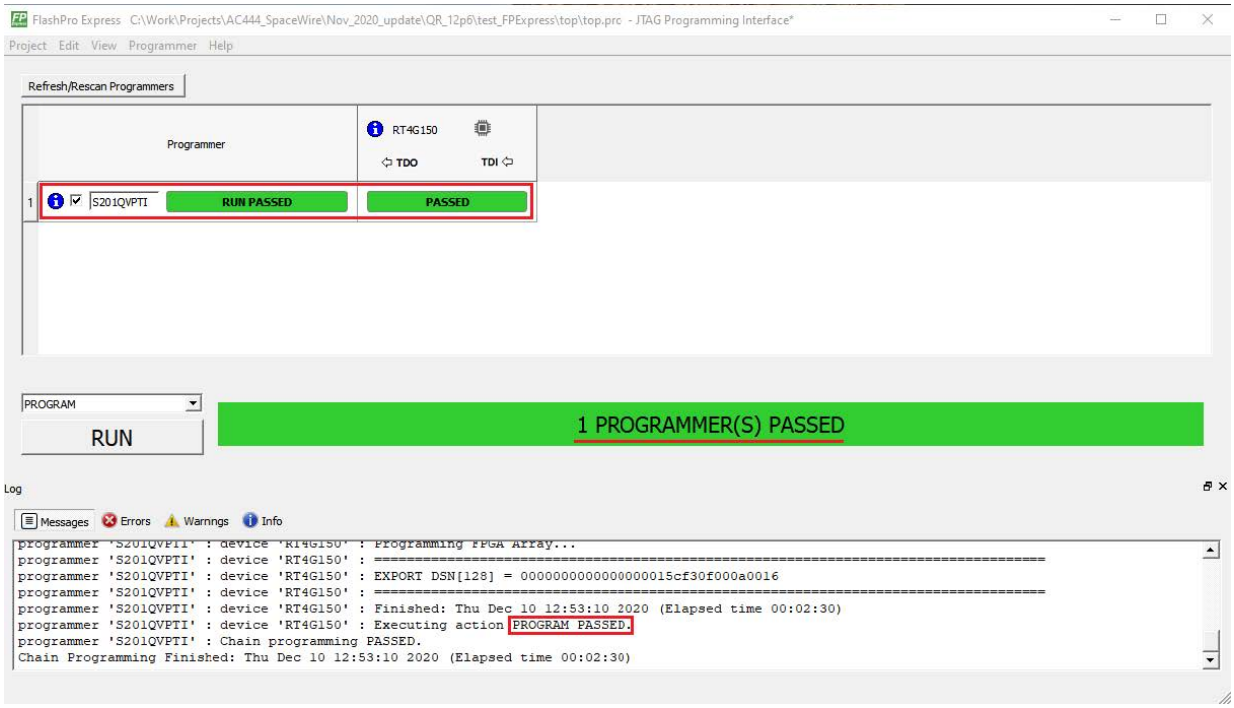
9. Click **OK**. The required programming file is selected and ready to be programmed in the device.
10. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan** Programmers.

Figure 34 • **Programming the Device**



11. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

Figure 35 • **FlashPro Express—RUN PASSED**



12. Close **FlashPro Express** or click **Exit** in the Project tab.

4 Appendix 2: Running the TCL Script

TCL scripts are provided in the design files folder under directory TCL_Scripts. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, follow the steps below:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click Browse and select `script.tcl` from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within TCL_Scripts directory.

For more information about TCL scripts, refer to **rtg4_tu0565_df/TCL_Scripts/readme.txt.**

Refer to *Libero® SoC TCL Command Reference Guide* for more details on TCL commands. Contact Technical Support for any queries encountered when running the TCL script.