SmartFusion2 and IGLOO2 PCIe Data Plane Demo Using 2 Channel Fabric DMA - Libero SoC 11.7

DG0517 Demo Guide

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1 Preface

1.1 Purpose

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA devices. It provides instructions on how to use the reference design.

1.2 Intended Audience

This user guide is intended for:

- FPGA designers
- Embedded designers
- System-level designers

1.3 References

The following documents are referred in this user guide.

- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide*
- *TU0456: SmartFusion2 SoC FPGA PCIe Control Plane Demo Tutorial*
- *TU0509: IGOO2 FPGA PCIe Control Plane Design Libero SoC Flow Tutorial*

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: *http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2*

Refer to the following web page for a complete and up-to-date listing of IGLOO2 device documentation: *http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga*

2 SmartFusion2 and IGLOO2 PCIe Data Plane Demo Using 2 Channel Fabric DMA

2.1 Introduction

This demo highlights the high-speed data transfer, the capability of SmartFusion2 and IGLOO2 devices through the PCIe interface. To achieve the high-speed data transfers, an advanced extensible interface (AXI) based direct memory access (DMA) controller is implemented in the FPGA fabric. An application, **PCIe_Demo** that runs in the host PC is provided for setting up and initiating DMA transactions from the SmartFusion2 or IGLOO2 PCIe endpoint to the host PC device. Drivers for connecting the host PC to the SmartFusion2 or IGLOO2 PCIe endpoint are provided as part of the demo deliverables.

Microsemi® provides three different PCIe data plane demos for SmartFusion2 devices:

- *DG0501: SmartFusion2 PCIe MSS HPDMA Demo Guide*: This demo shows the low throughput data transfers between PCIe and double data rate (DDR).
- *DG0535: SmartFusion2 PCIe Data Plane Demo using MSS HPDMA and SMC_FIC Demo Guide*: This demo shows the medium throughput data transfers between PCIe and embedded static random access memory (eSRAM).
- DG0517: SmartFusion2 and IGLOO2 PCIe Data Plane Demo using 2 Channel Fabric DMA Demo Guide (current demo): This demo shows the high throughput data transfers between PCIe and large SRAM (LSRAM).

The high-speed serial interface (SERDESIF) available in the SmartFusion2 or IGLOO2 devices provides a fully hardened PCIe endpoint implementation and is compliant to the PCIe Base Specification Revision 2.0, 1.1 and 1.0. For more information, refer to the *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide*.

This demo demonstrates the performance of the PCIe and DDR controller of the SmartFusion2 and IGLOO2 device families. For a tutorial design on how to develop and use the PCIe endpoint including the tools flow and simulation, see the *TU0456: SmartFusion2 SoC FPGA PCIe Control Plane Demo Tutorial*.

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Advanced Development Kit: 12 V adapter PCI Edge Card Ribbon Cable	Rev B or later
IGLOO2 Evaluation Kit: FlashPro4 programmer 12 V adapter USB A to Mini-B cable	Rev C or later
Host PC (or Laptop) with 8GB RAM and PCIe 2.0 Gen1 or Gen2 compliant slot.	Any 64-bit Windows Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	v11.7
FlashPro programming software	v11.7
PCIe_Demo Application	13.6 or later

Notes:

- For SmartFusion2 Kit, PCIe with x4 or higher is required. For IGLOO2 Kit, PCIe with x1 or higher is required.
- PCI Express card slot and PCIe Express card adapter (for Laptop only).
- PCIe Express card adapter is not supplied with the IGLOO2 Evaluation Kit.

2.2 Demo Design

The demo design files are available for download from the following path in the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_dg0517_pcie_fabric_dma_liberov11p7_df*

The demo design files include:

- Drivers_64bitOS
- GUI
- Libero Project
- Programming files
- Readme.txt file

Figure 1 on page 8 shows the top-level structure of the design files. For further details, see the `readme.txt` file.

Figure 1 • **Demo Design Files Top Level Structure**

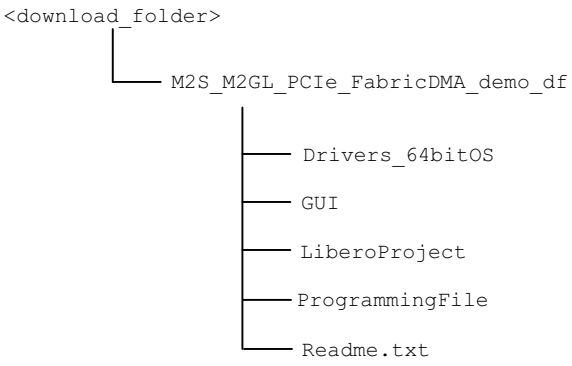


Figure 2 on page 9 describes the demo design. The PCIe core in the SmartFusion2 or IGLOO2 devices supports both the AXI and AMBA high-performance bus (AHB) master and slave interfaces. This demo design uses the AXI master and slave interfaces to achieve maximum bandwidth. The PCIe_Demo application on the host PC initiates the DMA transfers and the embedded PCIe core in the SmartFusion2 or IGLOO2 device initiates the AXI transactions through the AXI master interface to the DMA controller in the FPGA fabric. The DMA controller has two independent channels that share the AXI read/write channels of the PCIe AXI slave interface and the MDDR AXI slave interface. The DMA controller in the FPGA fabric initiates the DMA channels depending on the type of the DMA transfer. Each channel has a timer for calculating the throughput and has 4 KB of LSRAM buffer.

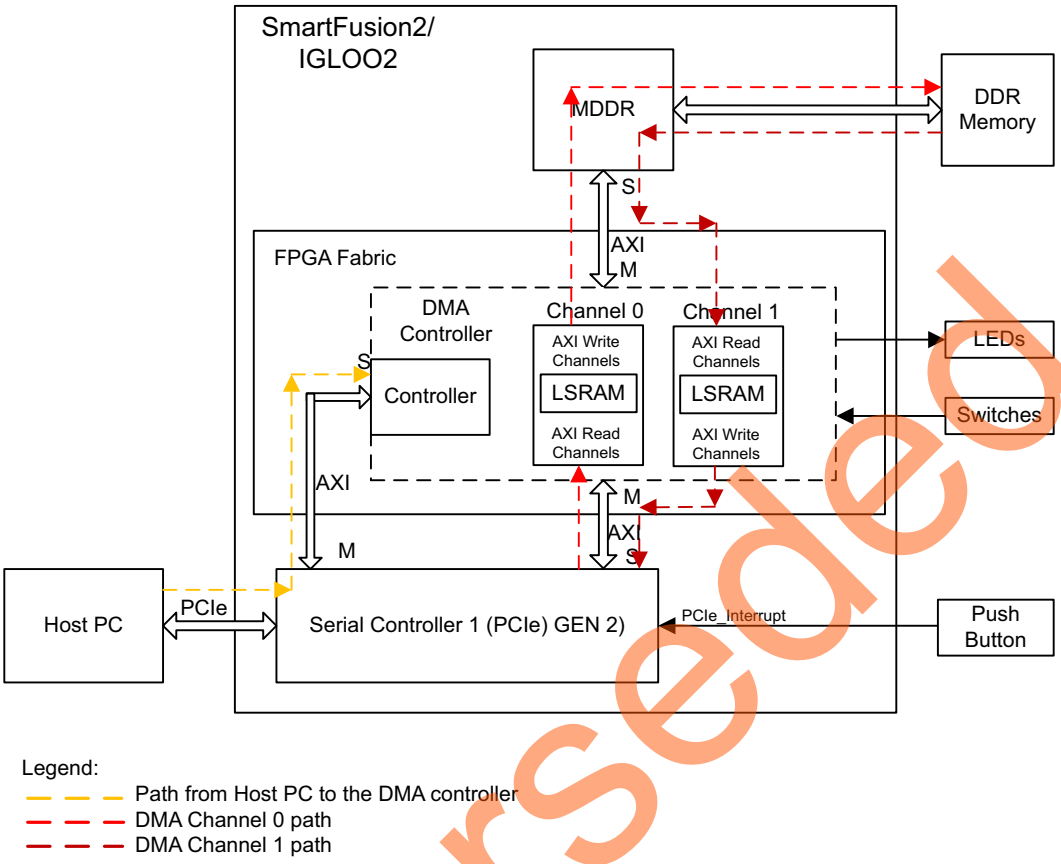
DMA channel 0 handles the following DMA transfers:

- Host PC memory to LSRAM
- Host PC memory to DDR memory
- LSRAM to DDR memory

DMA channel 1 handles the following DMA transfers:

- LSRAM to host PC memory
- DDR memory to host PC memory
- DDR memory to LSRAM

Figure 2 • **PCIe Data Plane Demo Block Diagram**



For SmartFusion2 Advanced Development Kit, MDDR is configured for accessing DDR3 memory in x32 mode. The MDDR clock is configured to 310 MHz (620 Mbps DDR) with a 155 MHz DDR_FIC clock for an aggregate memory bandwidth of nearly 2480 MBps. The PCIe AXI interface clock, ARM® Cortex®-M3 clock, PCIe AXI interface clock, and fabric DMA controller clocks are configured to 155 MHz.

For IGLOO2 Evaluation Kit, MDDR is configured for accessing LPDDR memory in x16 mode. The MDDR clock is configured to 155 MHz (310 Mbps DDR) with a 155 MHz DDR_FIC clock for an aggregate memory bandwidth of nearly 620 MBps. The PCIe AXI interface clock and fabric DMA controller clocks are configured to 155 MHz.

2.2.1 Demo Design Features

- DMA data transfers between the host PC memory and the LSRAM
- DMA data transfers between the host PC memory and the DDR memory
- DMA data transfers between the DDR memory and the LSRAM
- Throughput for every DMA data transfer
- Enables continuous DMA transfers for observing throughput variations
- Displays the PCIe link enable/disable, negotiated link width, and the link speed on the PCIe_Demo application
- Displays the position of DIP switches on the SmartFusion2 Advanced Development Kit or IGLOO2 Evaluation Kit on the PCIe_Demo application
- Displays the PCIe Configuration Space on the PCIe_Demo application
- Controls LEDs on the board according to the command from the PCIe_Demo application
- Enables read and write operations to scratchpad register in the FPGA fabric
- Interrupts the host PC, when the Push button is pressed. The PCIe_Demo application displays the count value of the number of interrupts sent from the board.

2.2.2 Demo Design Description

There are six different types of data transfers supported by this demo design. The following sections describe the process of each data transfer:

- "Host PC Memory to LSRAM (Read)"
- "LSRAM to Host PC Memory (Write)"
- "Host PC Memory to DDR Memory (Read)"
- "DDR Memory to Host PC Memory (Write)"
- "LSRAM to DDR Memory (Write)"
- "DDR Memory to LSRAM (Read)"

2.2.2.1 Host PC Memory to LSRAM (Read)

Data transfer from PC memory to the LSRAM occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address, and size (4 KB).
2. Fabric DMA controller initiates a 16 beat AXI burst (that is, 128 bytes) read transaction to the PCIe AXI slave interface.
3. The PCIe core sends the memory read (MRd) transaction layer packets (TLP) to the host PC.
4. The host PC returns a completion (CplD) TLP to the PCIe link.
5. This returned data completes the AXI read initiated by the fabric DMA controller.
6. This data is stored in the LSRAM.
7. The fabric DMA controller repeats this process until the 4 KB of data transfer is completed.
8. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.2.2.2 LSRAM to Host PC Memory (Write)

Data transfer from the LSRAM to PC memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. Fabric DMA controller reads the LSRAM data and initiates an AXI 16 beat burst write transaction to PCIe AXI slave interface.
3. The PCIe core sends a memory write (MWr) TLP to the host PC.
4. The fabric DMA controller repeats this process until the 4 KB size of data transfer is completed.
5. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.2.2.3 Host PC Memory to DDR Memory (Read)

Data transfer from the PC memory to the DDR memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. Fabric DMA controller initiates 16 beat AXI burst (that is, 128 bytes) read transaction to the PCIe AXI interface.
3. The PCIe core sends a memory read (MRd) transaction layer packets (TLP) to the host PC.
4. The host PC returns a completion data (CplD) TLP to the PCIe link.
5. This returned data completes the AXI read initiated by the fabric DMA controller.
6. This data is stored in the dual port LSRAM.
7. The LSRAM data is written to the DDR controller through the AXI interface as an AXI 16 beat burst write transaction. The reads from the host PC memory and the writes to the DDR memory occur independent of each other for achieving high throughput. Empty flags are generated in the fabric DMA controller to avoid reading unknown data from the LSRAM.
8. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
9. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.2.2.4 DDR Memory to Host PC Memory (Write)

Data transfer from the DDR memory to the PC memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. The fabric DMA controller initiates a 16 beat burst (that is, 128 bytes) AXI read transaction from the DDR through the MDDR controller.
3. The data is stored in the dual port LSRAM.
4. The LSRAM data is written to the PCIe core as an AXI 16 beat burst write transaction. The reads from the DDR memory and writes to the host PC memory occur independent of each other for achieving high throughput. Empty flags are generated in the fabric DMA controller to avoid reading unknown data from the LSRAM.
5. The PCIe core sends a memory write (MWr) TLP to the host PC.
6. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
7. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application.

2.2.2.5 LSRAM to DDR Memory (Write)

Data transfer from the LSRAM to the DDR memory occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. The LSRAM data is written to the DDR controller through AXI interface as an AXI 16 beat burst write transaction.
3. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
4. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application for display.

2.2.2.6 DDR Memory to LSRAM (Read)

Data transfer from the DDR memory to the LSRAM occurs in the following sequence:

1. PCIe_Demo application sets up the fabric DMA controller through the PCIe link. This includes DMA direction, address and size (4 KB).
2. The fabric DMA controller initiates a 16 beat burst AXI read transaction of the DDR through the MDDR controller.
3. The data is stored in the dual port LSRAM.
4. The fabric DMA controller repeats this process until 4 KB of data transfer is completed.
5. The fabric DMA controller provides the DMA completion status and the number of clock cycles consumed to complete the DMA transaction to the PCIe_Demo application for display.

2.3 Throughput Calculation

This demo implements a timer to measure the throughput of DMA transfers. The throughput measured includes all of the overhead of the AXI, PCIe, and DMA controller transactions. The procedure for measuring throughput is:

1. Setup the DMA controller for the complete transfer.
2. Start a timer and the DMA controller.
3. Initiate data transfer for the requested number of bytes.
4. Wait till DMA transfer is completed.
5. Record the number of clock cycles consumed for steps 2-4.

To arrive at a realistic system performance, the throughput calculation takes into account all the overheads during a transfer. The throughput formula is as shown below:

Throughput = Transfer Size (Bytes) / (Number of clock cycles taken for a transfer * Clock Period)

EQ 1

2.4 Setting Up the Demo Design

2.4.1 Jumper Settings for SmartFusion2 Advanced Development Kit

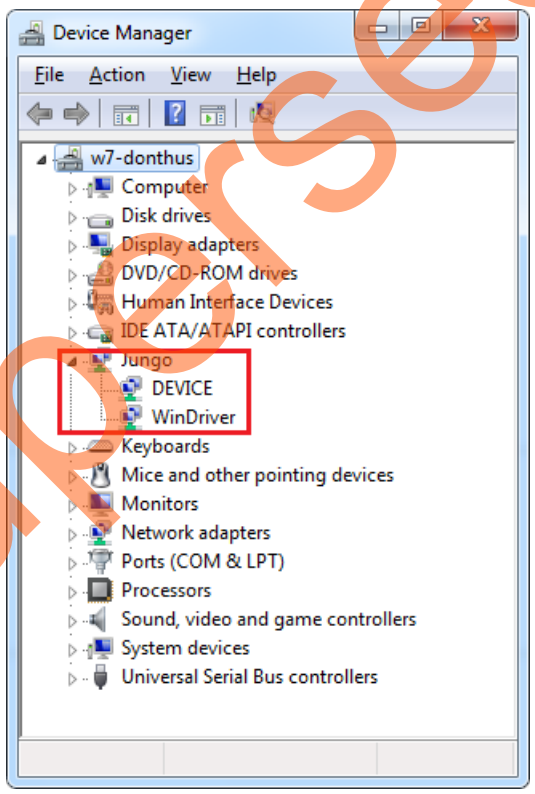
1. Connect the jumpers on the SmartFusion2 Advanced Development Kit, as shown in Table 2. **CAUTION**: While making the jumper connections, the power supply switch **SW7** must be switched OFF.

Table 2 • **SmartFusion2 FPGA Advanced Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J116, J353, J354, J54	1	2	These are the default jumper settings of the Advanced Development Kit board. Make sure these jumpers are set accordingly.
J123	2	3	
J124, J121, J32	1	2	JTAG programming via FTDI

2. Connect the host PC to the J33 Connector using the USB A to mini-B cable. The USB to UART bridge drivers are automatically detected. Verify, if the detection is made in the device manager as shown in Figure 3.

Figure 3 • **Device Manager**



3. Connect the power supply to the J18 connector. Switch ON the power supply switch **SW7**.

2.4.2 Jumper Settings for IGLOO2 Evaluation Kit

1. Connect the jumpers on the IGLOO2 Evaluation Kit as shown in Table 3.
   CAUTION: While making the jumper connections, the power supply switch **SW7** must be switched OFF.

Table 3 • **IGLOO2 FPGA Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

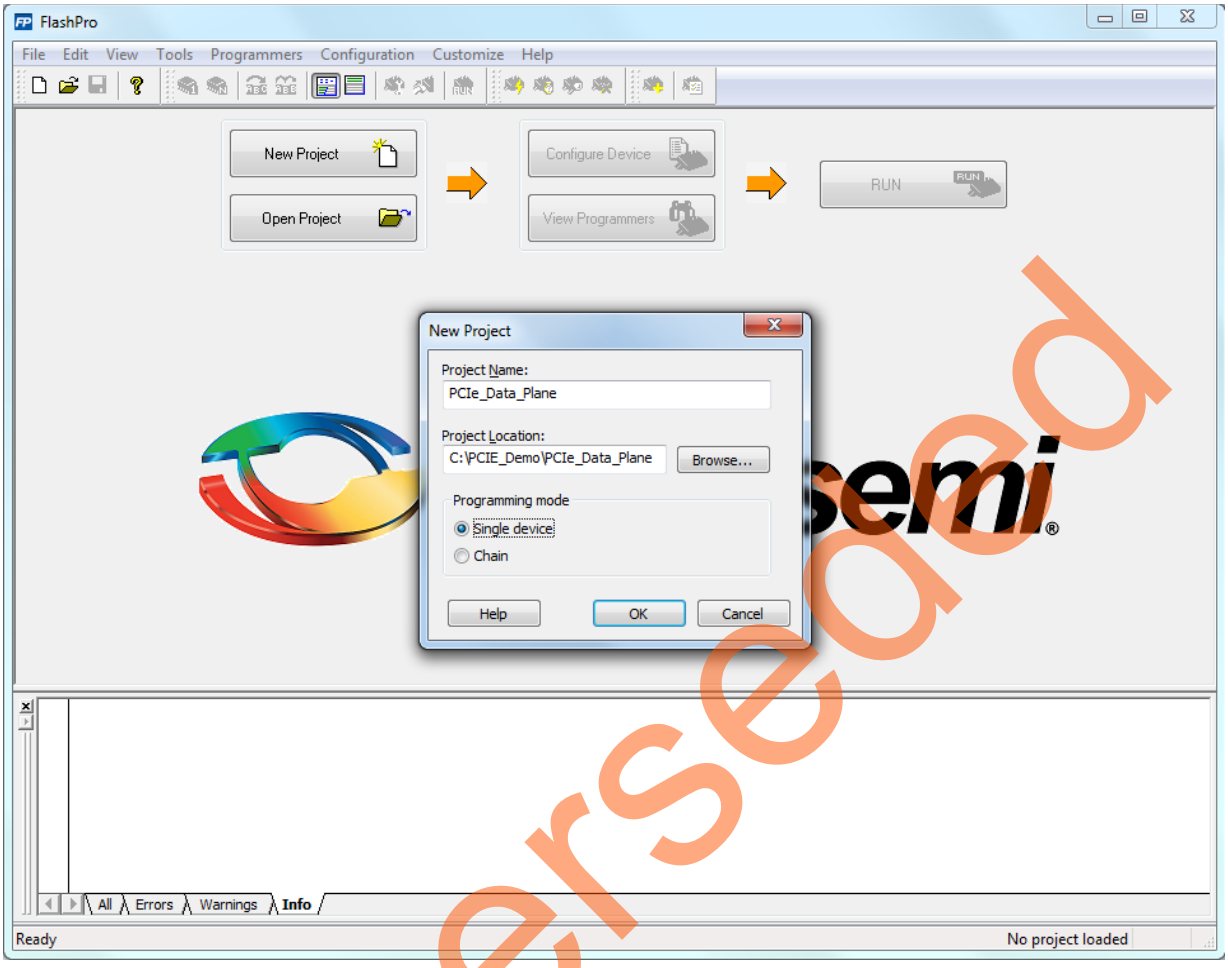
2. Connect the FlashPro4 programmer to the J5 connector of the IGLOO2 Evaluation Kit.
3. Connect the power supply to the J6 connector. Switch ON the power supply switch **SW7**.

2.4.3 Programming the Device

Download the demo design from:
http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_dg0517_pcie_fabric_dma_liberov11p7_df

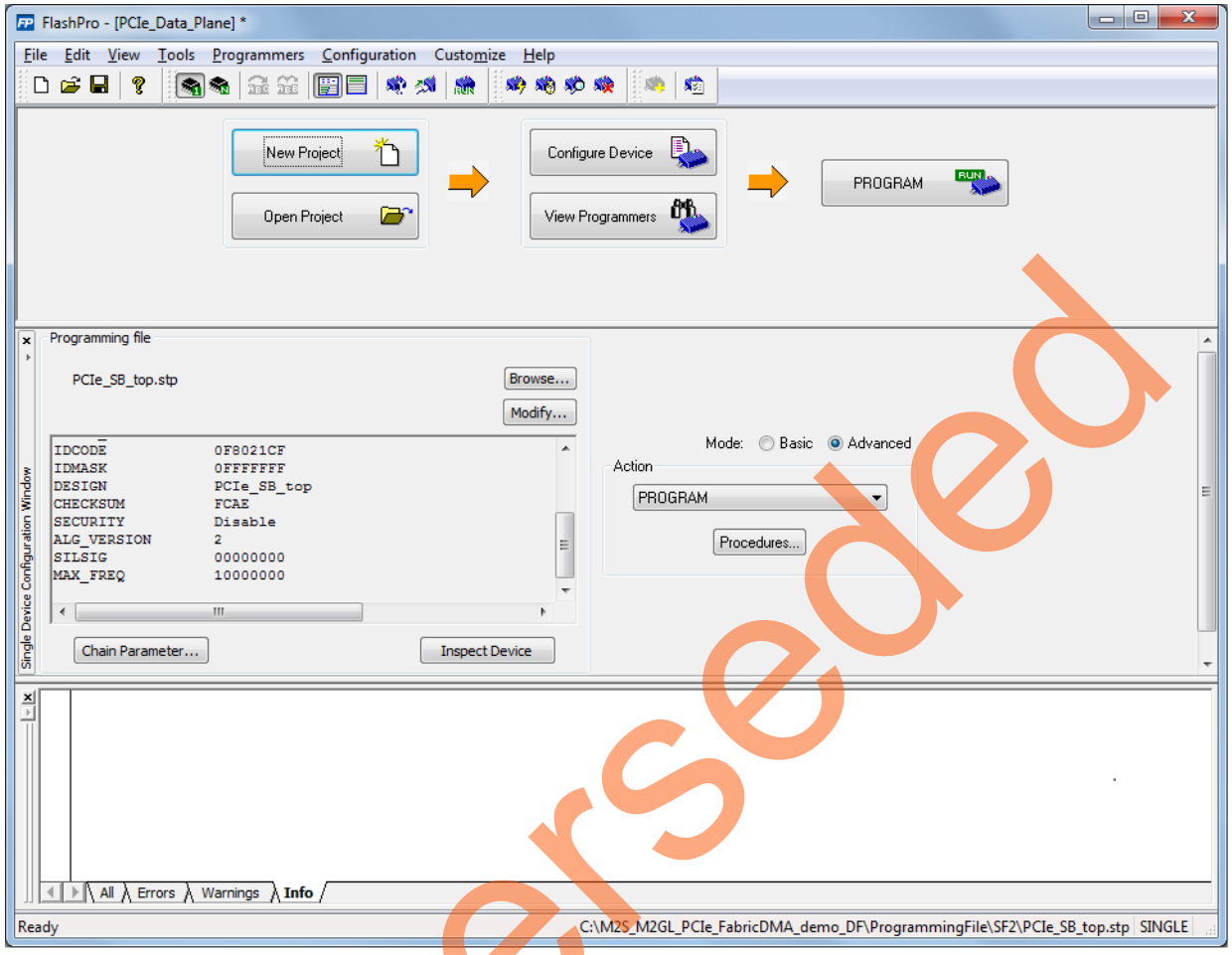
1. Launch the FlashPro software.
2. Click **New Project**.
3. In the **New Project** window, type the project name.

Figure 4 • **FlashPro New Project**



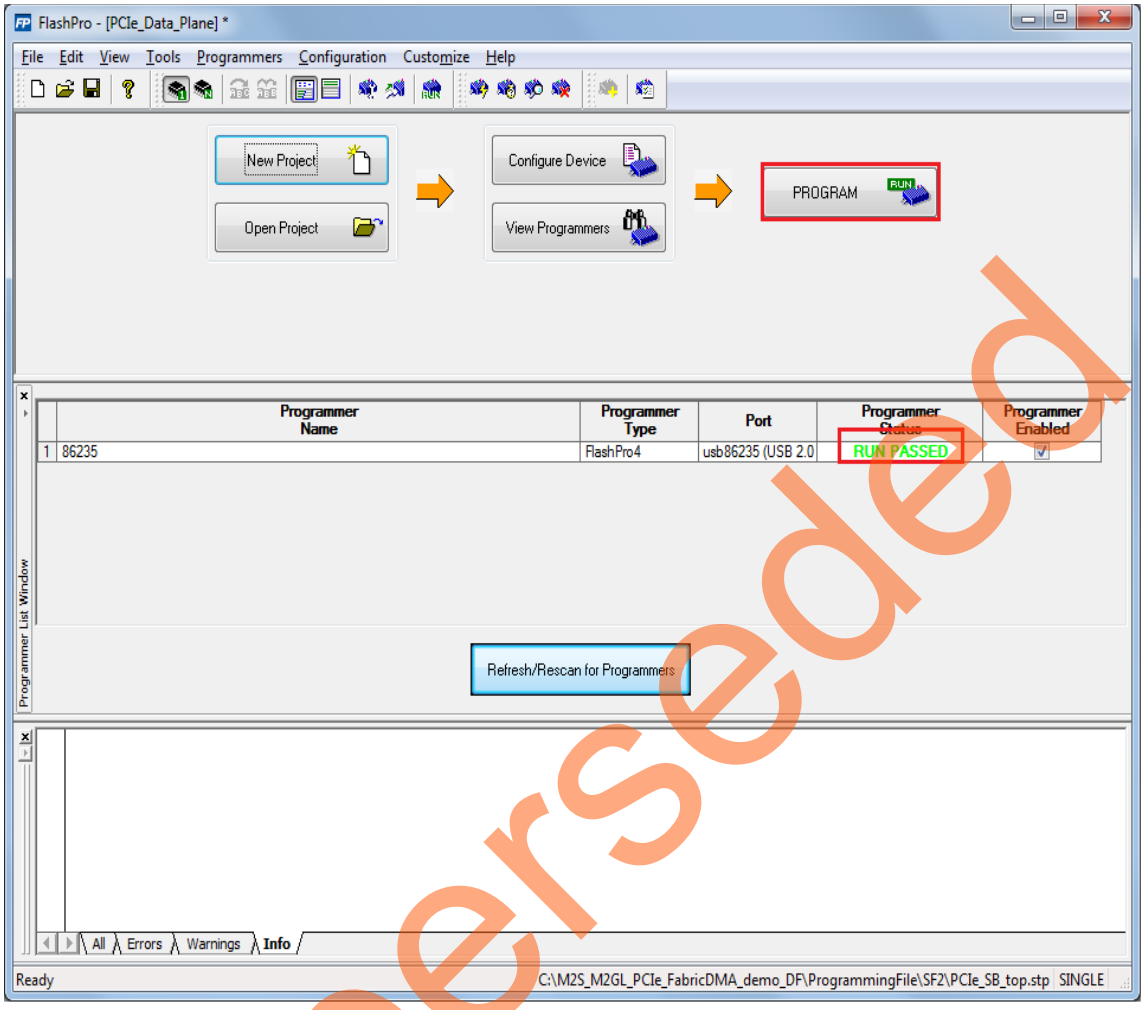
4. Click **Browse** and navigate to the location where you want to save the project.
5. Select **Single device** as the **Programming mode**.
6. Click **OK** to save the project.
7. Click **Configure Device**.
8. Click **Browse** and navigate to the location where the `PCIe_SB_top.stp` file is located and select the file. The default location is:
   SmartFusion2: *<download_folder>\M2S_M2GL_PCIe_FabricDMA_demo_DF\Programming-File\SF2*
   IGLOO2: *<download_folder>\M2S_M2GL_PCIe_FabricDMA_demo_DF\ProgrammingFile\IGL2*
9. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

Figure 5 • **FlashPro Project Configured**



10. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the program passed.

Figure 6 • **FlashPro Programming Passed**



2.4.4 Connecting the Kit to Host PC PCIe Slot

1. After successful programming, switch OFF the SmartFusion2 Advanced Development Kit or the IGLOO2 Evaluation Kit and shut down the host PC.
2. This demo is designed to run in any PCIe Gen 2 compliant slot. If the host PC does not support Gen 2 compliant slot the demo switches to Gen 1 mode. Connect the CON1 - PCIe Edge connector of the SmartFusion2 Advanced Development Kit to the host PC's PCIe slot through the PCI Edge card ribbon cable.

   OR,

   Connect the CON1 - PCIe Edge connector of the IGLOO2 Evaluation Kit to the PCIe slot of the host PC or connect the CON1-PCIe Edge connector to the laptop PCIe slot using the Express card adapter. If using a laptop, the Express card adapters support only Gen 1 and the demo works in Gen 1 mode.

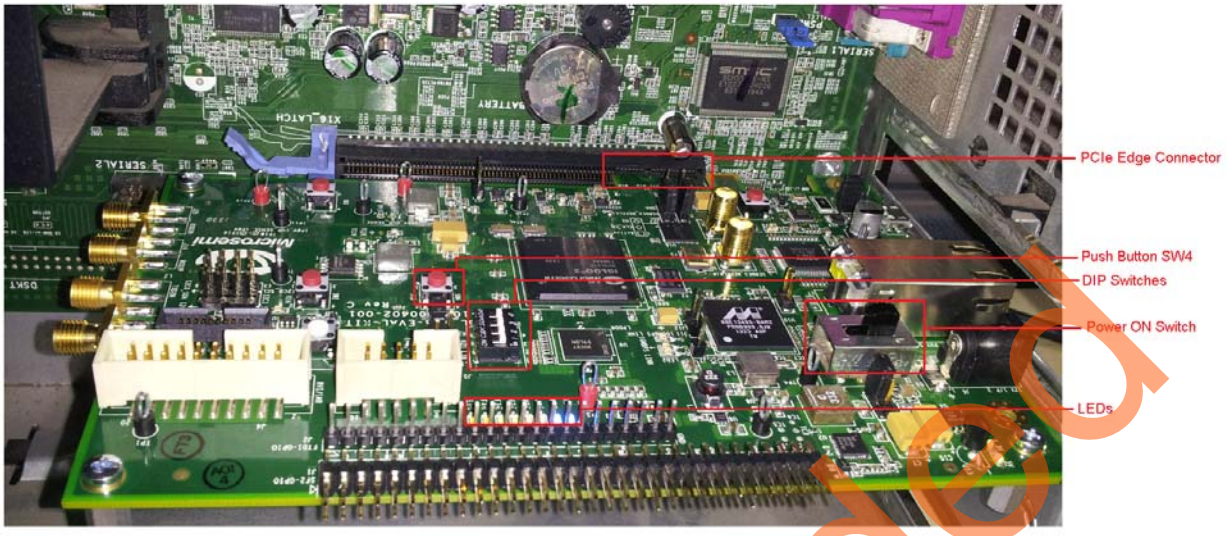
CAUTION: Power OFF the host PC (or laptop) while inserting the PCIe Edge connector. If it is not powered OFF, the PCIe device detection and the selection of Gen1 or Gen2 mode may not occur properly. The device detection and selection are dependent on the host PC (or laptop) PCIe configuration.

3. Figure 7 on page 17 shows the board setup for the host PC in which SmartFusion2 Advanced Development Kit is connected to the host PC PCIe slot.

Figure 7 • **SmartFusion2 Advanced Development Kit Setup for Host PC**

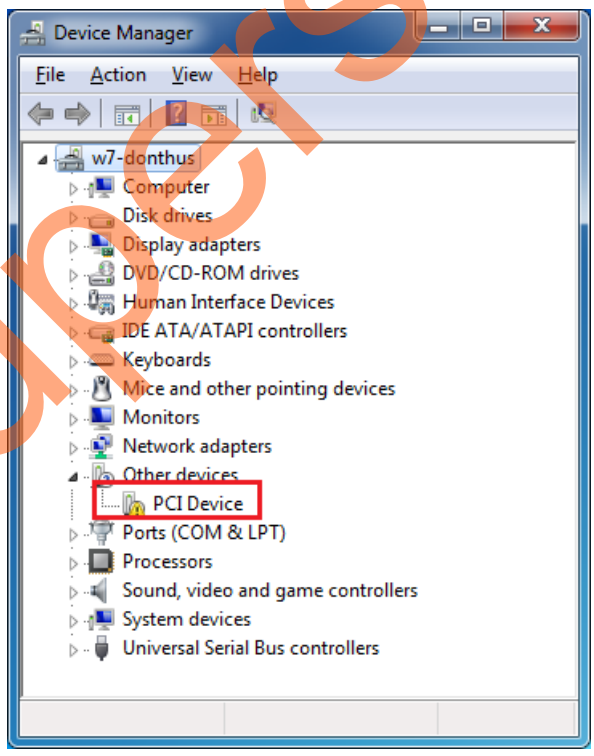
Figure 8 on page 18 shows the board setup for the host PC in which the IGLOO2 Evaluation Kit is connected to the host PC PCIe slot. To connect the IGLOO2 Evaluation Kit to the laptop using the Express card adapter, see "Appendix: IGLOO2 Evaluation Kit Board Setup for Laptop".

Figure 8 • **IGLOO2 Evaluation Kit Setup**



4. Switch ON the power supply switch **SW7**.
5. Switch ON the host PC and check the **Device Manager of the Host PC** for **PCIe Device**. Figure 9 shows the example **Device Manager** window. If the device is not detected, power cycle the SmartFusion2 Advanced Development Kit or the IGLOO2 Evaluation Kit and click **scan for hardware changes** option in the **Device Manager**.

Figure 9 • **Device Manager - PCIe Device Detection**



Note: If the device is still not detected, check whether or not the BIOS version in the host PC is latest, and if PCI is enabled in the host PC BIOS.

2.4.5 Drivers Installation

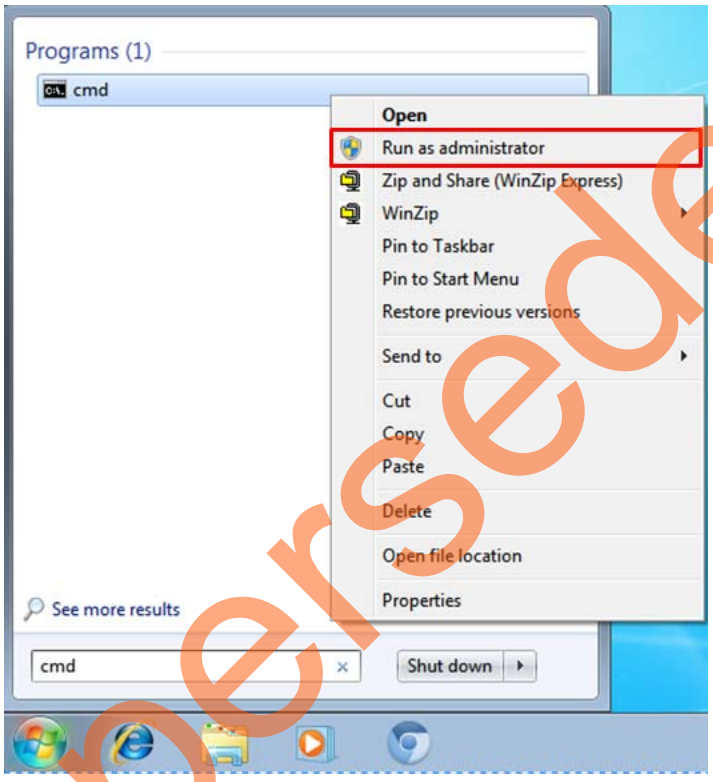
The PCIe Demo uses a driver framework provided by Jungo WinDriverPro. The following steps describe how to install the PCIe drivers on the host PC:

1. Extract the `PCIe_Demo.rar` to C:\ drive. The `PCIe_Demo.rar` is located at: *<Download Folder>\M2S_M2GL_PCIe_FabricDMA_demo_DF\Drivers_64bitOS\ PCIe_Demo.rar*

Note: Installing these drivers requires the host PC administration rights.

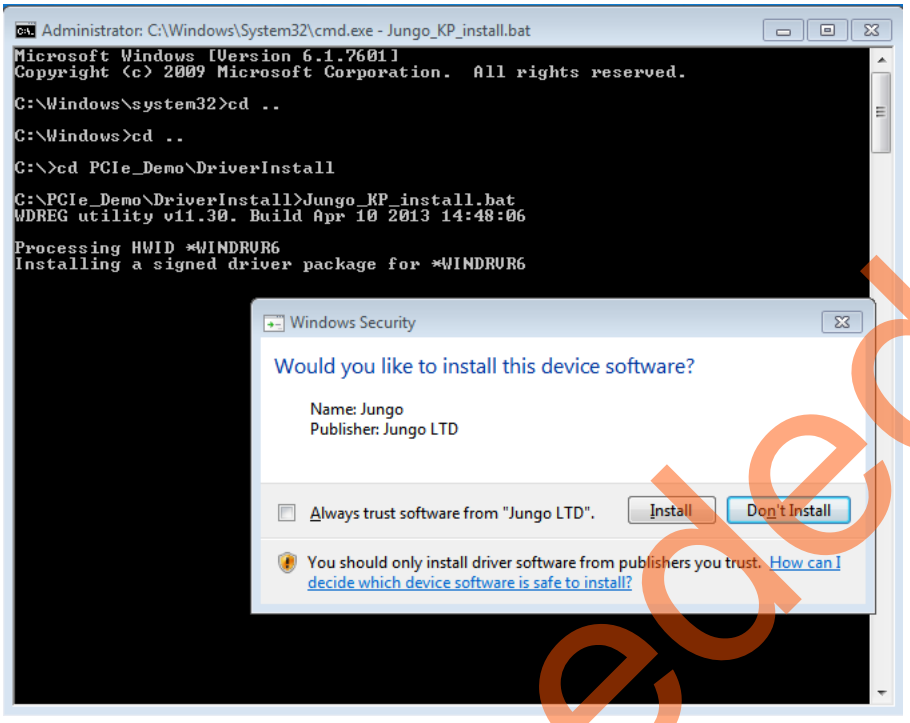
2. Open the command prompt as an administrator.

Figure 10 • **Opening Command Prompt as Administrator**



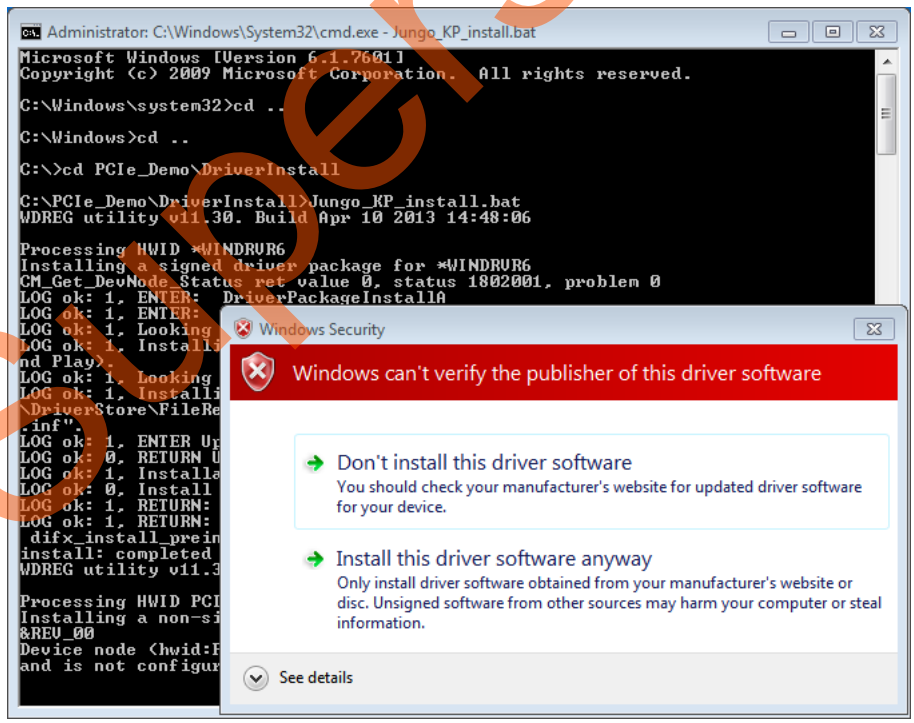
3. Navigate to *C:\PCIe_Demo\DriverInstall* and run the batch file `Jungo_KP_install.bat`.
4. In the **Windows Security** dialog box, click **Install**.

Figure 11 • **Installing Jungo Driver**



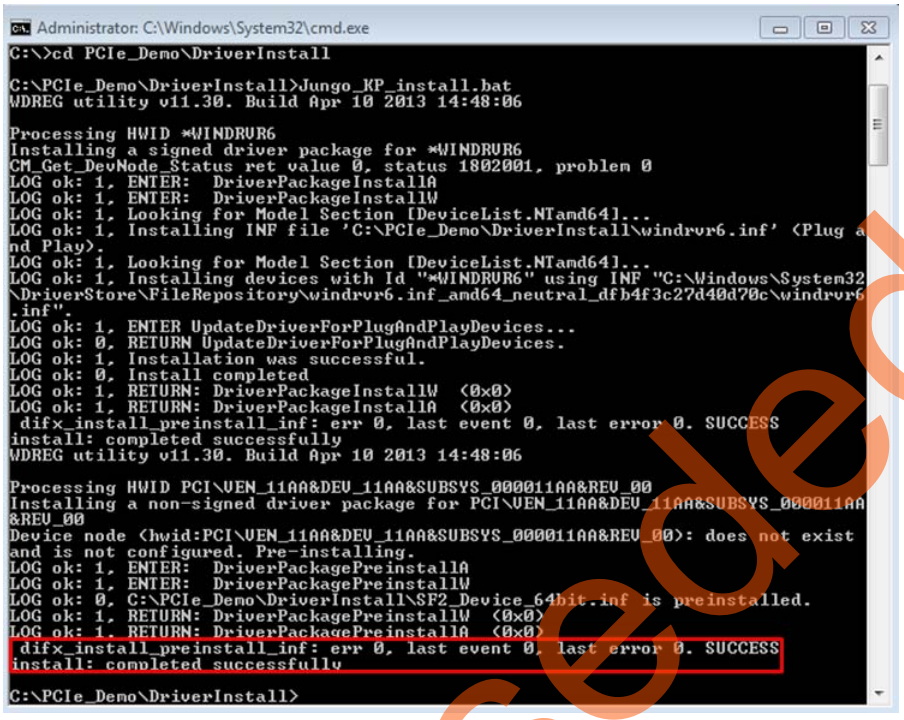
5. When prompted, click **Install this driver software anyway**.

Figure 12 • **Windows Security Dialog**



After the installation is complete, the **completed successfully** message is displayed.

Figure 13 • **Installation Complete Message**

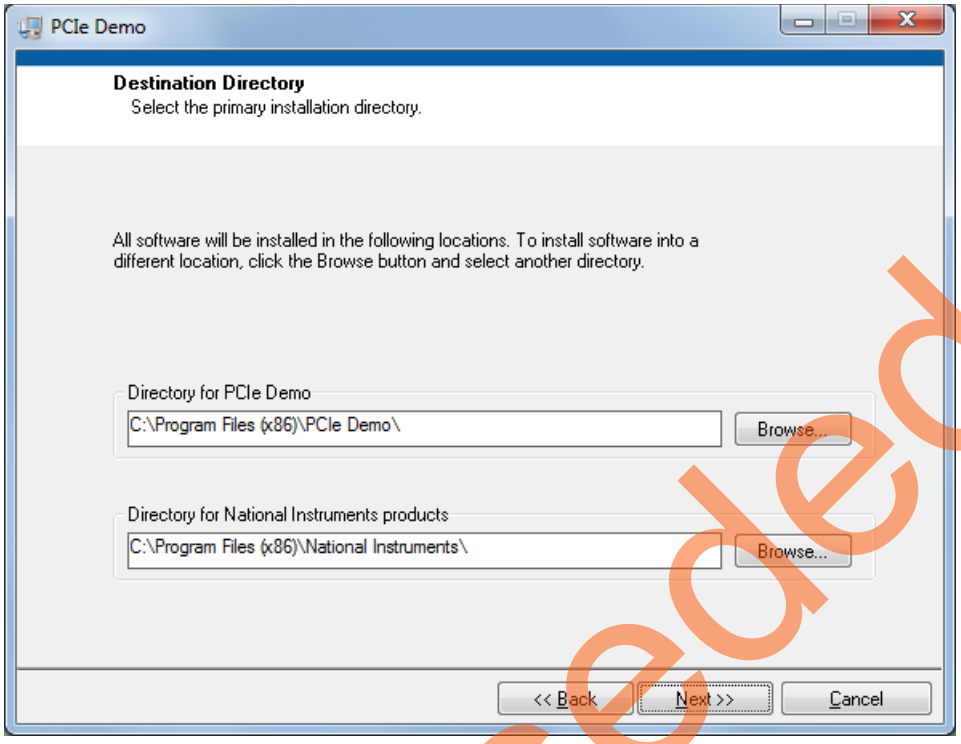


2.4.6 PCIe_Demo Application

The PCIe_Demo application is a simple graphic user interface that runs on the host PC to communicate with the SmartFusion2 or IGLOO2 PCIe endpoint device. It provides PCIe link status, driver information and demo controls. The PCIe_Demo application invokes the PCIe driver installed on the host PC and provides commands to the driver according to the selection made. To install the PCIe_Demo application:

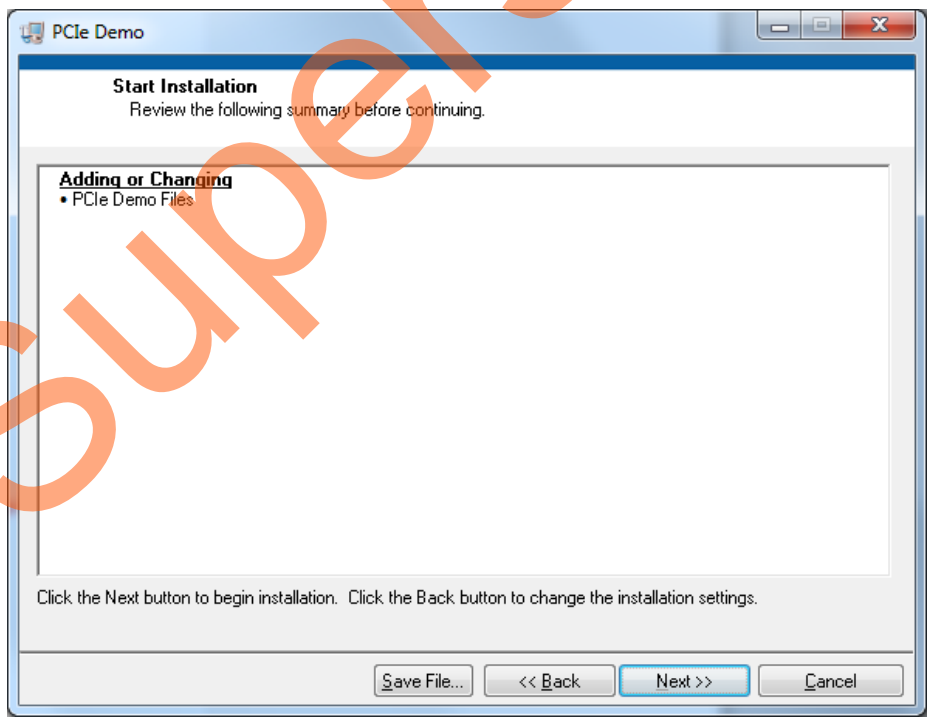
1. Download the PCIe demo GUI installer from *http://soc.microsemi.com/download/rsc/?f=PCIe_Demo_GUI_Installer*
2. Extract the **PCIe_Demo_GUI_Installer.rar**.
3. Double-click the **setup.exe** in the provided GUI installation (PCIe_Demo_GUI_Installer\setup.exe). Apply default options as shown in Figure 14.

Figure 14 • **Installing PCIe_Demo Application**



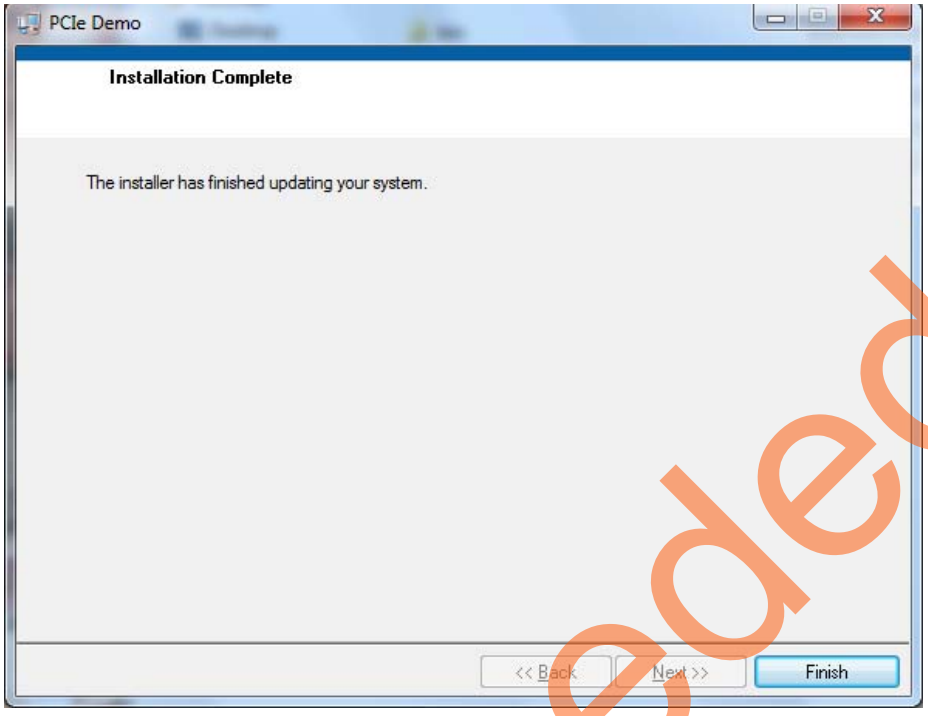
4. To start the installation, click **Next**.

Figure 15 • **PCIe_Demo Application Installation Steps**



5. Click **Finish** to complete the installation.

Figure 16 • **Successful Installation of PCIe_Demo Application**

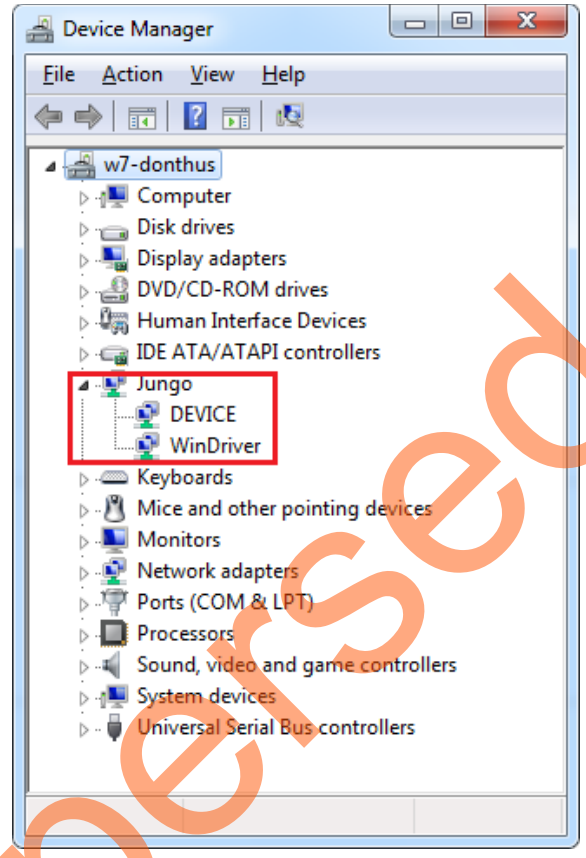


6. Shut down the host PC.
7. Power cycle the SmartFusion2 Advanced Development Kit.
8. Restart the host PC.

2.5 Running the Design

1. Check the host PC **Device Manager** for the drivers. Figure 17 shows an example Device Manager window highlighting the Jungo drivers installed. If the device is not detected, power cycle the SmartFusion2 Advanced Development Kit or the IGLOO2 Evaluation Kit and click **scan for hardware changes** in **Device Manager**.

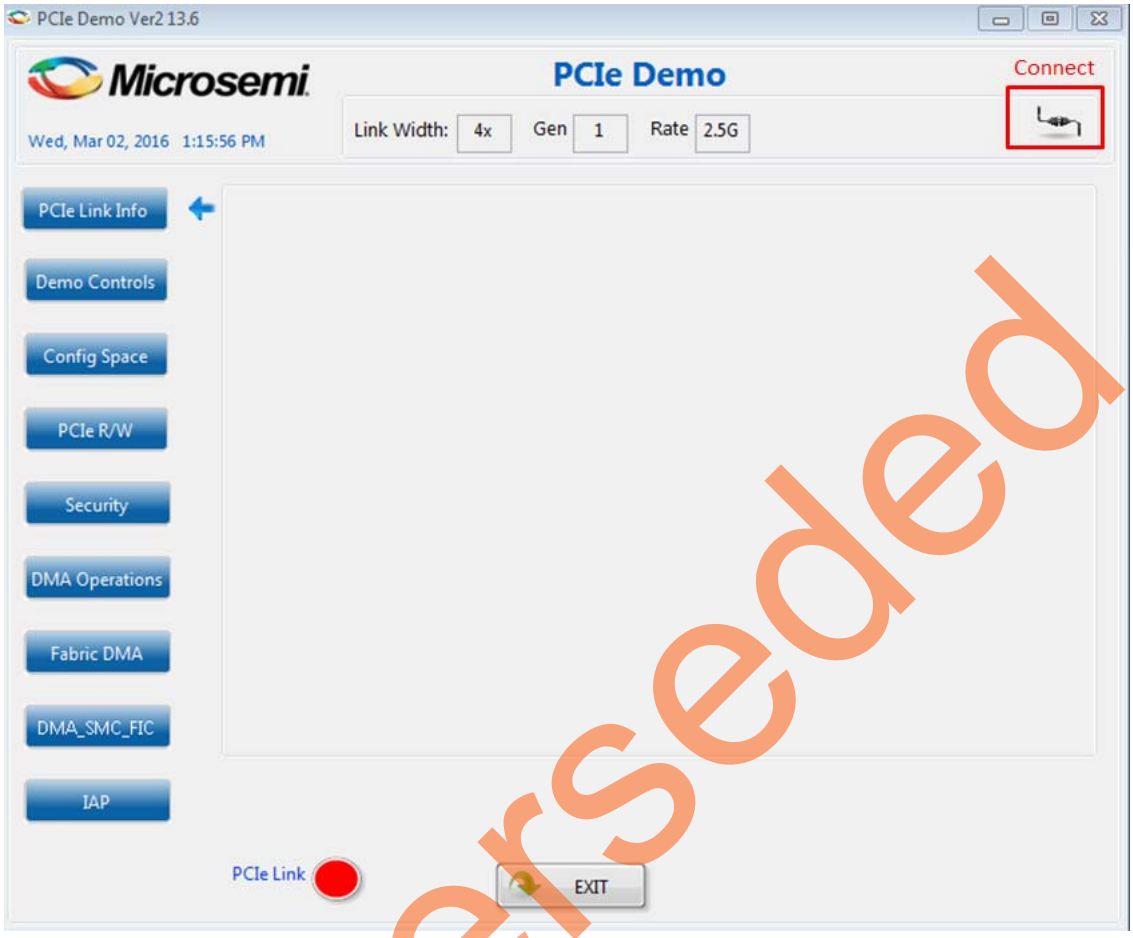
Figure 17 • **Device Manager - PCIe Device Detection**



Note: If a warning appears on **DEVICE** or **WinDriver** in the Device Manager, uninstall the drivers and repeat the installation.

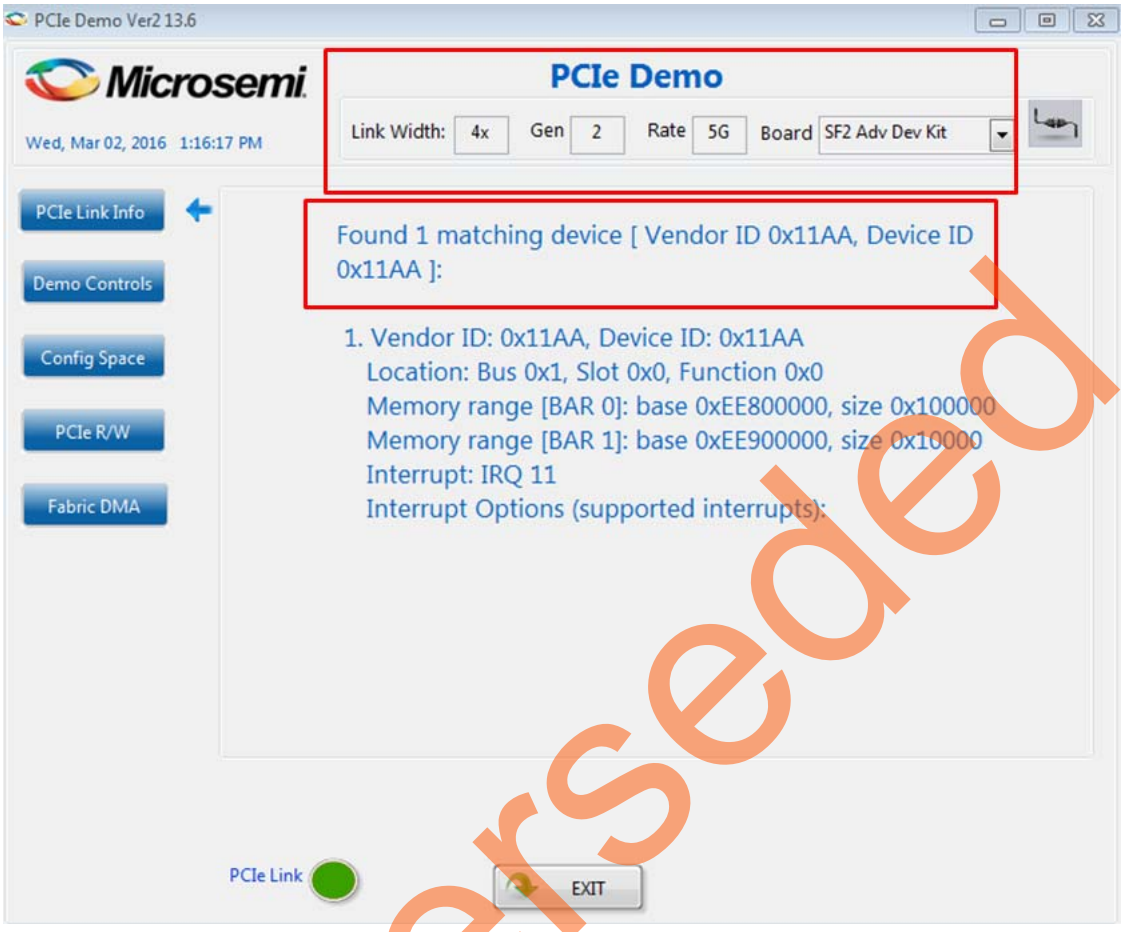
2. Invoke the PCIe_Demo application from **ALL Programs > PCIe Demo > PCIe Demo GUI**. Figure 18 on page 25 shows the PCIe_Demo launch window.

Figure 18 • **PCIe_Demo Application**



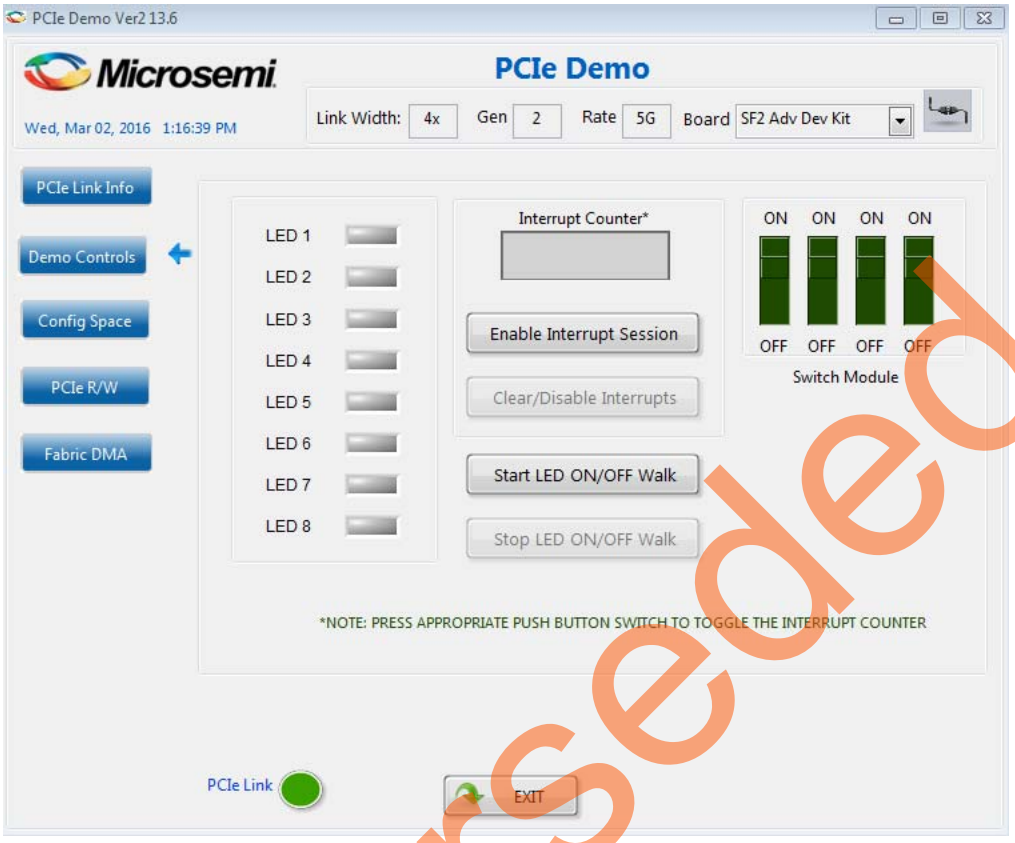
3. Click **Connect** at the top right corner of the PCIe_Demo application window. The application detects and displays the connected kit, demo design, and PCIe link. Figure 19 on page 26 shows the example messages after the connection is established.

Figure 19 • **PCIe Device Information**



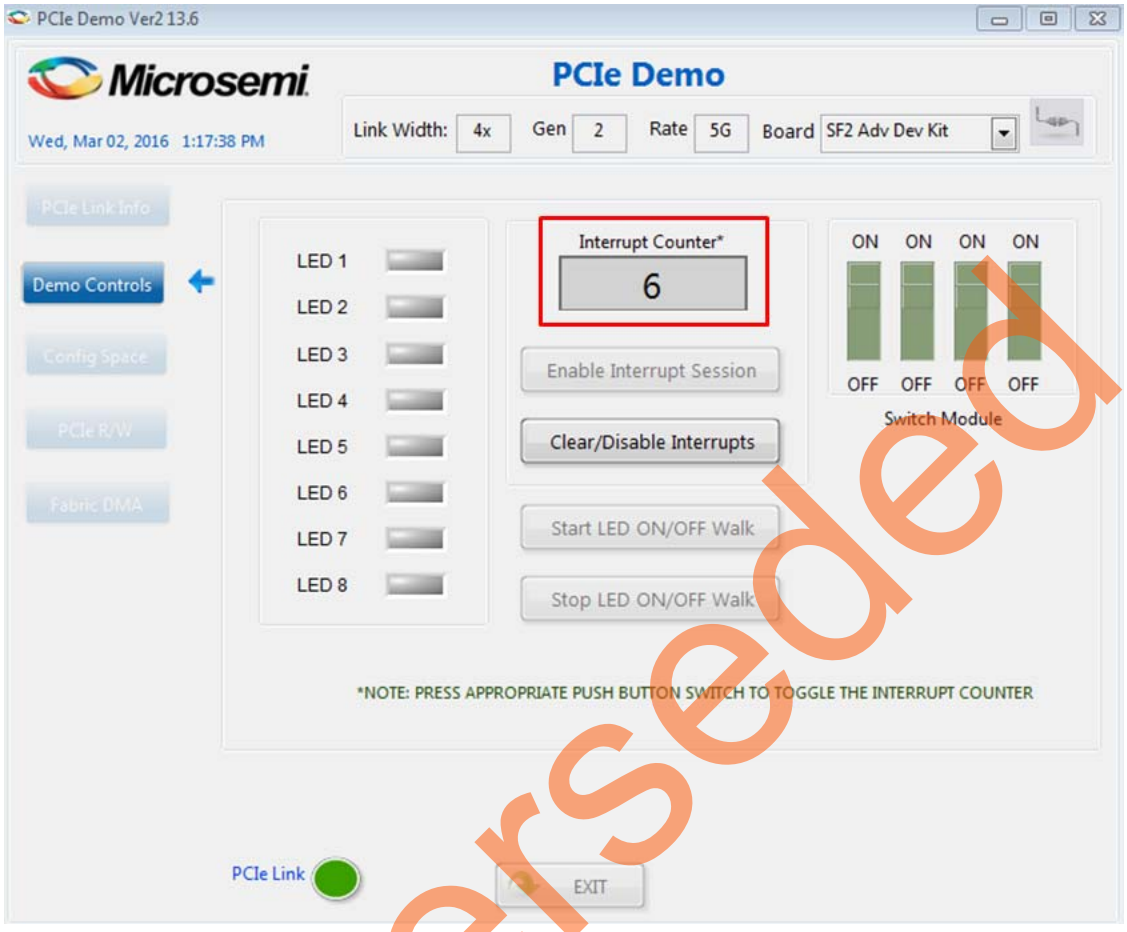
4. Click **Demo Controls** to display the LED options and the DIP switch positions as shown in Figure 20 on page 27.

Figure 20 • **Demo Controls**



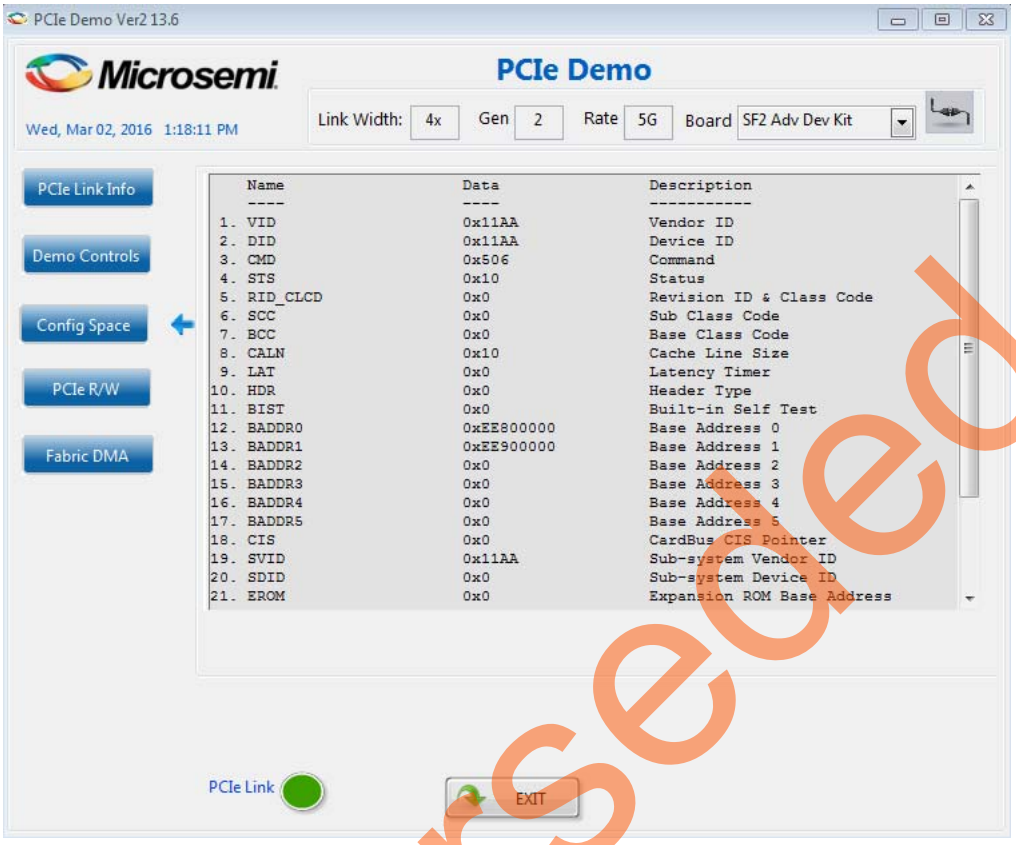
5. Click LED buttons to switch ON or OFF the LEDs on the board.
6. Click **Start LED ON/OFF Walk** to blink the LEDs on the board.
7. Click **Stop LED ON/OFF Walk** to stop the LEDs blinking.
8. Change the DIP switch positions on the board and observe it getting reflected in the switches of the **Switch Module** of the PCIe_Demo application.
9. Click **Enable Interrupt Session** to enable the PCIe interrupt.
10. Press the push button, **SW1** on the SmartFusion2 Advanced Development Kit board or **SW4** on the IGLOO2 Evaluation Kit board. Observe the interrupt count on the **Interrupt Counter** field in PCIe_Demo application as shown in Figure 21 on page 28.

Figure 21 • **PCIe Interrupt**



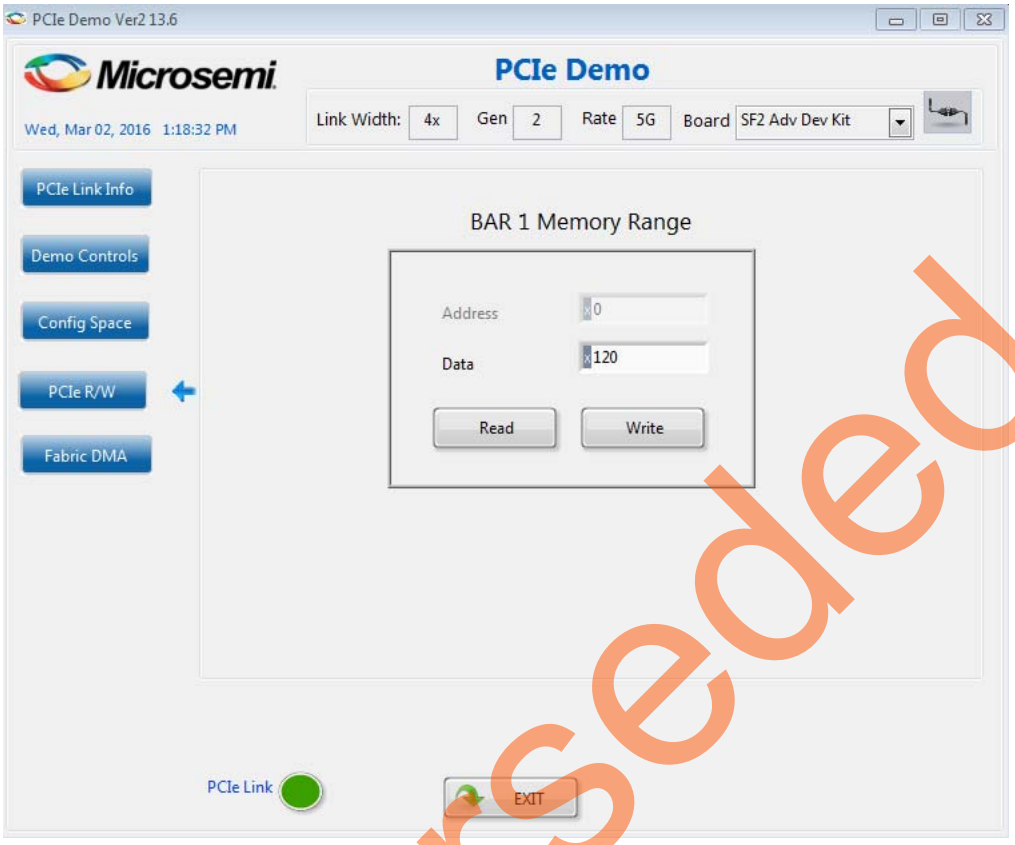
11. Click **Clear/Disable Interrupts** to clear and disable the PCIe interrupts.
12. Click **Config Space** to see the details about the PCIe configuration space. Figure 22 on page 29 shows the PCIe configuration space.

Figure 22 • **PCIe Configuration Space**



13. Click **PCIe R/W** to execute read and writes to a 32-bit scratchpad register through BAR1 space. Figure 23 on page 30 shows the PCIe R/W panel.

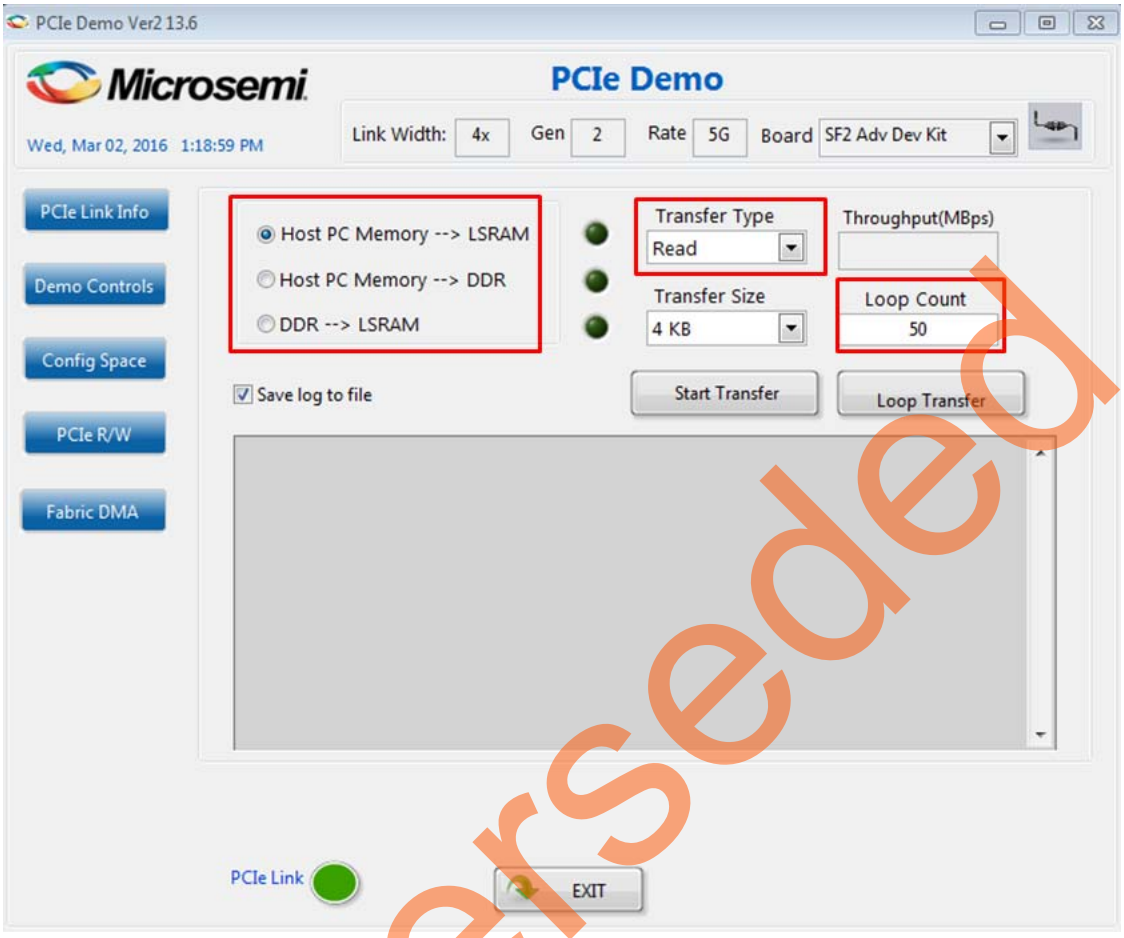
Figure 23 • **Read and Writes to Scratchpad Register**



14. Click **Fabric DMA** to execute the DMA operations. Three types of DMA transactions are possible:
    - Between host PC memory and LSRAM
    - Between host PC memory and DDR3 memory
    - Between LSRAM and DDR3 memory

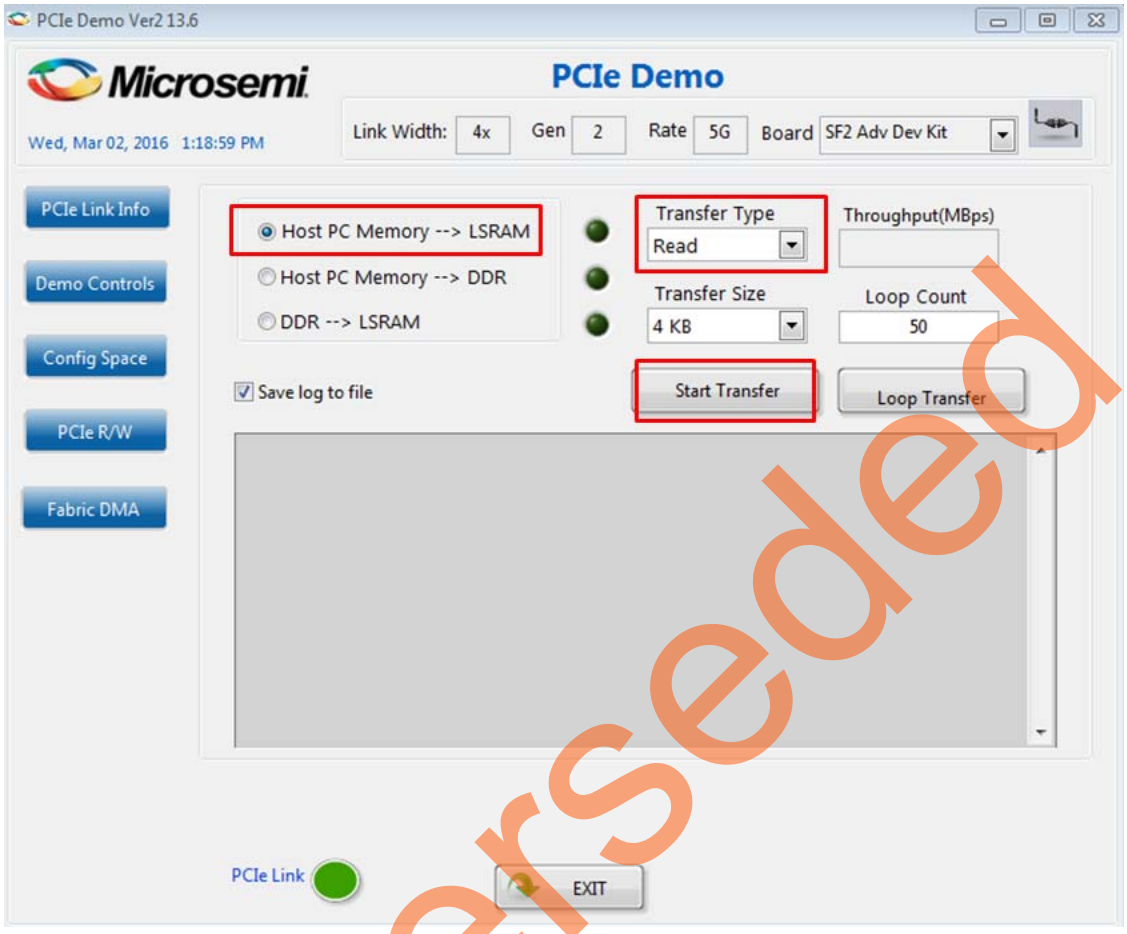
    For each operation, **Transfer Type** can be selected as **Read**, **Write**, or **Read/Write** as shown in Figure 24 on page 31. It also has a **Loop Count** field to execute the DMA operation in loop.

Figure 24 • **Fabric DMA Controls**



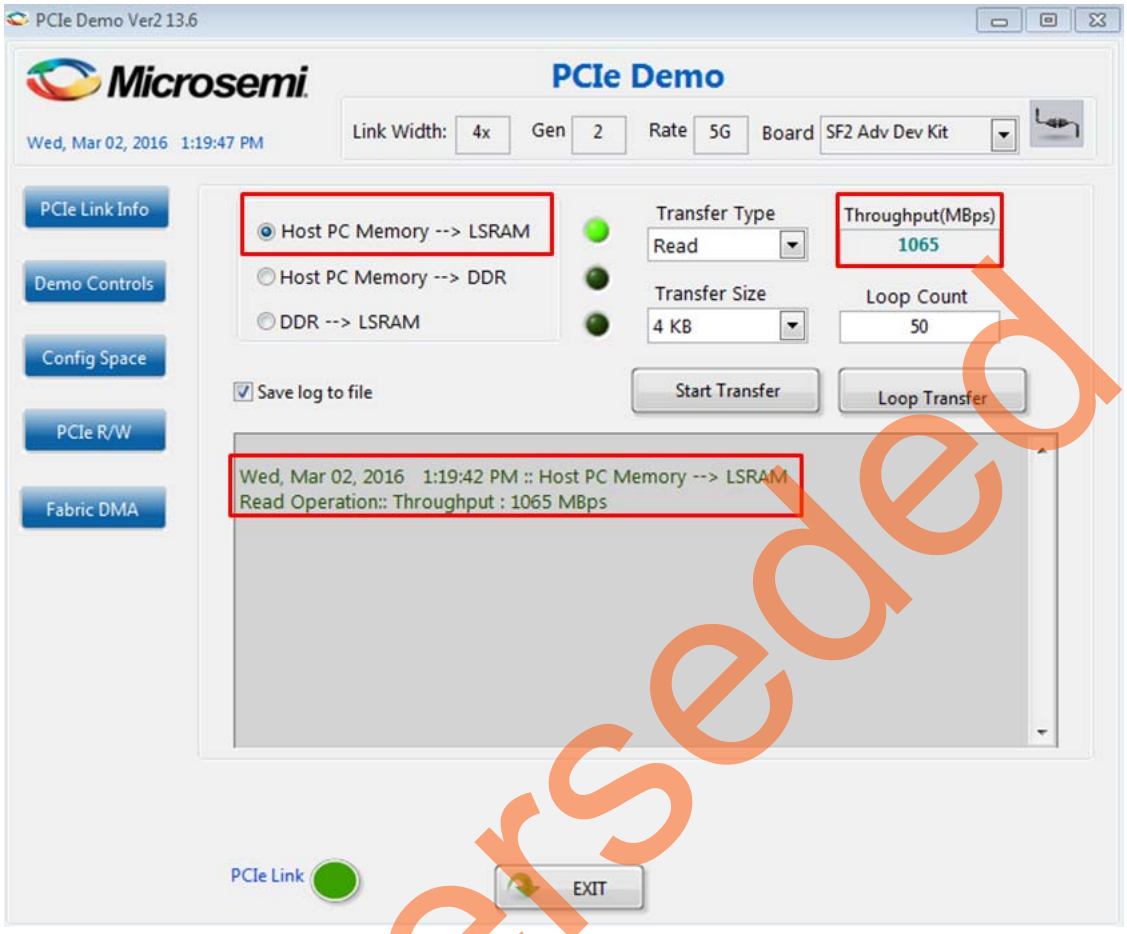
15. Select **Transfer Type** as **Read**, and then select **Host PC Memory - - > LSRAM** to execute the DMA transactions from the host PC to the LSRAM. Click **Start Transfer**. Figure 25 on page 32 shows the fabric DMA panel.

Figure 25 • **DMA Transactions between Host PC Memory and LSRAM**



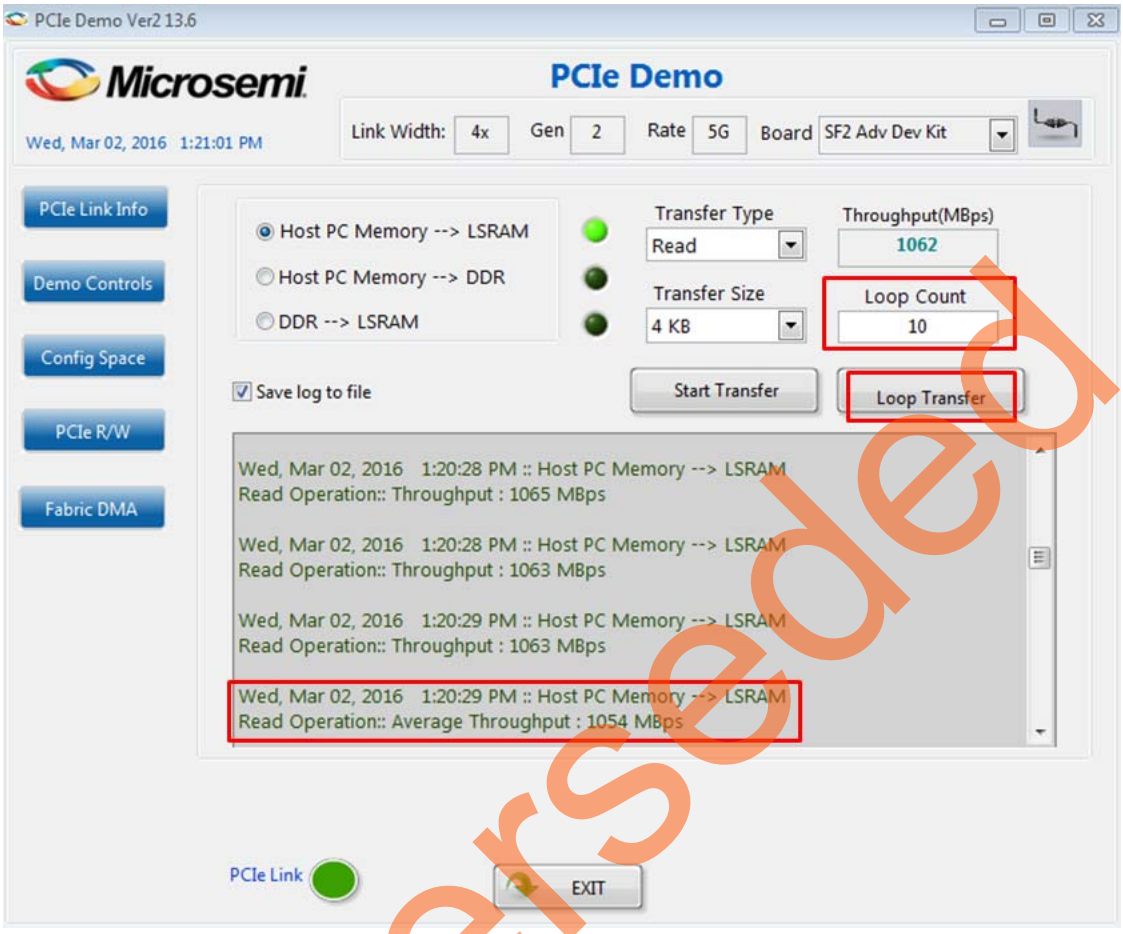
16. After the completion of the data transfer, the throughput is displayed as shown in Figure 26 on page 33.

Figure 26 • **DMA between Host PC Memory and LSRAM**



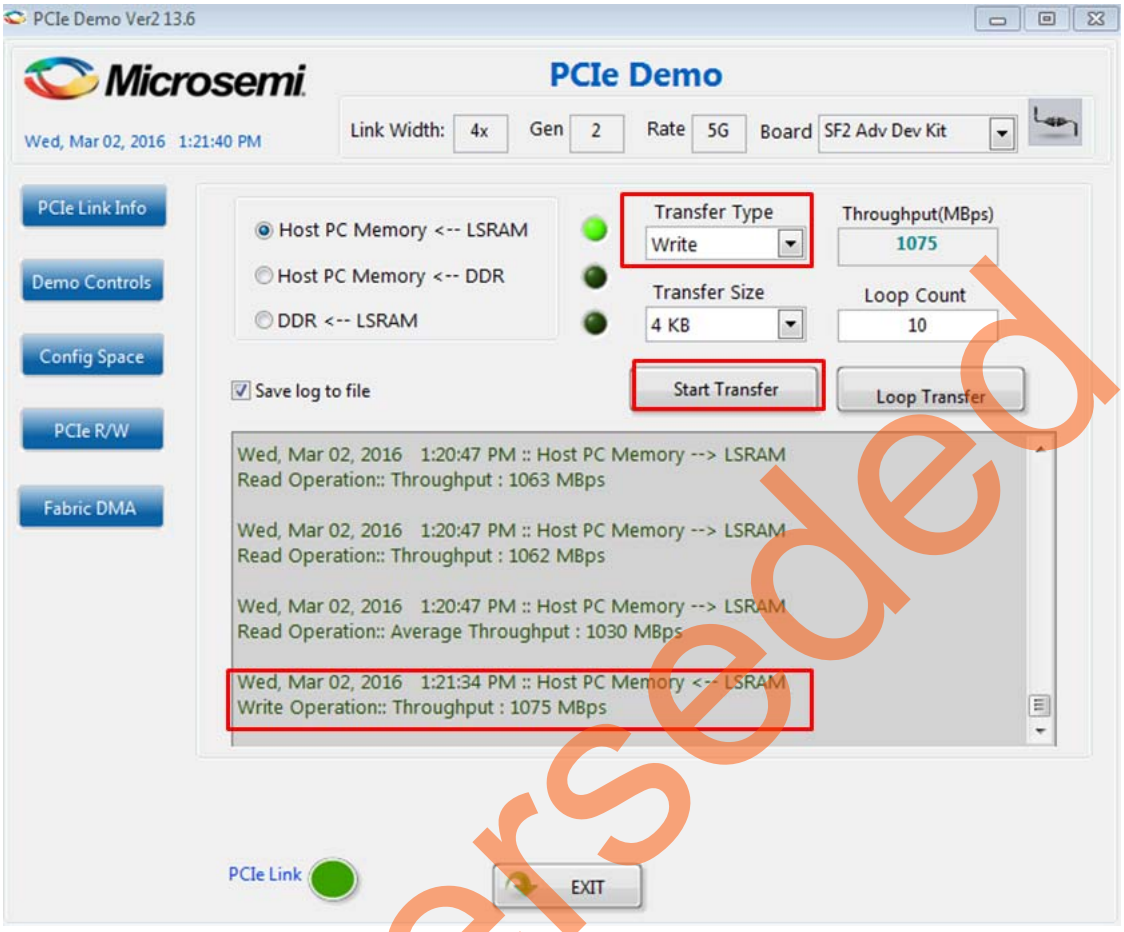
17. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 sequential DMA transactions. After the completion of the data transfer, the PCIE_DEMO application displays the throughputs as shown in Figure 27 on page 34. The average throughput is also logged. The log file is stored in the host PC at *C:\PCIe_Demo\DriverInstall*.

Figure 27 • **DMA between Host PC Memory and LSRAM - Loop Transfer**



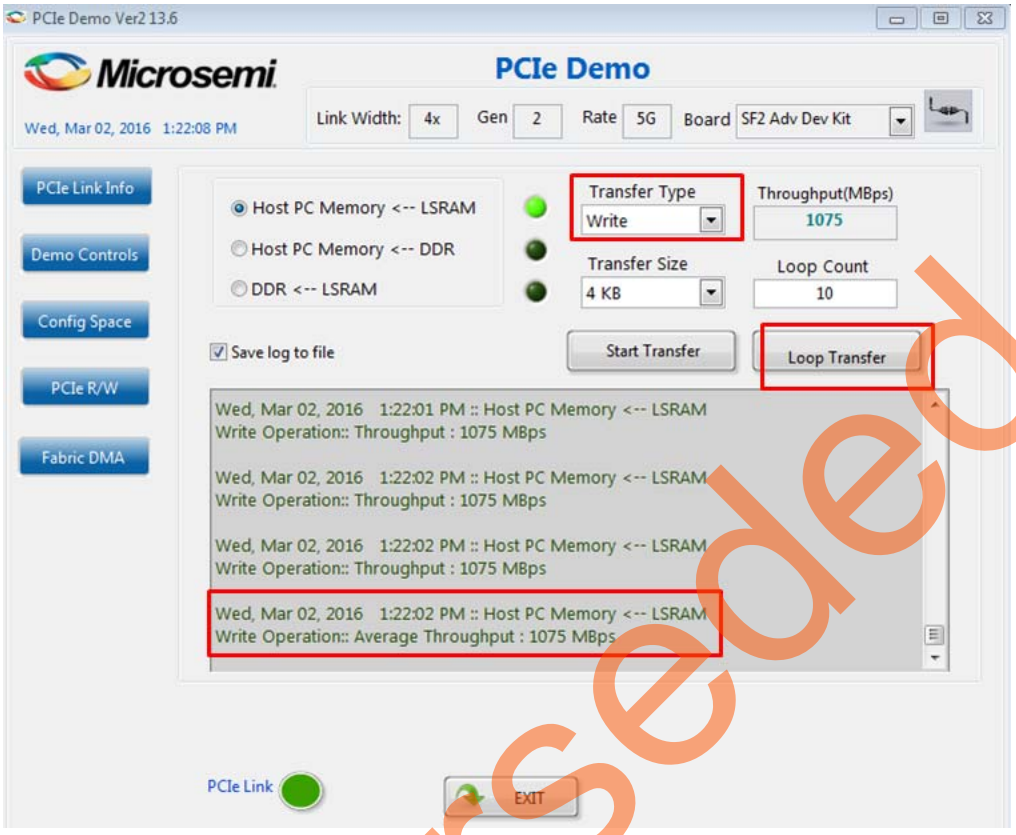
18. Select **Transfer Type** as **Write**, and then select **Host PC Memory < - - LSRAM** to execute the DMA transactions from the LSRAM to the host PC. Click **Start Transfer** to perform a single DMA transaction. After the completion of the data transfer, the throughput is displayed as shown in Figure 28 on page 35.

Figure 28 • **DMA between Host PC Memory and LSRAM**



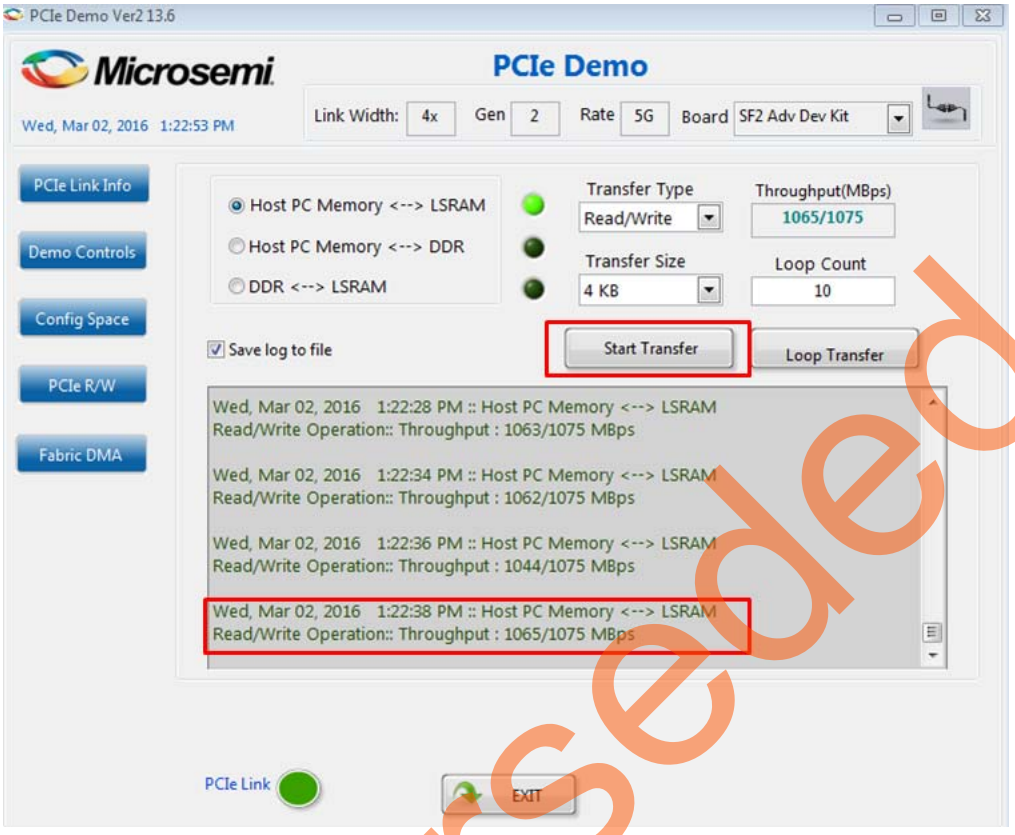
19. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 repeated DMA transactions. After the completion of the data transfer, the throughputs are displayed as shown in Figure 29 on page 36.

Figure 29 • **DMA between Host PC Memory and LSRAM - Loop Transfer**



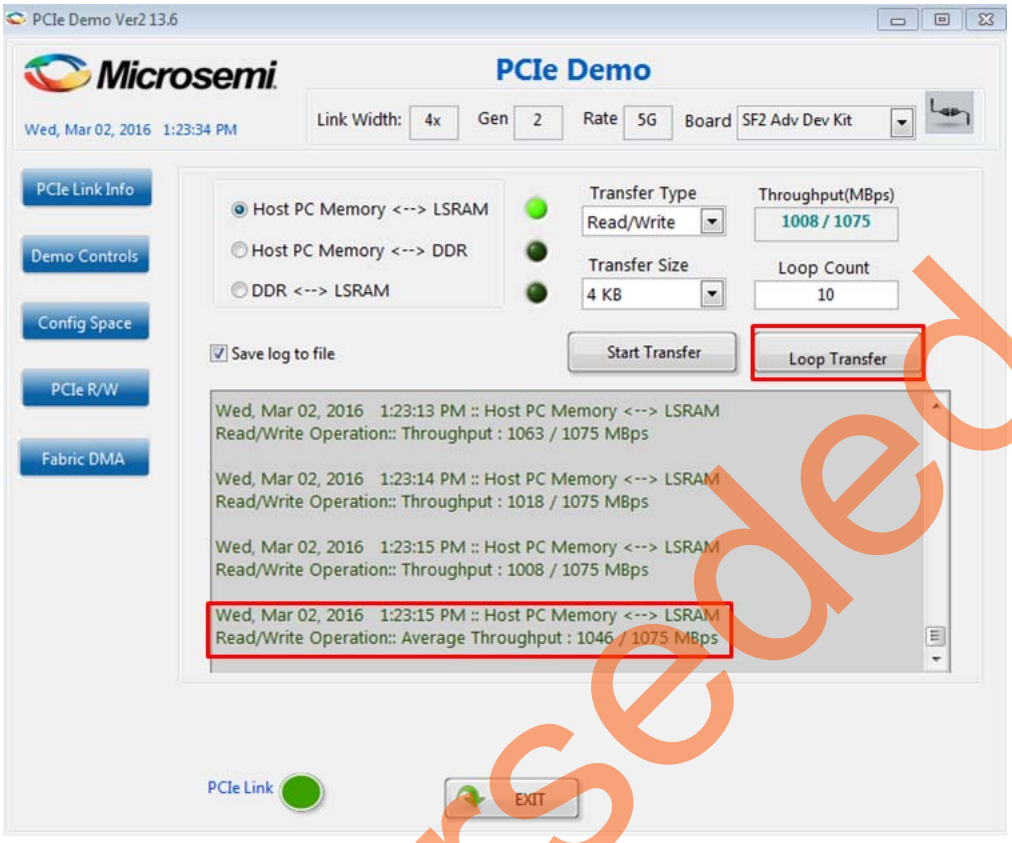
20. Select **Transfer Type** as **Read/Write** to perform simultaneous read and writes. Click **Start Transfer** to perform a single DMA transaction. After the completion of the data transfer, the throughput is displayed as shown in Figure 30 on page 37.

Figure 30 • **DMA between Host PC Memory and LSRAM**



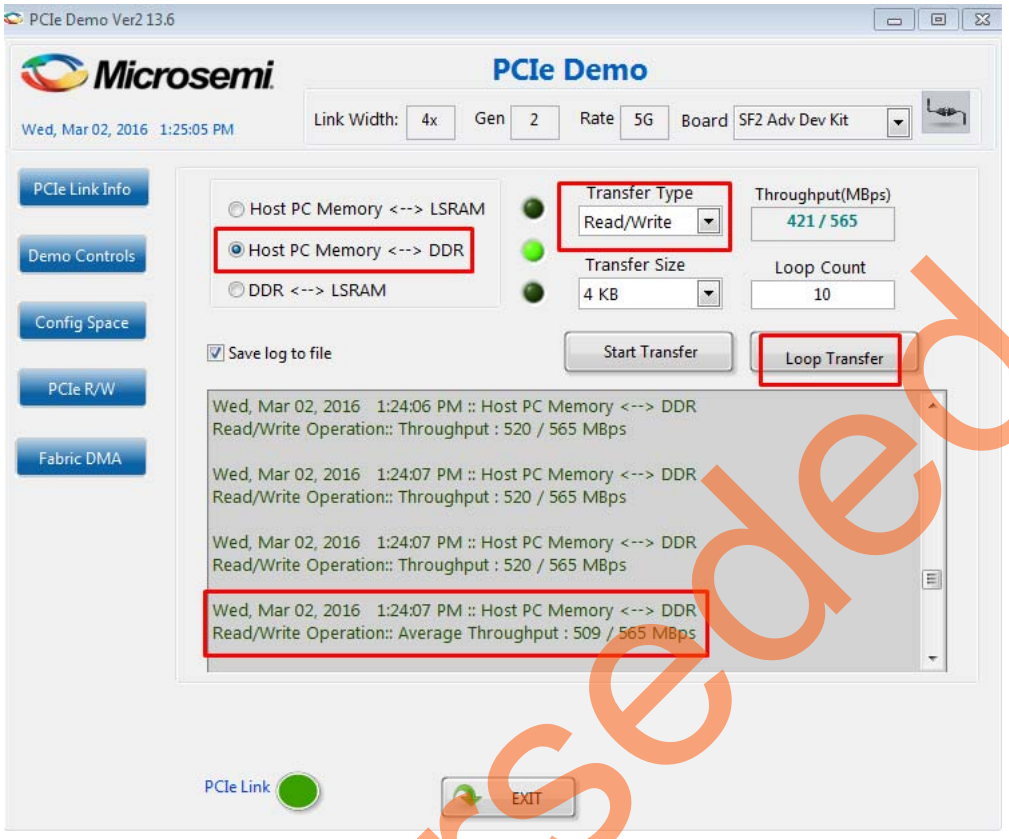
21. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 sequential DMA transactions. After the completion of the data transfer, the throughput is displayed as shown in Figure 31 on page 38.

Figure 31 • **DMA between Host PC Memory and LSRAM**



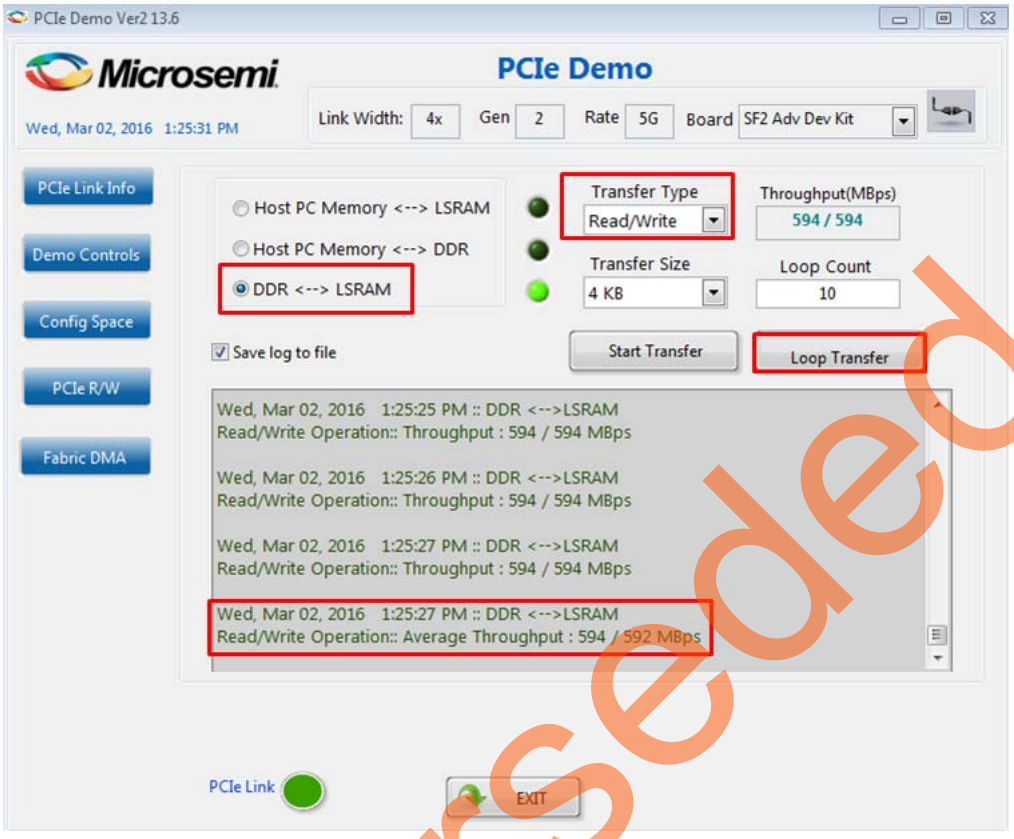
22. Select the type of DMA transfer as host PC memory to DDR3, select **Transfer Type** as **Read/Write** to perform simultaneous read and writes. Click **Loop Transfer** to perform 10 repeated DMA transactions. After the completion of the data transfer, the throughput is displayed as shown in Figure 32 on page 39.
    The **Transfer Type** can be selected as **Read** or **Write** also.

Figure 32 • **DMA between Host PC Memory and DDR**



23. Select the type of DMA transfer as **DDR to LSRAM**. Select **Transfer Type** as **Read/Write** to perform simultaneous read and writes. Click **Loop Transfer** to perform 10 repeated DMA transactions. After the completion of the data transfer, the throughput is displayed as shown in Figure 33 on page 40. The **Transfer Type** can be selected as **Read** or **Write**.

Figure 33 • **DMA between LSRAM and DDR**



24. Click **Exit** to quit the demo.

2.6 Summary

This demo shows how to implement a PCIe data plane design using the AXI-based fabric DMA controller. Throughput for data transfers is dependent on the host PC system configuration and the type of PCIe slots used. Table 4 shows the throughput values observed on the HP workstation Z220 PCIe slot 4.

Table 4 • **Throughput Summary**

DMA Transfer Type		Throughput in Mbytes/sec							
		SmartFusion2 (X4 Lane)				**IGLOO2 (X1 Lane)**			
		Gen1		**Gen2**		**Gen1**		**Gen2**	
		Single xfer	**Loop xfer (50)**	**Single xfer**	**Loop xfer (50)**	**Single xfer**	**Loop xfer (50)**	**Single xfer**	**Loop xfer (50)**
Host PC to LSRAM	Read	696	678	1065	1054	196	162	383	385
	Write	828	830	1075	1075	224	220	491	492
	R/W	694/829	674/829	1065/1075	1042/1075	183/223	173/203	384/492	380/492
DDR to LSRAM	Read	594	580	594	583	555	546	521	512
	Write	594	594	594	592	352	352	329	322
	R/W	594/594	594/594	594/594	594/592	551/352	554/345	520/329	519/320
Host PC to DDR	Read	495	487	522	512	152	161	295	290
	Write	565	565	565	555	217	191	431	432
	R/W	494/565	488/552	522/565	512/550	186/188	157/199	294/431	284/430

3 Appendix: IGLOO2 Evaluation Kit Board Setup for Laptop

Figure 34 shows how to line up the IGLOO2 Evaluation Kit PCIe connector with the adapter card slot.

Figure 34 • **Lining up the IGLOO2 Evaluation Kit Board**

Note: The notch (highlighted in red) does not go into the adapter card.

Figure 35 shows the IGLOO2 Evaluation Kit PCIe connector inserted into the PCIe adapter card slot.

Figure 35 • **Inserting the IGLOO2 Evaluation Kit PCIe Connector**

Figure 36 on page 43 shows the PCIe adapter card and the IGLOO2 Evaluation Kit connected to the laptop.

Figure 36 • **IGLOO2 Evaluation Kit Connected to the Laptop**

4 Appendix: Register Details

Table 5 shows the registers used to interface with the fabric DMA Controller. These registers are in BAR1 address space.

Table 5 • **Register Details**

Register Name	Register Address	Description
PC_BASE_ADDR	0x8028	Host PC memory base address provided by the driver.
DMA_DIR	0x8008	DMA direction: **Direction** **Register Value** 1. PCIe → DDR memory 0x11AA0001 2. DDR → PCIe memory 0x11AA0002 3. LSRAM → DDR memory 0x11AA0003 4. DDR → LSRAM memory 0x11AA0004 5. PCIe → LSRAM memory 0x11AA0005 6. LSRAM → PCIe memory 0x11AA0006 To reset the DMA, the register value is 0x11AA0007. Before initiating DMA transactions, reset the DMA with the register value, 0X11AA0007. The DMA transactions 1 and 2, 3 and 4, or 5 and 6 can be performed simultaneously by writing the corresponding values one after other.
DMA_CH0_STATUS	0x8100	DMA Channel-0 status DMA_CH0_STATUS[31] 1 = DMA operation completed 0 = DMA operation not completed DMA_CH0_STATUS[15:0] = CLK count
DMA_CH1_STATUS	0x8108	DMA Channel-1 status DMA_CH1_STATUS[31] 1 = DMA operation completed 0 = DMA operation not completed DMA_CH1_STATUS[15:0] = CLK count
RW_REG	0X0	Scratchpad register for PCIe R/W.
LED_CTRL	0xA0	LEDs control register.
SWITCH_STATUS	0x90	DIP switch status.
Note: For the DDR memory, the source memory address is fixed as 0x0100_0000 and the destination memory address is fixed as 0x0000_0000.		

5 Revision History

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision 7 (April 2016)	Updated the document for Libero v11.7 software updates (SAR 77470).
Revision 6 (October 2015)	Updated the document for Libero v11.6 software updates (SAR 72063).
Revision 5 (August 2014)	Updated the designs files links.
Revision 4 (July 2014)	Updated the document for Libero v11.4 software updates (SAR 59587).
Revision 3 (April 2014)	Updated document for Libero v11.3 and for other enhancements (SAR 56080).
	MDDR throughput displayed in Mbps (SAR 53589).
	Throughput for Read and Write Transfer type is reversed in Throughput "Summary" on page 40 (SAR 53822).
	Updated throughput values in "Summary" on page 40 (SAR 53490).
Revision 2 (December 2013)	Updated Table 4 on page 40 (SAR 53490).
Revision 1 (December 2013)	Initial release.

6 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

6.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

6.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

6.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

6.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

6.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

6.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

6.5.2 My Cases

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6.5.3 Outside the U.S.

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6.6 ITAR Technical Support

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