SmartFusion2 SoC FPGA - Error Detection and Correction of eSRAM Memory - Libero SoC v11.7

DG0388 Demo Guide

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Contents

Figures

Tables

1 Preface

1.1 Purpose

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on single error correction and double error detection (SECDED) capabilities of the embedded static random-access memory (eSRAM).

1.2 Intended Audience

This demo guide is intended for:

- FPGA designers
- Embedded designers
- System-level designers

1.3 References

The following documents are referred in this demo guide:

- *UG0443: SmartFusion2 and IGLOO2 FPGA Security and Reliability User Guide*
- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *TU0546: SoftConsole v4.0 and Libero SoC v11.7 Tutorial*

2 SmartFusion2 SoC FPGA - Error Detection and Correction of eSRAM Memory

2.1 Introduction

This document describes the error detection and correction (EDAC) capabilities of the SmartFusion2 devices on the eSRAM.

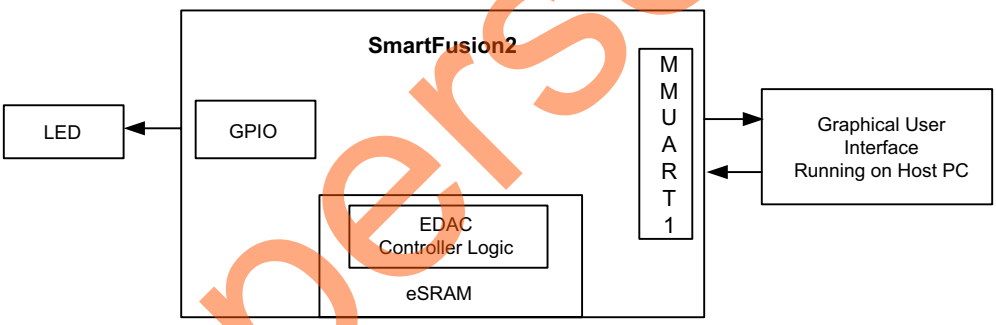
The EDAC controllers implemented in the SmartFusion2 devices support SECDED. All memories within the microcontroller subsystem (MSS) of the SmartFusion2 are protected by SECDED. The eSRAM memory can be eSRAM_0 or eSRAM_1. The address range of eSRAM_0 is 0x20000000 to 0x20007FFF and the address range of eSRAM_1 is 0x20008000 to 0x2000FFFF.

When SECDED is enabled:

- A write operation computes and adds 8 bits of SECDED code to every 32 bits of data
- A read operation reads and checks the data against the stored SECDED code to support 1-bit error correction and 2-bit error detection

In this demo, the EDAC can be identified by the blinking light-emitting diode (LED) on the board and by graphical user interface (GUI).

Figure 1 • **Top-Level Block Diagram**



The EDAC of eSRAM supports the following features:

1. SECDED mechanism
2. Provides interrupts to the ARM® Cortex®-M3 processor and FPGA fabric upon the detection of a 1-bit error or 2-bit error.
3. Stores the number of 1-bit and 2-bit errors to the error counter registers.
4. Stores the address of the last 1-bit or 2-bit error affected memory location.
5. Stores 1-bit or 2-bit error data into the SECDED registers.
6. Provides error bus signals to the FPGA fabric.

Refer to the EDAC chapter of the *UG0443: SmartFusion2 and IGLOO2 FPGA Security and Reliability User Guide* and the eSRAM chapter of the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

2.2 Demo Requirements

Table 1 shows the demo requirements.

Table 1 • **Demo Requirements**

Hardware Requirements	**Description**
SmartFusion2 Security Evaluation Kit: • FlashPro4 programmer • USB A to Mini - B USB cable • 12 V Adapter	Rev D or later
Operating System	Any 64-bit or 32-bit Windows XP SP2 Any 64-bit or 32-bit Windows 7
Software Requirements	
Libero® system-on-chip (SoC) software	v11.7
SoftConsole	v3.4 SP1*
FlashPro programming software	v11.7
Host PC Drivers	USB to UART drivers
For launching demo GUI	Microsoft .NET Framework 4 client
Note: *For this user guide, SoftConsole v3.4 SP1 is used. For using SoftConsole v4.0, see the *TU0546: SoftConsole v4.0 and Libero SoC v11.7 Tutorial*.	

2.2.1 Design Files

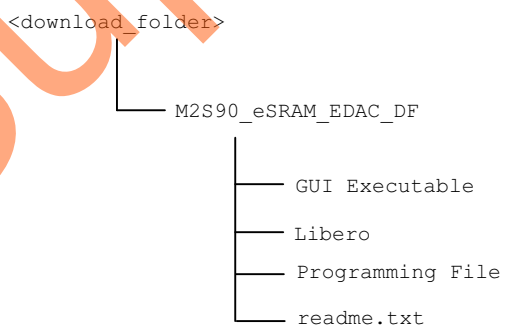
The demo design files are available for download from the following path in the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0388_liberov11p7_df*

Design files include:

- Libero
- Programming files
- GUI Executable
- Readme file

Figure 2 shows the top-level structure of the design files. For further details, see the `readme.txt` file.

Figure 2 • **Demo Design Top-Level Structure**



2.3 Demo Design Description

Each eSRAM within the MSS is protected by a dedicated EDAC controller. EDAC detects a 1-bit error or 2-bit error when data is read from the memory. If EDAC detects the 1-bit error, the EDAC controller corrects the same error bit. If EDAC is enabled for all the 1-bit and 2-bit errors, corresponding error counters in the system registers are incremented and corresponding interrupts and error bus signals to the FPGA fabric are generated.

In a single event upset (SEU) susceptible environment, random access memory (RAM) is prone to transient errors caused by heavy ions. This happens in real-time. To demonstrate this, an error is introduced manually and detection and correction is observed.

This demo design involves implementation of following tasks:

- Enable EDAC
- Write data to eSRAM
- Read data from eSRAM
- Disable EDAC
- Corrupt one or two bits
- Write data to eSRAM
- Enable EDAC
- Read the data
- In the case of a 1-bit error, the EDAC controller corrects the error, updates the corresponding status registers, and gives the data written in Step 2 at the read operation done at Step 8.
- In the case of a 2-bit error, a corresponding interrupt is generated and the application must correct the data or take the appropriate action in the interrupt handler. These two methods are demonstrated in this demo.

Two tests are implemented in this demo: loop test and manual test and they are applicable to both 1-bit and 2-bit errors.

2.3.1 Loop Test

Loop Test is executed when the SmartFusion2 receives a loop test command from the GUI. Initially, all the error counters and EDAC related registers are placed in the **RESET** state.

The following steps are executed for each iteration:

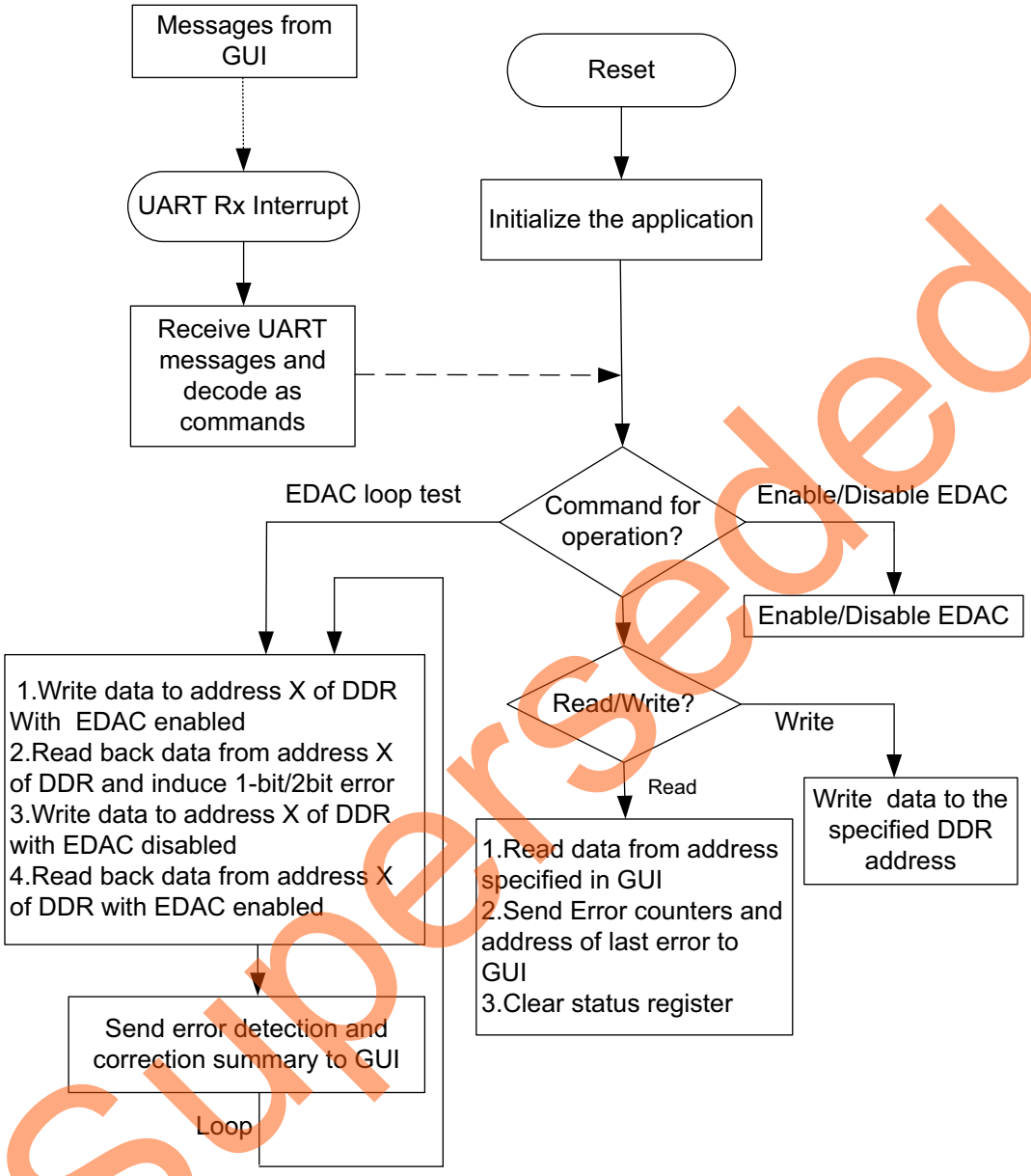
1. Enable the EDAC controller.
2. Write the data to the specific eSRAM memory location.
3. Disable the EDAC controller.
4. Write the 1-bit or 2-bit error induced data to the same eSRAM memory location.
5. Enable the EDAC controller.
6. Read the data from the same eSRAM memory location.
7. Send the 1-bit or 2-bit error detection and 1-bit error correction data in case of 1-bit error to the GUI.

2.3.2 Manual Test

This method allows manual testing for enabling or disabling EDAC and write or read operation. Using this method, 1-bit or 2-bit errors can be introduced to any location within the eSRAM. Enable the EDAC and write data to the specified address using the GUI fields. Disable the EDAC and write 1-bit or 2-bit corrupted data to the same address location. Enable the EDAC and read the data from the same address location then the LED on the board must toggle to notify the detection and correction of errors. The corresponding error counter is displayed on to the GUI. The GUI Serial Console logs all the actions performed in SmartFusion2.

Figure 3. shows the eSRAM EDAC demo operations.

Figure 3 • **Design Flow**



2.4 Running the Demo

This section describes the SmartFusion2 Security Evaluation Kit board setup, the GUI options, and how to execute the demo design.

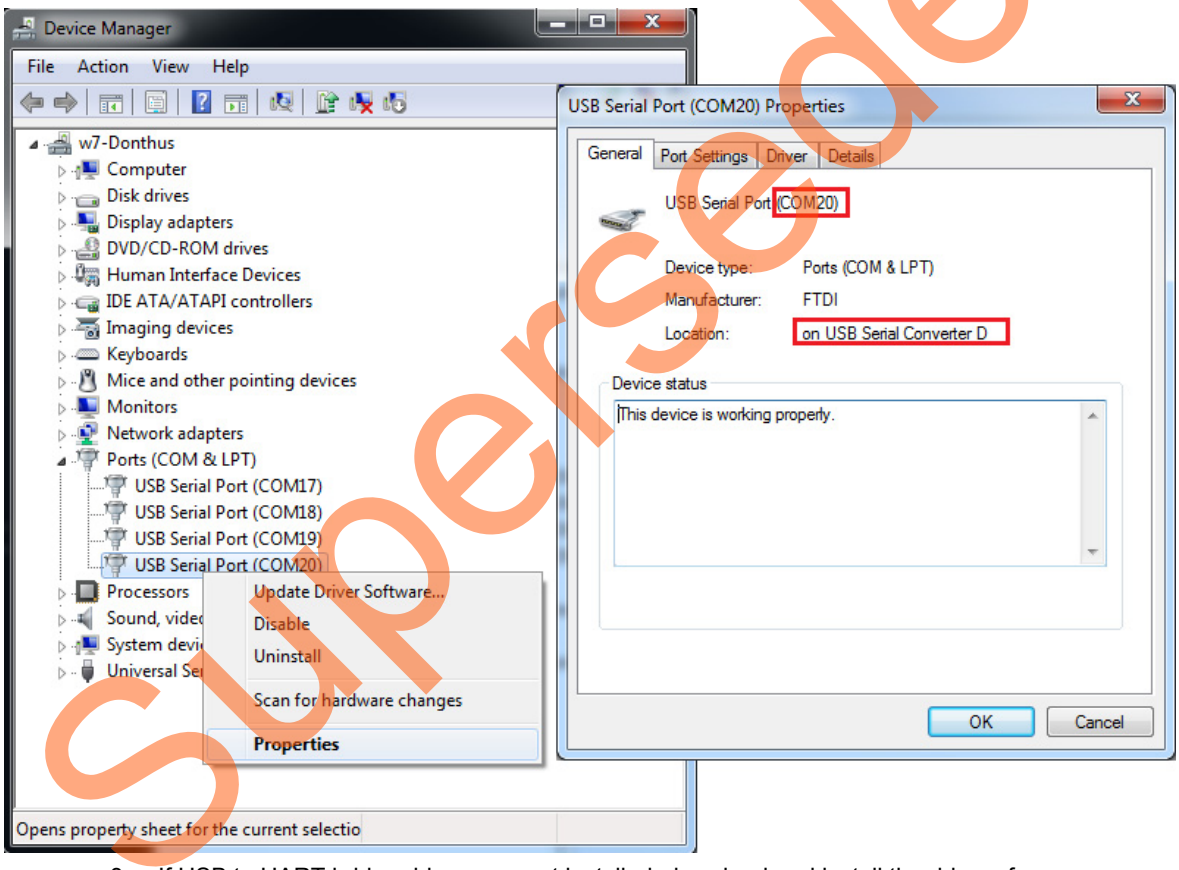
2.4.1 Demo Setup

The following steps describe how to setup the demo:

1. Connect the FlashPro4 programmer to the **J5** connector of SmartFusion2 Security Evaluation Kit board.
2. Connect one end of the USB mini-B cable to the **J18** connector provided in the SmartFusion2 Security Evaluation Kit board. Connect the other end of the USB cable to the host PC. Ensure that the USB to UART Bridge drivers are automatically detected (can be verified in the Device Manager), as shown in Figure 4.

Note: Copy the COM port number for serial port configuration. Ensure that the COM port **Location** is specified as **on USB Serial Converter D**, as shown in Figure 4.

Figure 4 • **USB to UART Bridge Drivers**



3. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip

4. Connect the jumpers on the SmartFusion2 Security Evaluation Kit board, as shown in Table 2. The power supply switch **SW7** must be switched **OFF** while making the jumper connections.

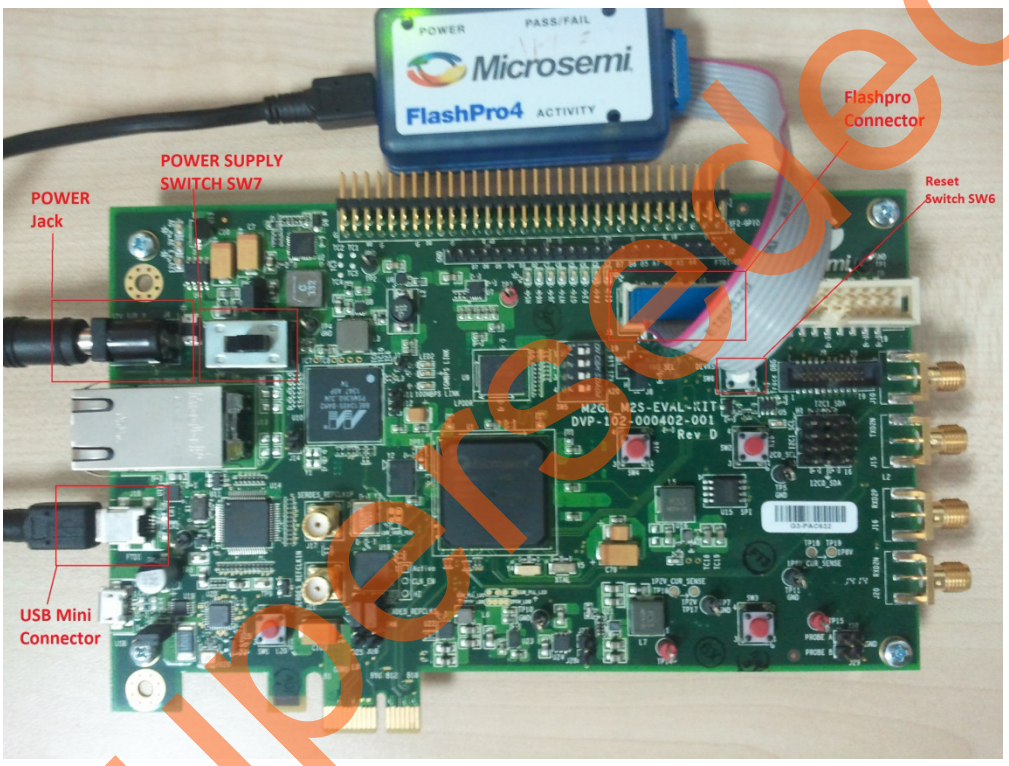
Table 2 • **SmartFusion2 Security Evaluation Kit Jumper Settings**

Jumper	Pin (From)	Pin (To)	Comments
J22, J23, J24, J8, J3	1 (default)	2	These are the default jumper settings of the SmartFusion2 Security Evaluation Kit board. Ensure that these jumpers are set accordingly.

5. Connect the power supply to **J18** connector.

Figure 5. shows the board setup for running the demo on the SmartFusion2 Security Evaluation Kit.

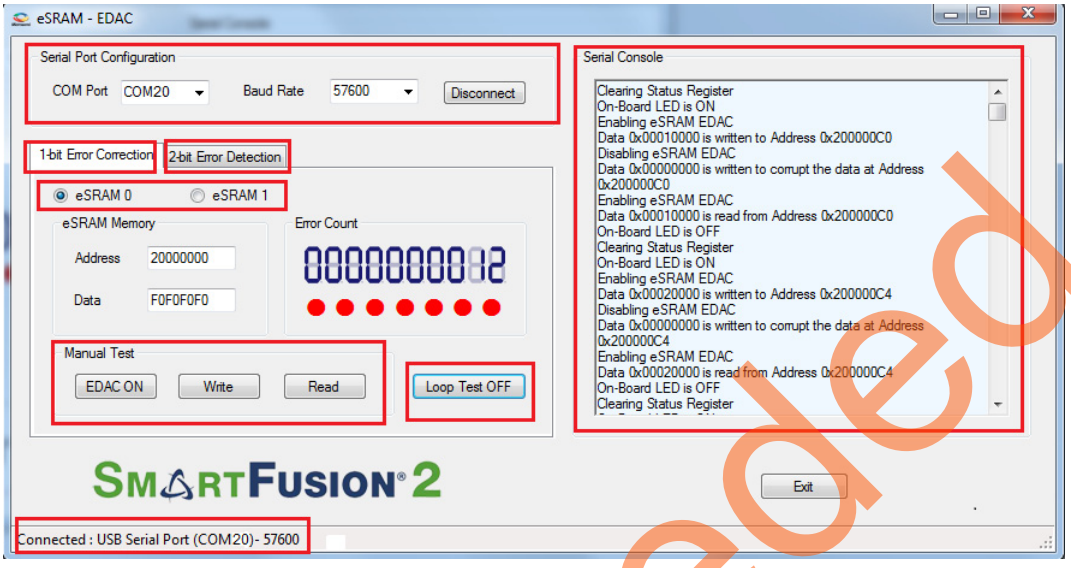
Figure 5 • **SmartFusion2 Security Evaluation Kit Board Setup**



2.4.2 Graphical User Interface

The following section describes about eSRAM - EDAC demo GUI.

Figure 6 • **eSRAM – EDAC Demo GUI**



The GUI supports the following features:

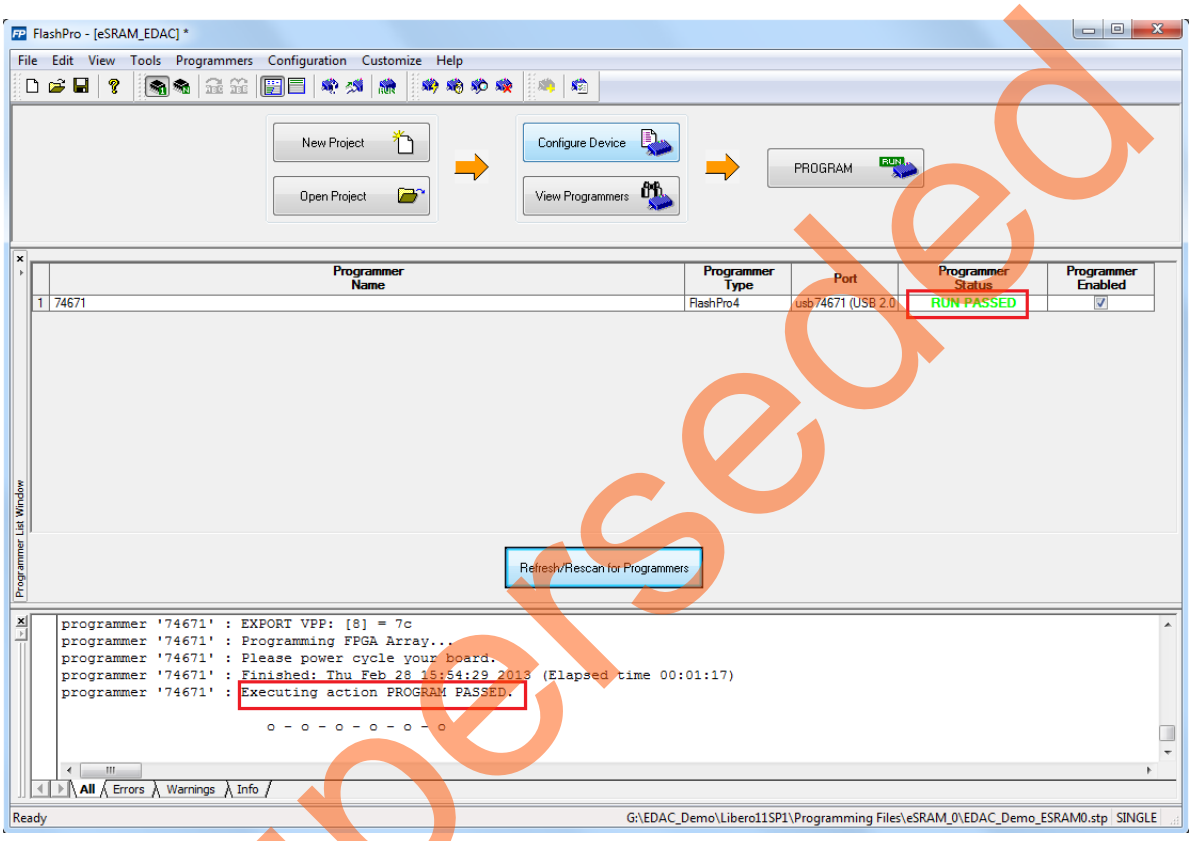
1. Selection of COM port and Baud Rate.
2. Selection of 1-bit error correction tab or 2-bit error detection tab.
3. Selection of eSRAM0 or eSRAM1.
4. Address field to write or read data to or from specified eSRAM address.
5. Data field to write or read data to or from specified eSRAM address.
6. Serial Console section to print the status information received from the application.
7. **EDAC ON/OFF**: Enables or disables the EDAC.
8. **Write**: Allows writing data to the specified address.
9. **Read**: Allows reading data from the specified address.
10. **LOOP test ON/OFF**: Allows testing the EDAC mechanism in a loop method.

2.4.3 Running the Design

The following steps describe how to run the design:

1. Switch **ON** the supply switch, **SW7**.
2. Program the SmarFusion2 device with the programming file provided in the design files (`\ProgrammingFiles\eSRAM_0\EDAC_Demo_eSRAM0.stp` or `\ProgrammingFiles\eSRAM_1\EDAC_Demo_eSRAM1.stp`) using FlashPro design software, as shown in Figure 7.

Figure 7 • **FlashPro Programming Window**



3. Press **SW6** switch to reset the board after successful programming.
4. Launch the **EDAC_eSRAM Demo** GUI executable file available in the design files (`\GUI Executable\ EDAC_eSRAM.exe`). The GUI window is displayed, as shown in Figure 6 on page 12.
5. Select the appropriate COM port (to which USB to UART Bridge drivers are pointed) from the **COM Port** drop-down list.
6. Select the **Baud Rate** as 57600 and click **Connect**. After establishing the connection, **Connect** changes to **Disconnect**.
7. Select eSRAM 0 or eSRAM 1 depending upon the programming file selected in step 2.
8. Select the 1-bit **Error Correction** tab or 2-bit **Error Detection** tab, as shown in Figure 8 on page 14. and Figure 9 on page 15.
9. Two types of tests can be performed: Manual and Loop.

2.4.3.1 Performing Loop Test

Click **Loop Test ON**. It runs in loop mode where continuous correction and detection of errors is done. The loop runs for 200 iterations. All actions performed in SmartFusion2 are logged in the **Serial Console** section of the GUI. The 2-bit Error Detection loop test prints the error affected eSRAM address offset in Serial Console. Click **Loop Test OFF** after 200 iterations completed.

Table 3 • **eSRAM Memory Addresses Used in Loop Test**

Memory	1-Bit Error Correction	2-Bit Error Detection
eSRAM0	0x20000000	0x20002000
eSRAM1	0x20008000	0x2000A000

2.4.3.2 Performing Manual Test

In this method, errors are introduced manually using GUI. Use the following steps to execute 1-bit error correction or 2-bit error detection:

1. Input Address and Data fields (use 32-bit Hexadecimal values).
2. Click **EDAC ON**.
3. Click **Write**.
4. Click **EDAC OFF**.
5. Just change 1-bit (in case of 1-bit error correction) or 2 bits (in case of 2-bit error detection) in Data field (introducing error).
6. Click **Write**.
7. Click **EDAC ON**.
8. Click **Read**.
9. Observe **Error Count** display and **Data** field in the GUI. The error count value increases by 1.

All the actions performed in SmartFusion2 are logged in **Serial Console** section of GUI.

Note: To switch from **1-bit Error Correction** tab to **2-bit Error Detection** tab or vice versa in EDAC_eSRAM Demo GUI, Reset the Hardware Board.

Figure 8 • **1-Bit Error Correction Tab**

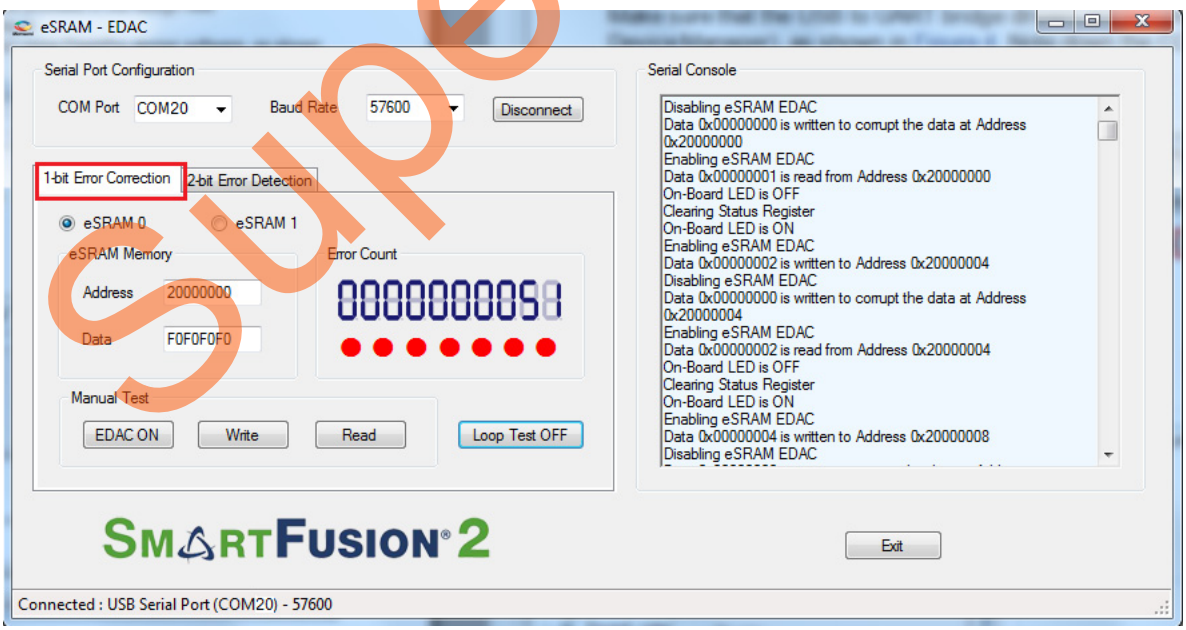
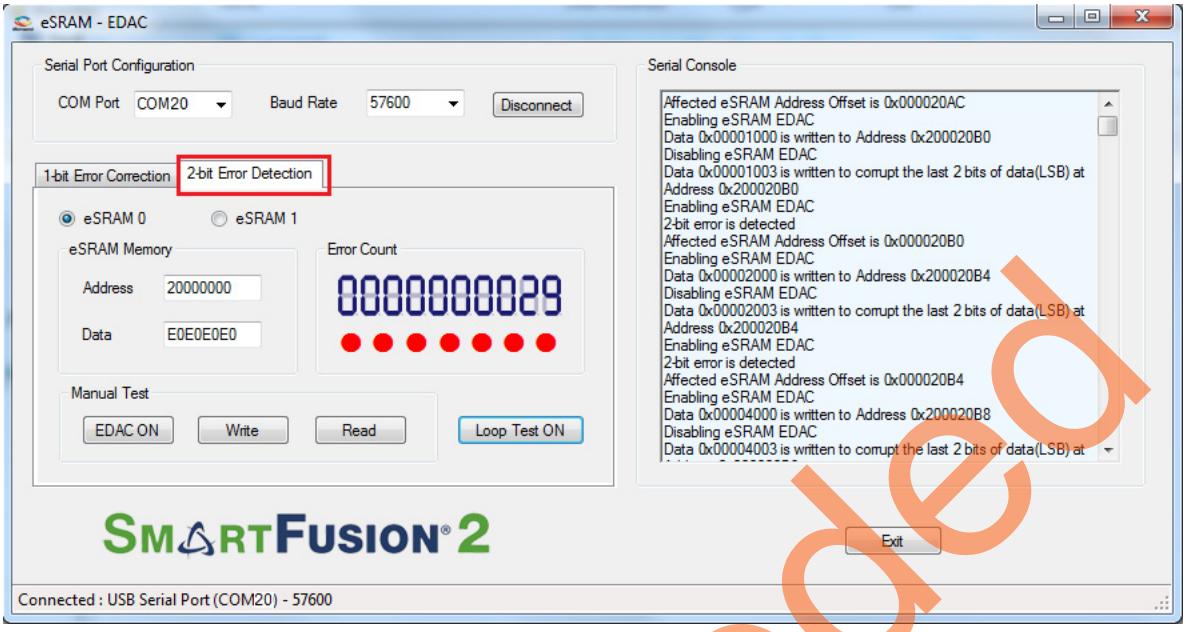


Figure 9 • **2-Bit Error Detection Tab**



2.5 Conclusion

This demo shows SmartFusion2 SECDED capabilities of the eSRAM.

3 Revision History

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision 8 (April 2016)	Updated the document for Libero SoC v11.7 software release (SAR 77402).
Revision 7 (October 2015)	Updated the document for Libero SoC v11.6 software release (SAR 72777).
Revision 6 (February 2015)	Updated the document for Libero SoC v11.5 software release (SAR 64979).
Revision 5 (September 2014)	Updated the document for Libero SoC v11.4 software release (SAR 60476).
Revision 4 (May 2014)	Updated the document for Libero SoC v11.3 software release (SAR 56852).
Revision 3 (November 2013)	Updated the document for Libero SoC v11.2 software release (SAR 52960).
Revision 2 (May 2013)	Updated the document for Libero SoC v11.0 software release (SAR 47858).
Revision 1 (March 2013)	Updated the document for Libero SoC v11.0 Beta SP1 (SAR 45586).

4 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

4.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

4.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

4.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

4.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

4.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

4.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

4.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

4.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

4.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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