UG0717
User Guide
Netlist Viewer

Microsemi
Power Matters.™

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50200717-1/1.17

Revision History

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision 1 January 2017	Initial release.
Revision 2 January 2017	Added support for PolarFire FPGA.

Contents

List of Figures

1 Introduction

The Netlist Viewer is a graphical representation of the design netlist. As FPGA designs grow in size and complexity, it has become essential for the FPGA designer to traverse the netlist to analyze the design.

Available for SmartFusion2, IGLOO2, RTG4, and PolarFire families, the Microsemi Netlist Viewer is a graphical user interface that displays different views for the different stages of the design process:

- RTL Netlist View - Technology-independent netlist view of the design before mapping of the design elements to the Microsemi-specific technology. Using the RTL view is a fast and easy way to determine whether the correct logic has been implemented by the software. Cross-probing from this view to the HDL code facilities troubleshooting when the design is not working as desired.
  Note: The RTL Netlist View cannot be opened if the project contains mixed Verilog and VHDL files.
- Post-Synthesis Hierarchical View - Hierarchical view of the netlist after synthesis and after technology mapping to the Microsemi FPGA technology.
- Post-compile flattened Netlist View - A flattened netlist after synthesis, technology mapping and further optimization based on the DRC rules of the device family and/or die.

Figure 1 • **Netlist Viewer - RTL View**

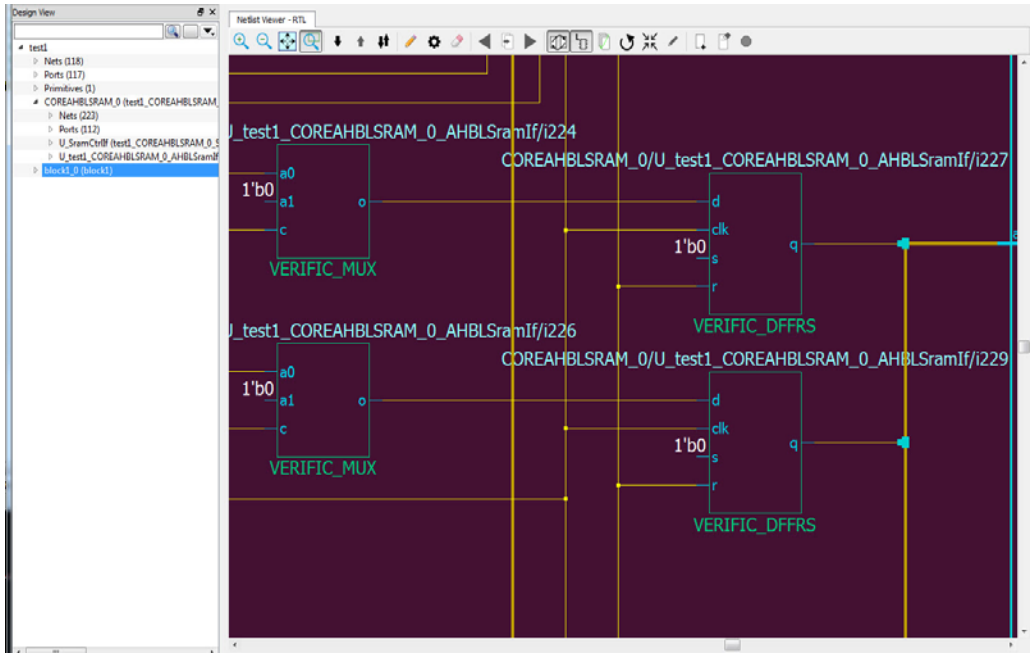


Figure 2 • **Netlist Viewer - Hierarchical View**

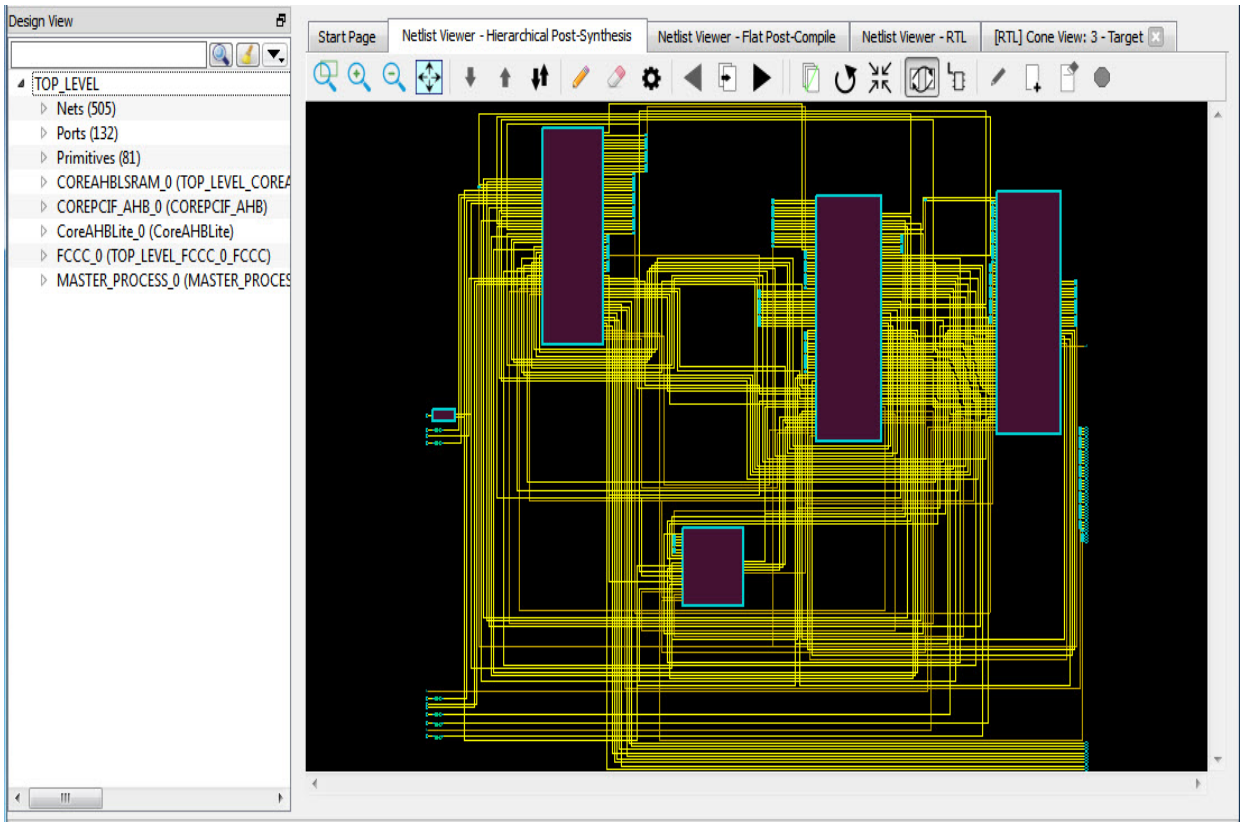
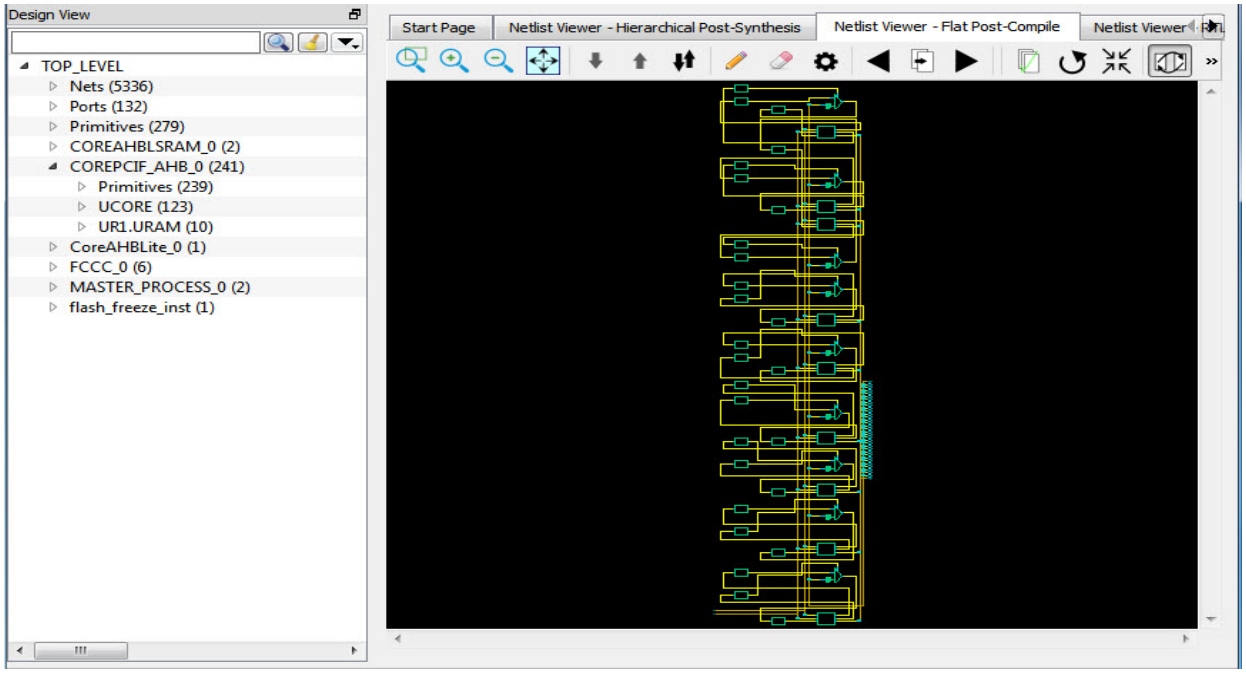


Figure 3 • **Netlist Viewer - Flattened View**



Note: A progress bar pops up to indicate the flattened netlist is being loaded. For a large netlist, the loading may incur some runtime penalty. A **Cancel** button is available to cancel the loading.

2 Invocation

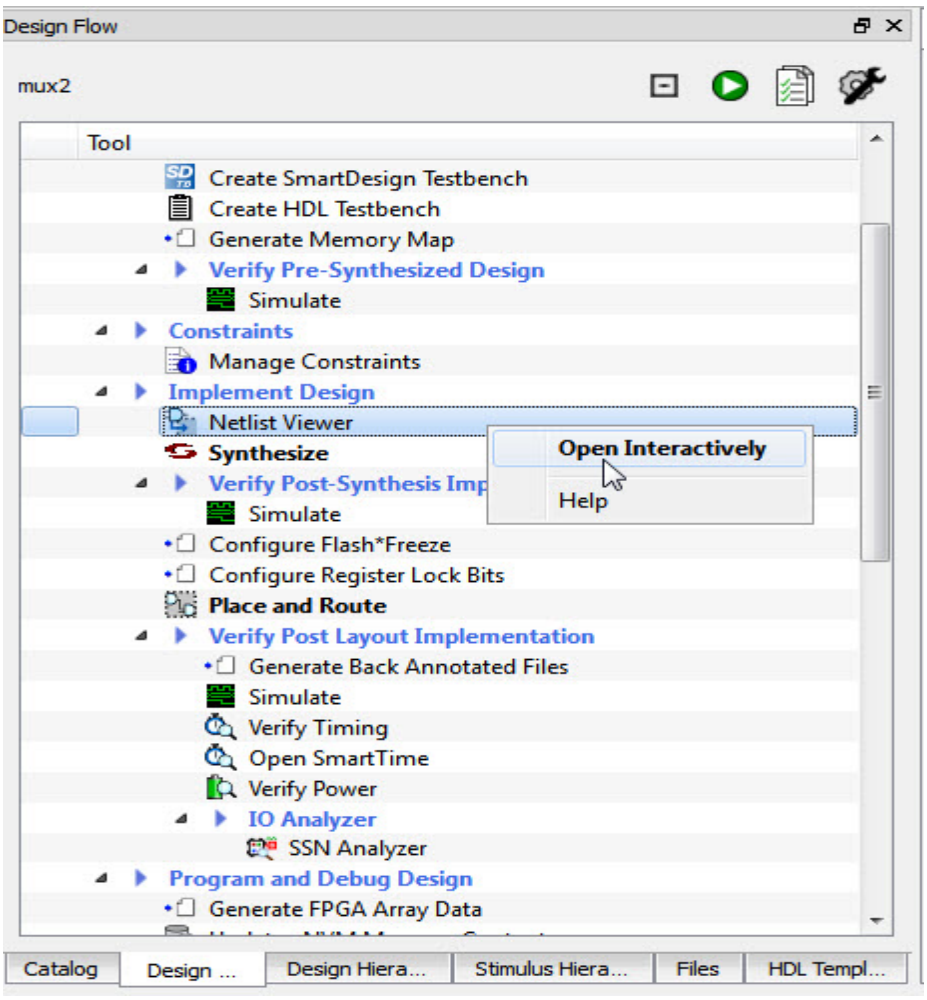
The standalone Netlist Viewer is invoked from the Design Flow window in the Libero SoC project.

The standalone Netlist Viewer is available for invocation in the Design Flow window for SmartFusion2, IGLOO, RTG4, and PolarFire devices.

To open the standalone Netlist Viewer, do one of the following:

- Double-click Netlist Viewer inside the Design Flow window.
- Right-click Netlist Viewer and select Open Interactively (**Netlist Viewer > Open Interactively**)

Figure 4 • **Netlist Viewer Invocation**



When Netlist Viewer opens, it makes available for loading and viewing the following views of the netlist:

- RTL Views - Available after design capture/design generation
- Hierarchical Post-Synthesis - Available after Synthesis
- Flat Post-Compile - Available after Synthesis or Place and Route. If after Place and Route, the Netlist Viewer loads the Flat Post-Compile view to reflect the netlist generated after Place and Route.

3 Netlist Viewer Windows

When the standalone Netlist Viewer opens, no netlist views are loaded.The Start Page displays what netlist views can be opened for viewing.

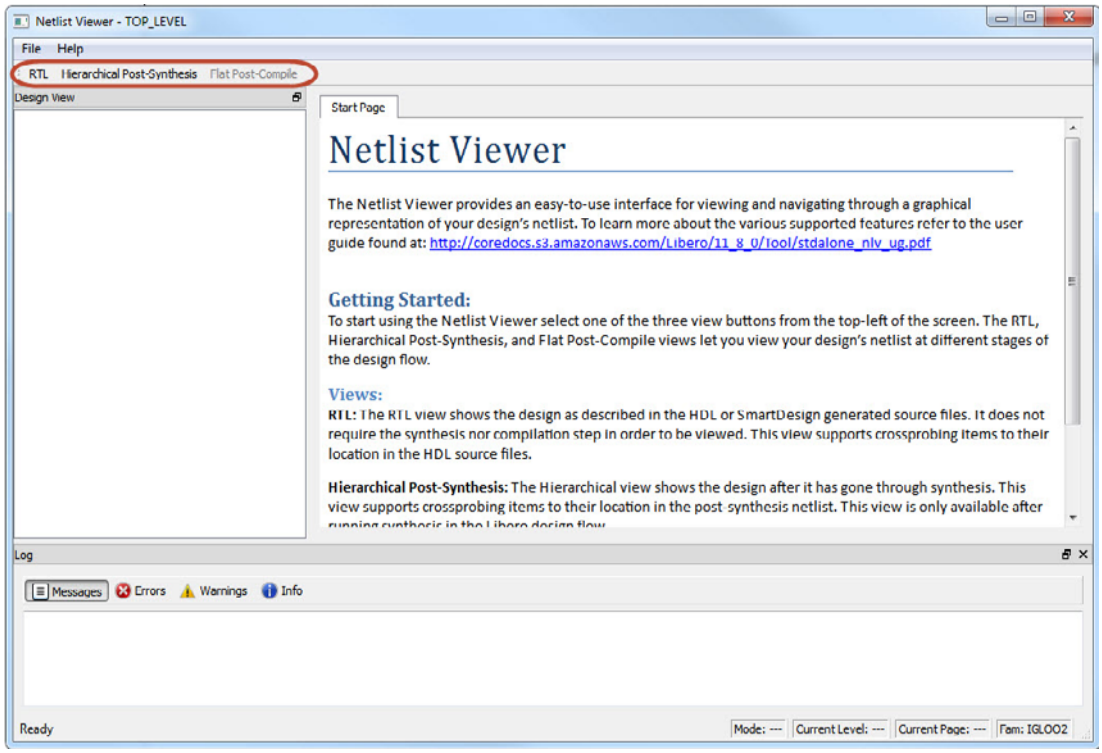
The Netlist Viewer User Guide is available from the Help menu (**Help > Reference Manuals**)

3.1 Opening a View

Click any one of following views (across the top left corner) to load the netlist into the Netlist Viewer for viewing:

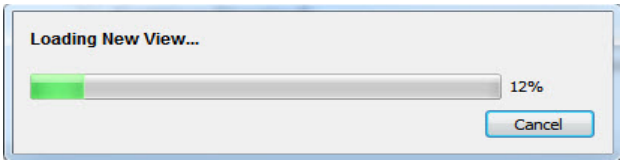
- RTL view
- Hierarchical Post-Synthesis view
  Note: Not available if synthesis is disabled in the design flow (**Project > Project Settings > Enable Synthesis** is unchecked)
- Flat Post-Compile view

Figure 5 • **Nelist Viewer on Start Up**



Note: When netlist views are opened for the first time in the Netlist Viewer, they are first loaded into the system memory and stay in the system memory until the Netlist Viewer exits. For very large designs, loading the netlist for the first time may incur some runtime penalty. A pop-up window reports the status of the loading process.

Figure 6 • **Pop-up Window**



When the netlist views are opened for the second and subsequent times, the netlist views are available almost immediately in the Netlist Viewer because they are already loaded into the system's memory.

3.2 Closing a View

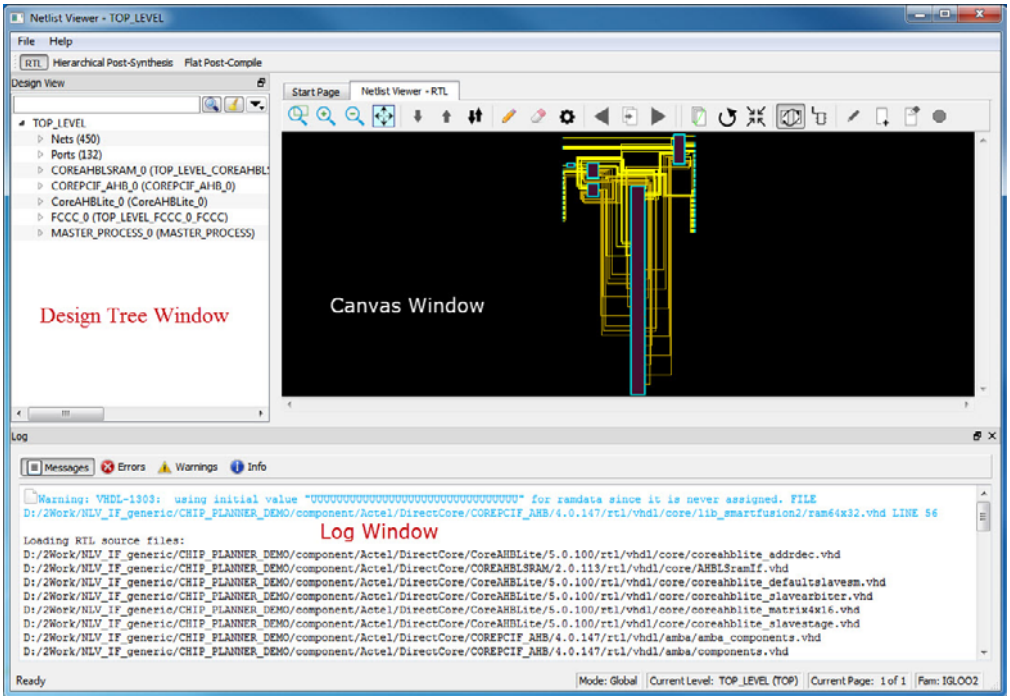
Click any opened view (across the top of the Netlist Viewer) to close any opened view. A closed view stays in the system memory as long as Netlist Viewer remains open. Opening the same netlist view at a later time does not incur runtime penalty as no loading is required.

3.3 Netlist Viewer Windows

The Netlist Viewer has three windows:

- Design Tree window - displays the design hierarchy from the top level
- Canvas Window - displays the netlist views
- Log Window - displays messages/warnings/Info etc.

Figure 7 • **Netlist Viewer Windows**



3.4 Design Tree Window

This Window displays the design hierarchy from the top level. Information displayed includes:

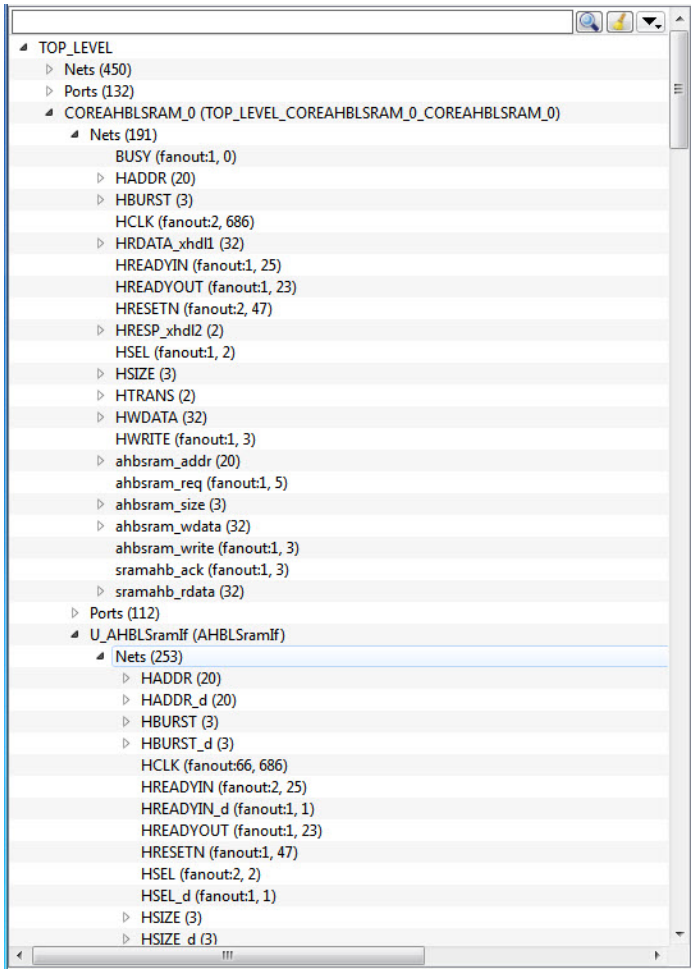
- Nets (<interger>) - the number in brackets is the total number of nets at the top level.
- Ports (<integer>) - the number in brackets is the total number of ports at top level
- Design components under the top level - each component can be collapsed or expanded to expose
  - nets - total number of nets at the component level
  - ports - total number of ports at the component level
  - sub-components inside the component

- Fanout Values (Nets) - When two numbers are displayed in the bracket, the first number is the fanout of the net at the local level (of hierarchy) and the second number is the fanout of the net at the global level. As an example, net_xyz (fanout:1,3) means the net goes down the levels of hierarchy to three different pins (global fanout 3) and is not connected to any other pins at the current level (local fanout 1).
- Primitives - Primitives refer to macros and low-level design objects and can appear in the top level or component level.

The design tree is different with different netlist views. For the Flat Post-Compile view, the design tree displays a much bigger number of nets than the RTL or Hierarchical Post-Synthesis view because the netlist is flattened in the Post-Compile view and all nets are counted. The nets in the Flat Post-Compile view, unlike the RTL view or the Hierarchical Post-Synthesis view, do not show the fanout value. Displaying the fanout value of all the nets in the Flat Post-Compile netlist incurs too much of a runtime penalty to make it practicable.

For the nets that are part of a NetBundle, the NetBundle name is followed by a number in parenthesis that indicates the total number of nets in the NetBundle.

Figure 8 • **Design Tree Window**



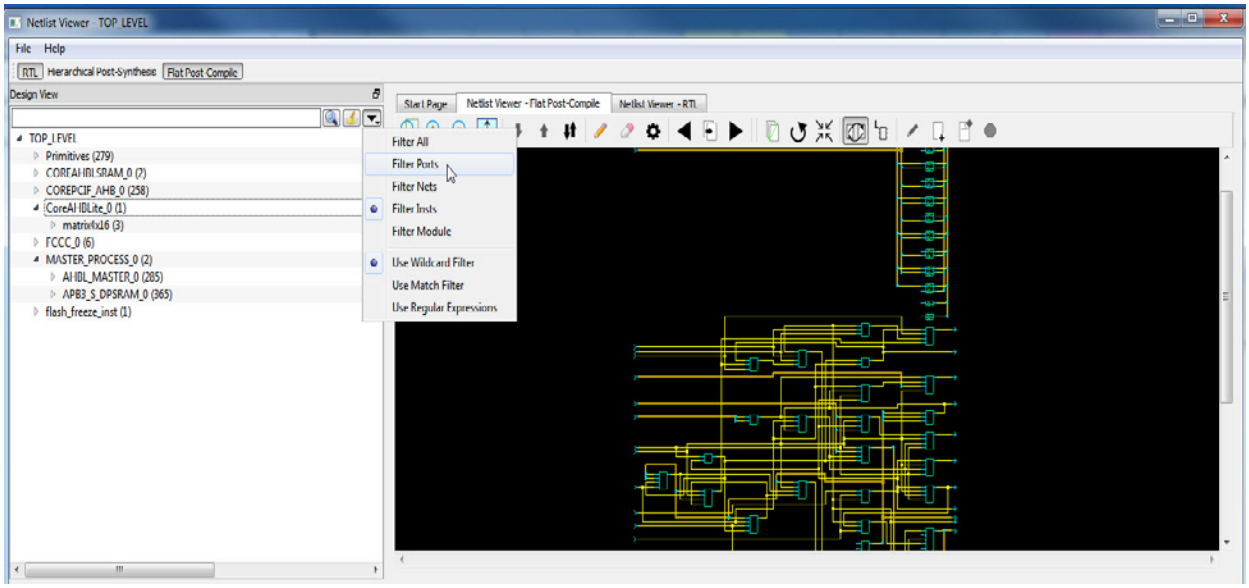
3.4.1 Filter

The display of design objects in this view can be filtered based on:

- Ports - displays all ports only, including component level ports
- Nets - displays all nets only, including component level nets
- Instances - display all instances only, including component level instances
- Modules - display all modules only

- Filter All - display all design objects only
- Use Wildcard Filter
- Use Match Filter
- Use Regular Expressions

Click the Filter button at the top right corner of the Design View to filter design objects.



3.4.2 Interoperability Between Windows and Views

When a design object such as a net, an instance or a port, is selected in the design tree window, the object is selected in the different netlist views. The reverse is also true. An object selected in one netlist view window is also selected in the design tree window and other netlist views.

Interoperability works only when the Toggle Crossprobing icon is enabled.

3.5 Canvas Window

The Canvas Window displays the:

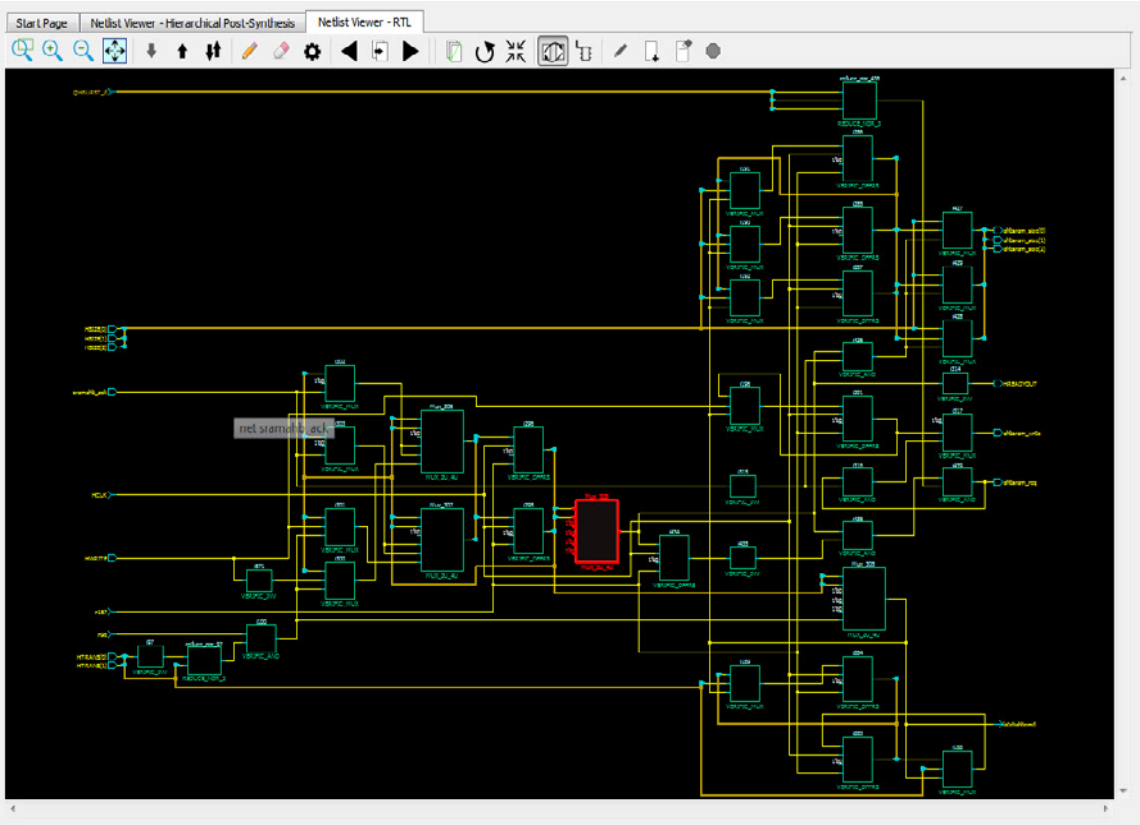
- RTL view
- Hierarchical Post-Synthesis view
- Flat Post-Compile view
- Cones view
- Opened HDL files (not available in the Flat Post-Compile view)
- Start Page - when no netlist views are opened

When a view is opened, a view tab is added across the top of the Canvas Window for ease of switching among the different views. Inside the canvas window, there is a list of icons across the top of the window for the user to

- Traverse vertically up (Pop) or down (Push) the design hierarchy
- Navigate horizontally across different pages of the design view
- Zoom in/out of the design view
- Trace critical nets to the driver/load
- Create logical cones for debugging
- Control the color display of the design objects in the Canvas Window

See the Netlist Viewer Interface User Guide for details.

Figure 9 • **Canvas Window**

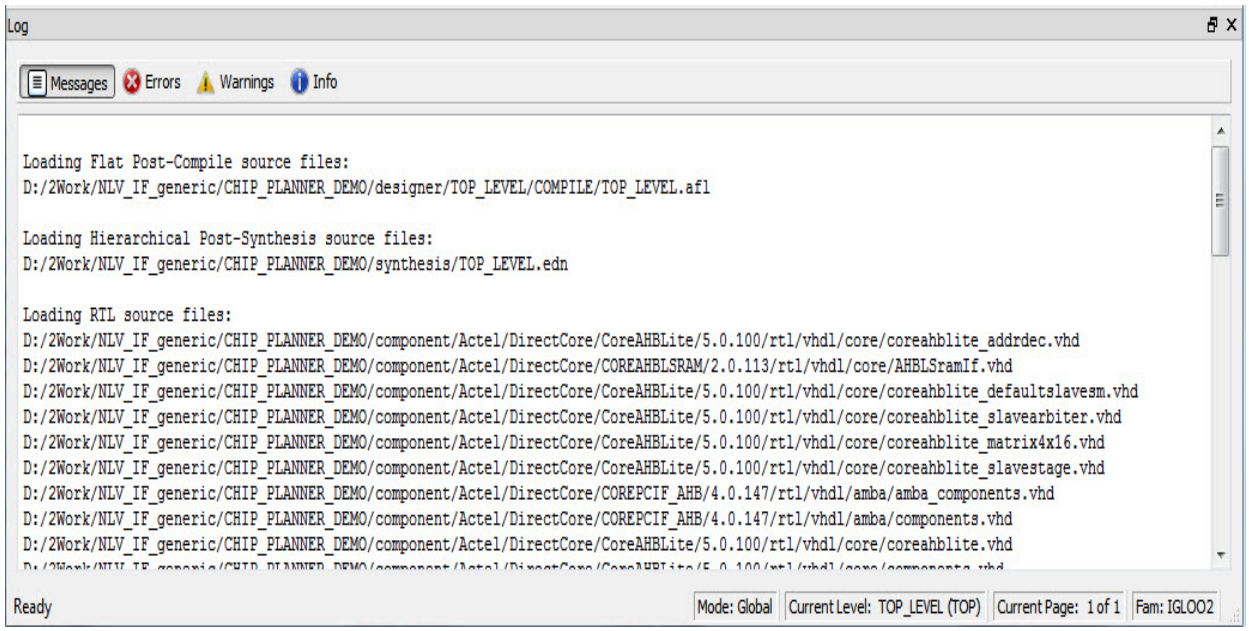


3.6 Log Window

The Log Window displays the following:

- Informational messages such as the location and name of the files used to display the view
- Error messages such as the failure to open design source files in RTL view because the design contains a mix of Verilog and VHDL source files
- Warning messages such as when over 1,000 items are selected in a netlist view.
- Syntax errors, if any, in the HDL file if the HDL file is opened with the “Open File Location” option (Right-click design object > Open File Location).

Figure 10 • **Log Window**



3.7 Status Bar

The status bar at the bottom right corner of the Netlist Viewer displays the following:

- Mode - Either Global or Local mode is displayed. Global mode means the Netlist Viewer can cross hierarchical boundaries when following nets to drivers or loads. Local means the Netlist Viewer stays in the current level of design hierarchy.
- Current Level - displays the current level of design hierarchy, either TOP_LEVEL instance name or instance name of the component.
- Current Page - displays the current page of the Netlist Viewer (Page x of <total>) when traversing across different pages of the Netlist Viewer.
- Fam - displays the technology family.

Figure 11 • **Status Bar**

4 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

4.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

4.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

4.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

4.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

4.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

4.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

4.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

4.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

4.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.