# PolarFire FPGA Board Design User Guide

## Introduction (Ask a Question)

Good board design practices are required to achieve expected performance from both Printed Circuit Boards (PCBs) and PolarFire® devices. High-quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines must be treated as a supplement to the standard board-level design practices.

This document is intended for readers who are familiar with the PolarFire device, experienced in digital board design, and know about the electrical characteristics of the systems. It discusses power supplies, high-speed interfaces, various control interfaces, and the associated peripheral components of the PolarFire FPGAs.

# Table of Contents

# 1. Designing the Board (Ask a Question)

PolarFire FPGAs are Flash-based FPGAs that support various high-speed memory interfaces such as DDR3/DDR4, lowest power 12.7 Gbps transceiver (XCVR), built-in low-power dual PCIe Gen2, and fabric I/O such as high-speed I/O (HSIO) and general-purpose I/O (GPIO).

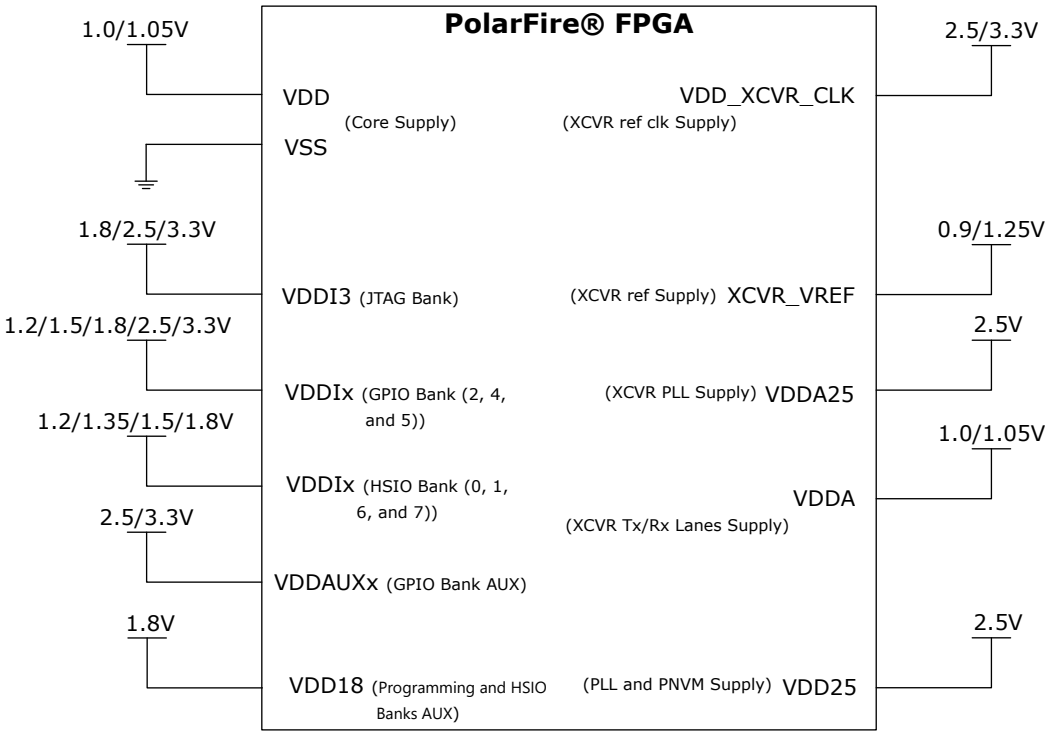
Subsequent sections discuss the following topics:



## 1.1 Power Supplies (Ask a Question)

The following illustration shows the typical power supply requirements for PolarFire devices and the recommended connections of power rails when every part of the device is used in a system. For information on decoupling capacitors associated with individual power supplies, see 1.1.1. PolarFire Decoupling Capacitors.

**Figure 1-1.** Power Supplies




To calculate the number of decoupling capacitors, it is important to know the target impedance of the power plane. Target impedance is calculated as follows:

**Equation 1-1.** Target Impedance

$$Z_{Max} = \%\ \text{Ripple} \times \frac{V_{supply}}{I_{trans}}$$

Where:

- $V_{supply}$: Supply voltage of the power plane
- % Ripple: Percentage of ripples that is allowed on the power plane. See PolarFire FPGA Datasheet for more information about ripple in Recommended Operating Conditions table.
- $I_{trans}$: Transient current drawn on the power plane. The transient current is half of the maximum current. Maximum current is taken from the Power Calculator Sheet.
- Zmax: Target impedance of the plane

For the device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All overshoots and undershoots must be within the absolute maximum ratings provided in the PolarFire FPGA Datasheet.

The following table lists the various power supplies required for PolarFire FPGAs.

**Table 1-1.** Supply Pins

| Name | Description |
|---|---|
| XCVR_VREF | Voltage reference for transceivers |
| VDD_XCVR_CLK | Power to input buffers for the transceiver reference clock |
| VDDA25 | Power to the transceiver PLL |
| VDDA[1] | Power to the transceiver TX and RX lanes |
| VSS | Core digital ground |
| VDD[2] | Device core digital supply |
| VDDI3 (JTAG Bank) | Power to JTAG bank pins |
| VDDIx (GPIO Banks) | Power to GPIO bank pins |
| VDDIx (HSIO Banks) | Power to HSIO bank pins |
| VDD25 | Power to corner PLLs and PNVM |
| VDD18 | Power to programming and HSIO auxiliary supply |
| VDDAUXx | Power to GPIO auxiliary supply |

**Notes:**

1. VDDA: This supply can be powered to 1.0V or 1.05V. For more information, see tables 4-2 in PolarFire FPGA Datasheet. This is a quiet supply for the device. One method is to use a Linear regulator to ensure the supply is quiet.
2. VDD: This supply can be powered to 1.0V or 1.05V. For more information, see tables 4-2 in PolarFire FPGA Datasheet.

VREFx: This is the reference voltage for DDR3 and DDR4 signals. The following VREF voltages can be generated internally and externally.

- Internal VREF: This is not subjected to PCB and package inductance and capacitance loss. These changes provide the highest performance and can be programmed as required by DDR controller.
- External VREF: This is fixed and cannot be programed as required. The PCB and package inductance and capacitance impact the VREF performance.

**Important:** If VDDI and VDDAUX need to be configured to the same voltage (2.5V or 3.3V), ensure both VDDI and VDDAUX are supplied from the same regulator. Do not use different regulators to source these rails. This prevents any voltage variations between VDDI and VDDAUX. In this case, the board must not supply the VDDI and VDDAUX from individual voltage supplies.

When a GPIO bank requires the VDDI to be less than 2.5V (1.2V, 1.5V, or 1.8V), the VDDAUX for that bank must be tied to 2.5V supply irrespective of the VDDI supply. The VDDI requires a separate supply for the specific I/O type (1.5V or 1.8V).

**Important:**

- The on-chip Power-on Reset circuitry requires the $V_{DD}$, $V_{DD18}$, and $V_{DD25}$ supplies to ramp monotonically from 0V to the minimum recommended operating voltage.
- You must initiate the I/O calibration only when both the VDDA and XCVR_VREF supplies are up.

For a detailed pin description, see PolarFire FPGA Packaging and Pin Descriptions User Guide.

### 1.1.1 PolarFire Decoupling Capacitors (Ask a Question)

The following tables list the requirement of all decoupling capacitors for different device variants and packages.

**Table 1-2.** Power-Supply Decoupling Capacitors[1]—MPF500T - FCG1152/FCG784 (1 mm)

| Pin Name | Ceramic | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|
| | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | — | 4 | — | — | — | — | 3 |
| VDD18 | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | 5 | — | — | 1 | — | — |
| VDDA | 3 | 1 | 6 | — | — | — | 2 | — |
| VDDA25 | — | — | 4 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | 2 | — | — | — | 1 | — |
| HSIO Bank[4] | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | 2 | — | — | — | — | — |

**Table 1-3.** Power-Supply Decoupling Capacitors[1]—MPF300T - FCG1152/FCG784/FCG484 (1 mm)

| Pin Name | Ceramic | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|
| | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | — | 4 | — | — | — | — | 2 |
| VDD18 | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | 5 | — | — | 1 | — | — |
| VDDA | 3 | 1 | 6 | — | — | — | 1 | — |
| VDDA25 | — | — | 4 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | 2 | — | — | — | 1 | — |

| .....continued | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Name | Ceramic | | | | | | | Tantalum |
| | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| HSIO Bank[4] | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | 2 | — | — | — | — | — |

**Table 1-4.** Power-Supply Decoupling Capacitors[1]—MPF300T/MPF200T/MPF100T/MPF050T - FCVG484 (0.8 mm)

| Pin Name | Ceramic | | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|---|
| | 1 nF | 2.2 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | — | — | 4 | 1 | — | — | — | 2 |
| VDD18 | — | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | — | 5 | — | — | 1 | — | — |
| VDDA | — | 2 | 2 | 1 | — | — | — | 1 | — |
| VDDA25 | 1 | — | — | 1 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | — | 2 | — | — | — | 1 | — |
| HSIO Bank[4] | — | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | — | 2 | — | — | — | — | — |

**Table 1-5.** Power-Supply Decoupling Capacitors[1]—MPF300T/MPF200T - FCSG536 (0.5 mm)

| Pin Name | Ceramic | | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|---|
| | 1 nF | 2.2 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | — | — | 4 | 1 | — | — | — | 2 |
| VDD18 | — | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | — | 5 | — | — | 1 | — | — |
| VDDA | 2 | 3 | 1 | 1 | — | — | — | 1 | — |
| VDDA25 | 1 | — | — | 1 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | — | 2 | — | — | — | 1 | — |
| HSIO Bank[4] | — | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | — | 2 | — | — | — | — | — |

**Table 1-6.** Power-Supply Decoupling Capacitors[1]—MPF200T - FCG784/FCG484 (1 mm)

| Pin Name | Ceramic | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|
| | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | 2 | 2 | — | — | — | — | 2 |
| VDD18 | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | 5 | — | — | 1 | — | — |
| VDDA | 3 | 1 | 6 | — | — | — | 1 | — |
| VDDA25 | — | — | 4 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | 2 | — | — | — | 1 | — |

| .....continued | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Name | Ceramic | | | | | | | Tantalum |
| | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| HSIO Bank[4] | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | 2 | — | — | — | — | — |

**Table 1-7.** Power-Supply Decoupling Capacitors[1]—MPF200T/MPF100T/MPF050T- FCSG325 (0.5 mm)

| Pin Name | Ceramic | | | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 nF | 2.2 nF | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | — | — | — | 4 | 1 | — | — | — | 2 |
| VDD18 | — | — | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | — | — | 5 | — | — | 1 | — | — |
| VDDA | — | 1 | 1 | 1 | 1 | — | — | — | 1 | — |
| VDDA25 | 1 | — | — | — | 1 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | — | — | 2 | — | — | — | 1 | — |
| HSIO Bank[4] | — | — | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | — | — | 2 | — | — | — | — | — |

**Table 1-8.** Power-Supply Decoupling Capacitors[1]—MPF100T - FCG484 (1 mm)

| Pin Name | Ceramic | | | | | | | | | Tantalum |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 nF | 2.2 nF | 4.7 nF | 10 nF | 0.1 µF | 1 µF | 4.7 µF | 10 µF | 47 µF | 330 µF |
| VDD | — | — | — | 2 | 2 | 1 | — | — | — | 1 |
| VDD18 | — | — | — | — | 2 | — | — | — | 2 | — |
| VDD25 | — | — | — | — | 5 | — | — | 1 | — | — |
| VDDA | — | — | 3 | 1 | 6 | — | — | — | 1 | — |
| VDDA25 | 1 | — | — | — | 4 | — | — | — | 1 | — |
| VDDIO3 | — | — | — | — | — | — | — | — | — | — |
| VDDAUXx[2] | — | — | — | — | 2 | — | — | — | 1 | — |
| GPIO Bank[3] | — | — | — | — | 2 | — | — | — | 1 | — |
| HSIO Bank[4] | — | — | — | — | 2 | — | — | — | 1 | — |
| VDD_XCVR_CLK | — | — | — | — | 2 | — | — | 1 | — | — |
| XCVR_VREF | — | — | — | — | 2 | — | — | — | — | — |

Decoupling capacitors other than those listed in the previous tables can be used if the physical sizes of capacitors meet or exceed the performance of the network given in this example. Substitution would require analyzing the resulting power distribution system's impedance versus frequency to ensure that no resonant impedance spikes the result. See Figure 1-1 for power supply design.

For more information about the internal package capacitance for power supplies associated with PolarFire packages, see section 2.4.2.1 section of PolarFire FPGA Packaging and Pin Descriptions User Guide.

The following table lists the required decoupling capacitors for PolarFire packages.

**Table 1-9.** Recommended Decoupling Capacitors For PolarFire Devices

| De-Cap Value | Part Number | Package | Description |
|---|---|---|---|
| 0.1 µF | GRM155R71C104KA88D | 0402 | For 1 mm package |

| .....continued | | | |
|---|---|---|---|
| De-Cap Value | Part Number | Package | Description |
| 10 nF | GRM15XR11C103KA86 | 0402 | For 1 mm package |
| 4.7 nF | GRM155R11H472KA01 | 0402 | For 1 mm package |
| 10 µF | GRM21BR71A106KE51 | 0805 | Bulk Caps (for 0.5, 0.8, and 1 mm) |
| 47 µF | GRM31CR61A476KE15 | 1206 | Bulk Caps (for 0.5, 0.8, and 1 mm) |
| 330 µF | T495D337K010ATE150 | 2917 | Bulk Caps (for 0.5, 0.8, and 1 mm) |
| 1 nF | GRM033R71C102KA01 | 0201 | For 0.8/0.5 mm package |
| 2.2 nF | GRM033R71A103KA01 | 0201 | For 0.8/0.5 mm package |
| 10 nF | GRM033R71A103KA01 | 0201 | For 0.8/0.5 mm package |
| 0.1 µF | GRM033C71C104KE14 | 0201 | For 0.8/0.5 mm package |

**Notes:**

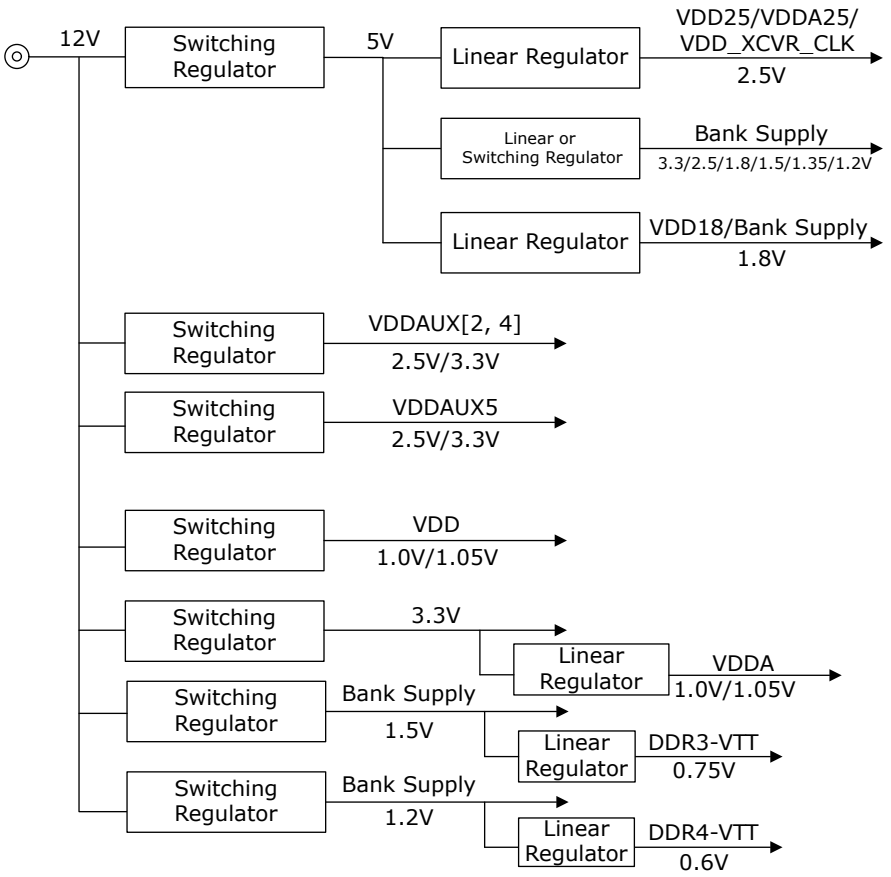
1. The guidelines are provided on how to effectively decouple only the FPGA device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the FPGA. Follow the recommended operational conditions as per PolarFire FPGA Datasheet.
2. Required Decoupling Capacitor for each VDDAUXx.
3. Required Decoupling Capacitor for each GPIO bank.
4. Required Decoupling Capacitor for each HSIO bank.

**Important:** The user can use equivalent capacitor values from a different vendor. For more information about Packaging Decoupling Capacitors, see PolarFire FPGA Packaging and Pin Descriptions User Guide.

### 1.1.2 Power-Supply Topology (Ask a Question)

PolarFire FPGAs require multiple power supplies. Figure 1-2 shows a power supply topology example for generating the required power supplies from a single 12V source. This example is based on the PolarFire MPF300-FCG1152 device with DDR3 and DDR4 interfaces.

**Figure 1-2.** Example Power-Supply Topology




The following table lists the suggested Microchip power regulators for PolarFire FPGA voltage rails.

**Table 1-10.** Power Regulators

| Voltage rail | Part Number | Description | Current |
|---|---|---|---|
| 5V | MIC24055YJL-TR | IC REG BUCK ADJ 12A SYNC 28QFN | 12A |
| VDD (1.0V) | MIC45212-2YMP-T1 | DC DC CONVERTER 0.8–5.5V 77W | 14A |
| VDDIO (3.3V) | MIC24055YJL-TR | IC REG BUCK ADJ 12A SYNC 28QFN | 12A |
| VCCIO_HPC_VADJ | MIC24046YFL-TR | IC REG BUCK PROG 5A SYNC 20VQFN | 5A |
| DDR4 (1.2V) | MIC23303YML-T5 | IC REG BUCK ADJ 3A SYNC 12DFN | 3A |
| DDR3 (1.5V) | MIC23303YML-T5 | IC REG BUCK ADJ 3A SYNC 12DFN | 3A |
| VDDAUX[2,4] | MIC23303YML-T5 | IC REG BUCK ADJ 3A SYNC 12DFN | 3A |
| VDDAUX5 | MIC23303YML-T5 | IC REG BUCK ADJ 3A SYNC 12DFN | 3A |
| VTT_DDR4 (0.6V) | MIC5166YML-TR | IC PWR SUP 3A HS DDR TERM 10MLF | 3A |
| VTT_DDR3 (0.75V) | MIC5166YML-TR | IC PWR SUP 3A HS DDR TERM 10MLF | 3A |
| VDDIO (1.8V) | MIC24046YFL-TR | IC REG BUCK PROG 5A SYNC 20VQFN | 5A |
| VDDA (1.0V) | MIC69502WR | IC REG LINEAR POS ADJ 5A SPAK-7 | 5A |
| VDD25, VDDA25, VDD_XCVR_CLK | MIC69502WR | IC REG LINEAR POS ADJ 5A SPAK-7 | 5A |
| VDD18 | MIC69502WR | IC REG LINEAR POS ADJ 5A SPAK-7 | 5A |

### 1.1.3 Unused Power Supply (Ask a Question)

Figure 1-3 shows how power supplies may be configured when not in use and also to reduce leakage and power for the system.

**Figure 1-3.** Option 1 for unused Connections

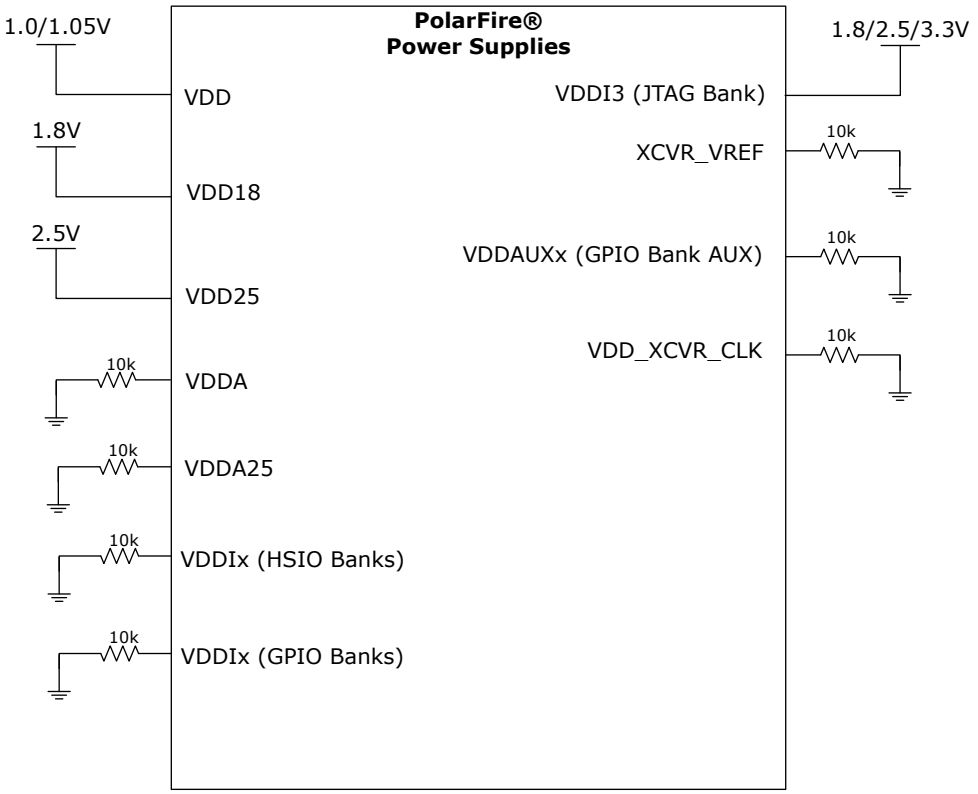
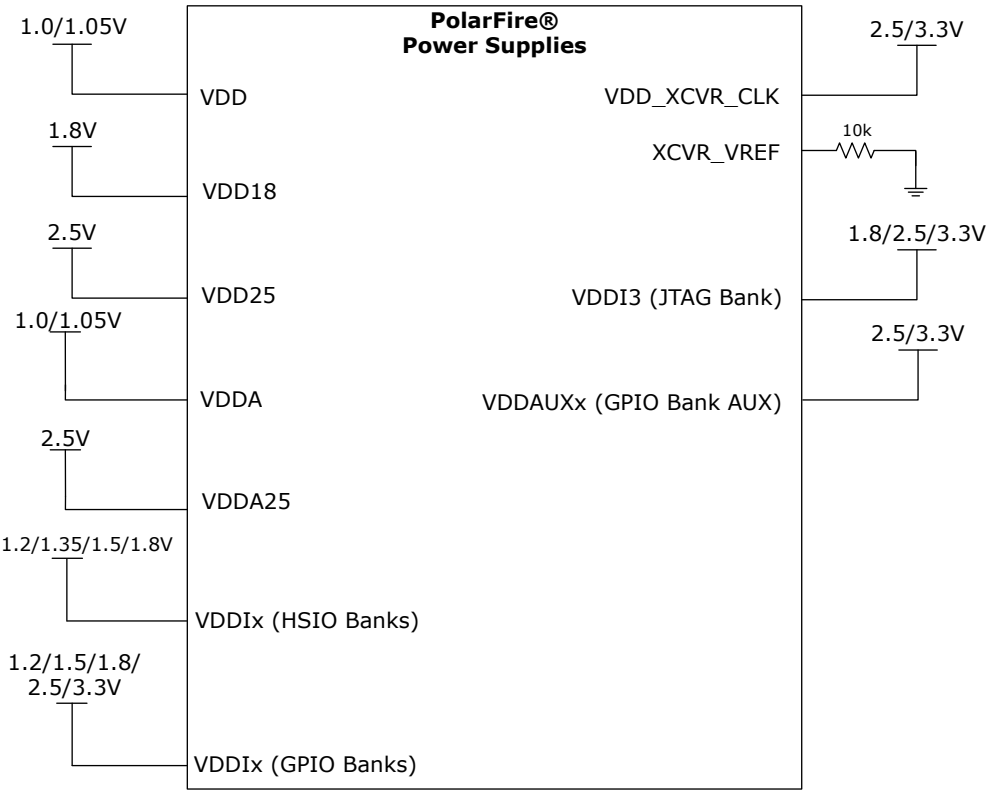



Figure 1-4 also shows the power configuration of unused supplies. This option can be used when there is an intent to power-up the various supplies at a later time in the system and the I/Os are not being used.

**Figure 1-4.** Option 2 for Unused Connections




**Important:** To simplify the board-level routing, multiple 10 kΩ resistors can be used as required or the power supplies can also be grouped into a single 10 kΩ resistor and tied-off to VSS.

### 1.1.4 Pin Assignment Tables (Ask a Question)

The Packaging Pin Assignment Table (PPAT) is available on the PolarFire FPGA Documentation web page. PPAT contains information about the recommended DDR pin-outs, PCI EXPRESS capability for XCVR-0, DDR Lane information for IO CDR, generic IOD interface pin placement, and unused condition for package pins.

## 1.2 I/O Glitch (Ask a Question)

A glitch might occur during power-up or power-down for GPIO/HSIO outputs in PolarFire devices. Glitch can occur before or after the device reaches a functional state. These glitches are not observed on LVDS outputs or Transceiver I/Os. No reliability issues are caused by either of the glitch types. There are three types of glitch that can occur:

- Parasitic glitches may occur for GPIOs or HSIOs before the device reaches functional state with a maximum glitch of 1V with a 0.4 ms width. This type of glitch can typically be ignored. It is recommended to use a 100K pull-down resistor on critical signals[1] of the GPIO or HSIO pins if this type of glitch cannot be ignored. No glitches are observed once mitigation recommendations are placed. This may occur for both erased/blank and programmed units.

[1] Critical outputs like Reset or Clock of the HSIO or GPIOs going into another device.

- Another type of glitch may occur on GPIOs and HSIOs during power-on sequencing or boot-up. This is due to a weak pull-up resistor being enabled by default on an input, output or bidirectional I/O. To mitigate this glitch, use the Libero SoC I/O Editor or PDC constraint to program a weak pull-down on the output buffer on the specified I/O. This may occur for both erased/blank and programmed units.
- The last type of glitch may occur after the device reaches functional state and may occur for both erased/blank and programmed units. This type of glitch is related to the power-up and power-down sequence of VDDI and VDDAUX supplies. This occurs only on GPIOs where the VDDI is 1.5V or 1.8V only with a maximum glitch of 1V with a 0.8 ms width during power-up and a maximum glitch of 1.8V with a 1 ms width during power-down. For HSIOs, where the VDDI is 1.5V or 1.8V only a maximum glitch of 600 mV and 1.5 ms width may occur at Power-Up and a maximum glitch of 220 mV 200 µs width may occur at Power-Down.

To mitigate the post functional state glitch, follow the recommendations in the following table.

**Table 1-11.** Power Sequencing[1] (For GPIO)

| Use Cases for GPIO | | Power-up Sequencing Requirement for Mitigating Glitches[2] | Power-down Sequencing Requirements for Mitigating Glitches[2] |
|---|---|---|---|
| VDDI | VDDAUX | | |
| 1.2V | 2.5V | No glitch occurs | No glitch occurs |
| 1.5V | 2.5V | Power up VDDAUX before VDDI of that bank | • Power down VDDI before or in concurrence with VDDAUX<br>• Power down VDDI before VDD or VDD25 |
| 1.8V | 2.5V | Power up VDDAUX before VDDI of that bank | • Power down VDDI before or in concurrence with VDDAUX<br>• Power down VDDI before VDD or VDD25 |
| 2.5V | 2.5V | Power up VDDAUX and VDDI from the same Regulator | No glitch occurs |
| 3.3V | 3.3V | Power up VDDAUX and VDDI from the same Regulator | No glitch occurs |

**Table 1-12.** Power Sequencing[1] (For HSIO)

| Use Cases for HSIO | | Power-up Sequencing Requirement for Mitigating Glitches[2] | Power-down Sequencing Requirements for Mitigating Glitches[2] |
|---|---|---|---|
| VDDI | VDD18 | | |
| 1.2V | 1.8V | No glitch occurs | No glitch occurs |
| 1.5V | 1.8V | Power up VDD18 before VDDI of that bank | Power down VDDI before VDD18, VDD, and VDD25 |
| 1.8V | 1.8V | Power up VDD18 before VDDI of that bank[3] | Power down VDDI before VDD18, VDD, and VDD25 |

**Notes:**

1. No glitches are observed once mitigation recommendations are placed.
2. The preceding power sequence does not mitigate any parasitic glitches. Add a 100K pull-down resistors to critical signals of GPIO or HSIO pins for mitigation of parasitic glitches.
3. When VDDI = 1.8V and VDD18 = 1.8V, VDDI and VDD18 must be sourced from two separate power sources to meet the power sequencing requirements described in Table 1-12. This mitigates any potential I/O glitch.

**Important:** A glitch might occur on GPIO pins during JTAG programming, if power is disrupted. The glitch can be mitigated by powering down VDDI before VDDAUX, VDD, and VDDI3.

## 1.3 User I/O (Ask a Question)

PolarFire FPGAs have two types of I/O buffers: HSIO and GPIO. HSIO buffers are optimized for single-ended buffers with supplies from 1.2V to 1.8V. GPIO buffers support single-ended and true differential interfaces with supplies from 1.2V to 3.3V.

**Important:** When the HSIO bank is configured as an LVDS receiver, the concerned I/Os must be connected externally by a 100Ω resistor.

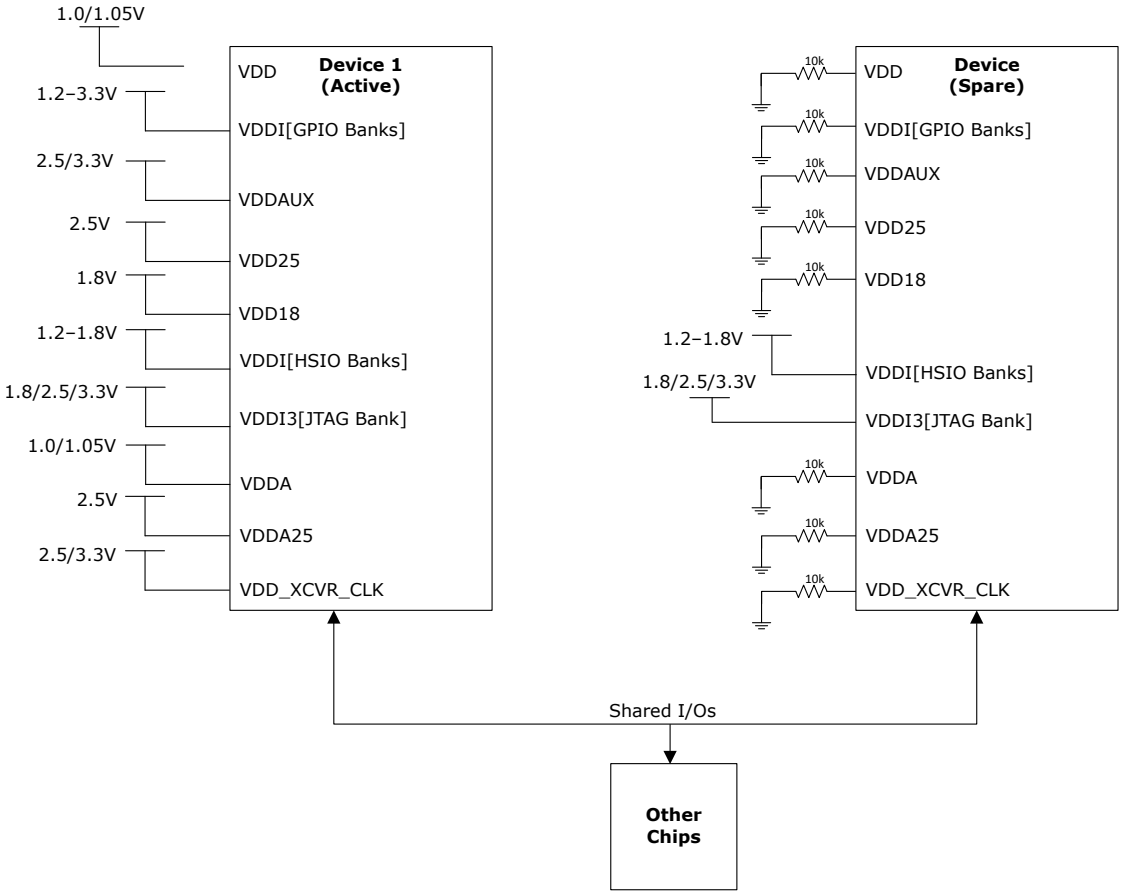
For more information about key features of I/O buffers and supported standards, see PolarFire FPGA Packaging and Pin Descriptions User Guide and PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide.

### 1.3.1 Cold Sparing (Ask a Question)

PolarFire devices support cold sparing for GPIO and HSIO. Cold sparing is implemented by connecting the devices as shown in the following figure. The system board has two PolarFire devices in parallel and the devices share I/O. The spare device has its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes. As a result, low power and a protected state for the spare device is established. The spare device can be changed to active device by powering-up all the supplies. The active device can be changed to spare device by powering down all the supplies except HSIO VDDI banks.

A typical cold sparing application integrates two parallel devices with shared I/O connections, as shown in the following figure.

**Figure 1-5.** Cold Sparing




**Important:** Transceiver pins do not support the cold sparing feature.

### 1.3.2 Hot Socketing (GPIO Only) (Ask a Question)

Hot socketing (also known as hot swapping or hot plug-in) prevents damage to the PolarFire FPGA if, at any time, voltage is detected at I/O while the device is powered off. It also helps prevent disruptions that might occur in the rest of the system if the I/O of a device are connected without a valid power supply.

Only GPIOs support hot socketing. In hot socketing, GPIOs are in high-impedance (hi-Z) state.

The GPIO maintains the following high-impedance state until the power supplies are at a valid state.

- VDDAUx is greater than or equal to 1.6V
- VDDIx is greater than or equal to 0.8V
- VDD and VDD25 are both high and the PolarFire FPGA controller has asserted the global I/O ring signal (IO_EN)

**Important:** TMS, TDI, TRSTB, DEVRST_N, and FF_EXIT_N do not support hot socketing.

#### 1.3.2.1 Over-Voltage Tolerance for GPIO (Ask a Question)

If GPIO is configured with the following settings, GPIO supports over-voltage tolerance, ensuring that the I/O signal at the pad is at a higher potential than the VDDIx power supply.

**Table 1-13.** Over-Voltage Tolerance

| Standard | OE | Clamp Diode | VREF (Input) | Weak Pull-Up/ Pull-Down | Termination | Hot-plug |
|---|---|---|---|---|---|---|
| PCI | x | ON | ON | ON | ON | Disabled |
| GPIO | 1 | ON | ON | ON | ON | Disabled |
| | 0 | OFF | OFF | OFF | OFF | Enabled |

For recommended operating conditions about over-voltage tolerance, see PolarFire FPGA Datasheet.

## 1.4 Clocks (Ask a Question)

PolarFire devices offer two on-chip RC oscillators (one 2 MHz and one 160 MHz) to generate free-running clocks. The clocks do not have any I/O pads and do not require external components to operate.

The following table lists the number of RC oscillators available in PolarFire devices.

**Table 1-14.** RC Oscillator Count

| Resource | Supported Range (MHz) | MPF100 | MPF200 | MPF300 | MPF500 |
|---|---|---|---|---|---|
| On-chip oscillator | 2 | 1 | 1 | 1 | 1 |
| | 160 | 1 | 1 | 1 | 1 |

Users need to understand the regional clock implications when targeting designs that might be migrated to different device sizes. It is important that users go through the pin planning before finalizing it on the board while targeting a Die. For more information about clocking in PolarFire devices, see PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide.

For information about the preferred clock inputs connectivity to PLLs, DLLs, and global clock network, see the Packaging Pin Assignment Table (PPAT).

## 1.5 Reset (Ask a Question)

For designing a robust system users may use the dedicated DEVRST_N pin or a general purpose reset signal using any GPIO/HSIO as a global system level reset.

For the following cases, users may use the DEVRST_N as a warm reset for the device:

- A user design modifies auto-initialized fabric RAMs or PCIe configuration during operation.
- A user design is using PCIe, transceivers, or user crypto.

For all other use cases, it is recommended to use a general purpose reset signal using any GPIO/ HSIO IO because they take much shorter time for design to come out of reset.

If the dedicated DEVRST_N is not used for warm resets, the DEVRST_N pin must be configured using one of the following methods:

- Drive the signal with a POR chip or an external device and keep the DEVRST_N asserted till the system/clocks are stable and the chip is properly powered up.
- Connect DEVRST_N to VDDI3 through a 1 kΩ resistor per pin without sharing with any other pins.

– In this case, the user needs to ensure that all clocks going to the device are stable before the user design is released from Power-on Reset. The details of the minimum time taken for the fabric design to be activated after power-on is specified in the PolarFire Datasheet (Power-Up To Functional section).

## 1.6 DDR (Ask a Question)

PolarFire devices support DDR3, DDR3L, LPDDR3, and DDR4. For more information about the DDR support in PolarFire devices, see PolarFire FPGA Datasheet.

The reliability of the DDR interface depends on the quality of the layout. For detailed information on board layout and routing, see PolarFire FPGA and PolarFire SoC Memory Controller User Guide.

## 1.7 Device Programming (Ask a Question)

The PolarFire device is programmed using one of the two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- JTAG programming
- SPI Master mode programming
- SPI Slave mode programming

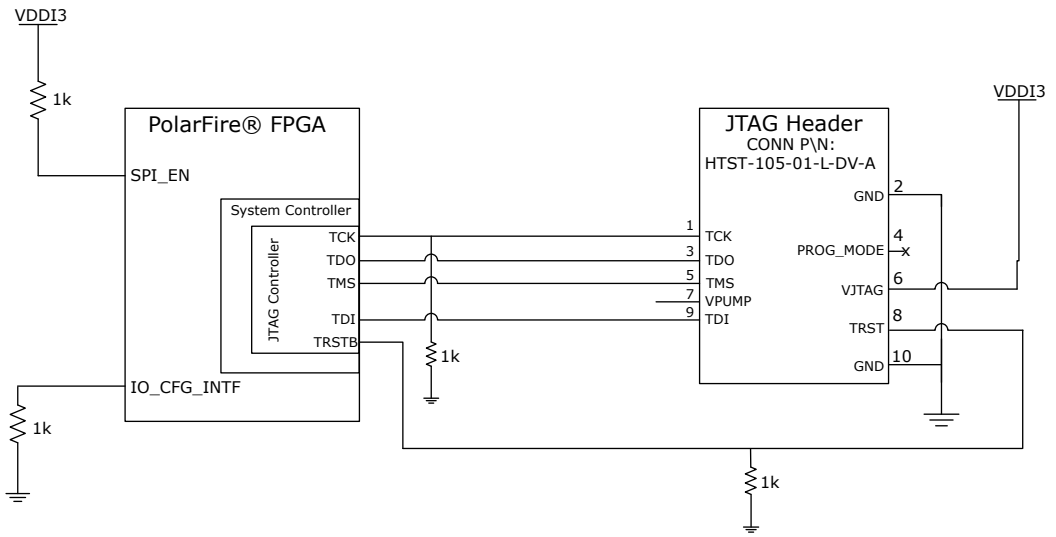
The PolarFire FPGA supports programming modes through the internal system controller using SPI Master mode, or an external Master using JTAG or SPI interfaces. For detailed information on hardware connections for each programming mode, see PolarFire FPGA and PolarFire SoC FPGA Programming User Guide.

### 1.7.1 JTAG Programming (Ask a Question)

The JTAG interface is used for device programming and testing, or for debugging firmware. When the device reset (DEVRST_N) is asserted, JTAG I/Os are not accessible. JTAG I/Os are powered by Bank 3 VDDI.

The following illustration shows the board-level connectivity for JTAG programming mode in PolarFire devices.

**Figure 1-6.** JTAG Programming




The following table lists the JTAG pin names and descriptions.

**Table 1-15.** JTAG Pins

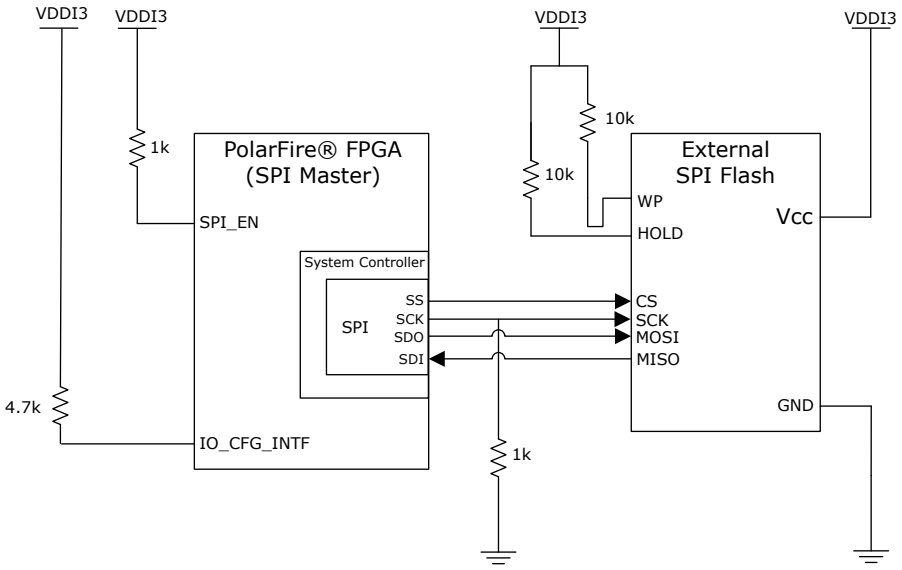
| Pin Names | Direction | Unused Condition | Description |
|---|---|---|---|
| TMS | Input | DNC | JTAG test mode select. |
| TRSTB | Input | Must be connected to VDDI3 through a 1 kΩ resistor | JTAG test reset. Must be held low during device operation. |
| TDI | Input | DNC | JTAG test data in. |
| TCK | Input | Must be connected to VSS through a 10 kΩ resistor | JTAG test clock. |
| TDO | Output | DNC | JTAG test data out. |

### 1.7.2 SPI Master Mode Programming (Ask a Question)

The embedded system controller contains a dedicated SPI block for programming, which can operate in Master or Slave mode. In Master mode, the PolarFire device interfaces are used to download programming data through the external SPI Flash. In Slave mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

The following illustration shows the board-level connectivity for SPI Master mode programming in PolarFire devices.

**Figure 1-7.** SPI Master Mode Programming




The following table lists the SPI Master mode programming pins.

**Table 1-16.** SPI Master Mode Programming Pins

| SPI Pin Name | Direction | Unused Condition | Description |
|---|---|---|---|
| SCK | Bidirectional | Connect to VSS through a 10 kΩ resistor | SPI clock[1]. |
| SS | Bidirectional | Connect to VSS through a 10 kΩ resistor | SPI slave select[1]. |

| .....continued | | | |
|---|---|---|---|
| **SPI Pin Name** | **Direction** | **Unused Condition** | **Description** |
| SDI | Input | Connect to VDDI3 through a 10 kΩ resistor | SDI input[1]. |
| SDO | Output | DNC | SDO output[1]. |
| SPI_EN | Input | Connect to VSS through a 10 kΩ resistor | SPI enable.<br>0: SPI output tri-stated<br>1: Enabled<br>Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O. |
| IO_CFG_INTF | Input | Connect to VSS through a 10 kΩ resistor | SPI I/O configuration.<br>0: SPI Slave interface<br>1: SPI Master interface<br>Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a Master or Slave. |

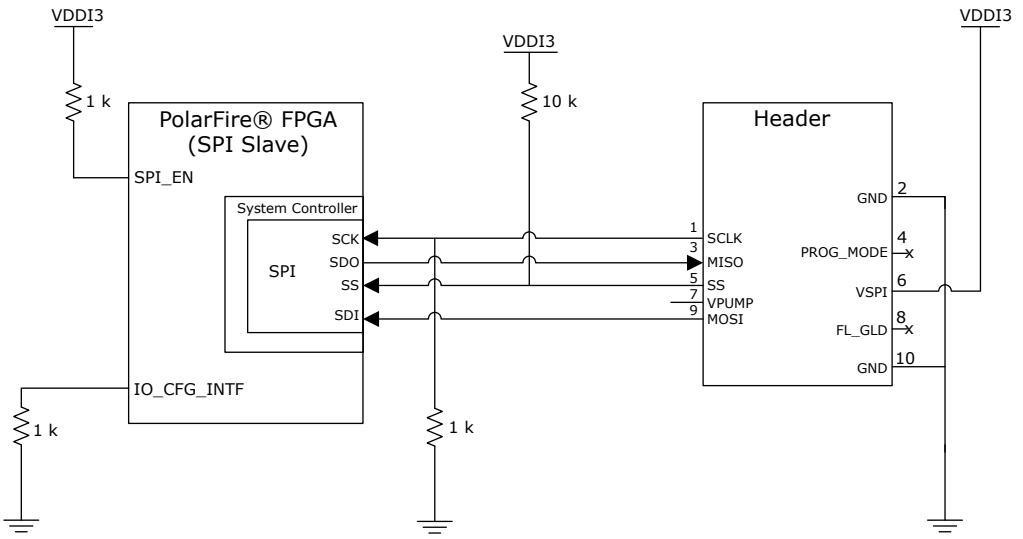
**Note:**

1. The SCK, SS, SDI, and SDO pins are shared between the system controller and the FPGA fabric. When the system controller's SPI is enabled and configured as a master, the system controller hands over the control of the SPI to the fabric (after device power-up).

### 1.7.3 SPI Slave Mode Programming (Ask a Question)

The following illustration shows the board-level connectivity for SPI slave mode programming in PolarFire devices.

**Figure 1-8.** SPI Slave Mode Programming




### 1.7.4 Special Pins (Ask a Question)

For information about special pins, see Table 13 of PolarFire FPGA Packaging and Pin Descriptions User Guide.

## 1.8 Transceiver (Ask a Question)

The following table lists the transceiver features supported in PolarFire devices, and transceiver blocks are located on the east corner of the device. PolarFire devices support PCIe interface only in Transceiver quad 0.

For more information about implementing PCIe interfaces, see PolarFire FPGA and PolarFire SoC FPGA PCI Express User Guide. For more information about implementing other transceiver based interfaces and power supplies, see PolarFire Family Transceiver User Guide.

The following table lists the number of transceivers supported in various PolarFire devices.

**Table 1-17.** Transceiver Support in PolarFire Devices

| Device | Transceiver Lane | TX PLL | Reference Clock I/O |
|---|---|---|---|
| MPF100 | 8 | 6 | 12 |
| MPF200 | 16 | 11 | 22 |
| MPF300 | 16 | 11 | 22 |
| MPF500 | 24 | 15 | 30 |

For more information about supported I/O standards, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide.

### 1.8.1 Reference Clock (Ask a Question)

A transceiver reference clock is delivered to each transmit PLL for transmit functions and to each receiver lane for receive Clock Data Recovery (CDR).

#### 1.8.1.1 Transceiver Reference Clock Requirements (Ask a Question)

The following are the requirements for the transceiver reference clock:

- Ensure the following when differential clock input is provided to the reference clock:
  - ODT must be enabled for transceiver reference clock pins.
  - Must be within the range of 20 MHz to 400 MHz.
- Must be within the tolerance range of I/O standards. The reference input buffer is provided and is expected to support these input standards directly without external components on the board. The reference I/O standards such as LVCMOS25, SSTL18, LVDS25, and HCSL25 are supported. For more information, see PolarFire Family Transceiver User Guide.

See the *PCI Express Base specification Rev 2.1* for detailed PHY specifications. Also, see the *PCIe Add-in Card Electro-Mechanical (CEM)* specifications.

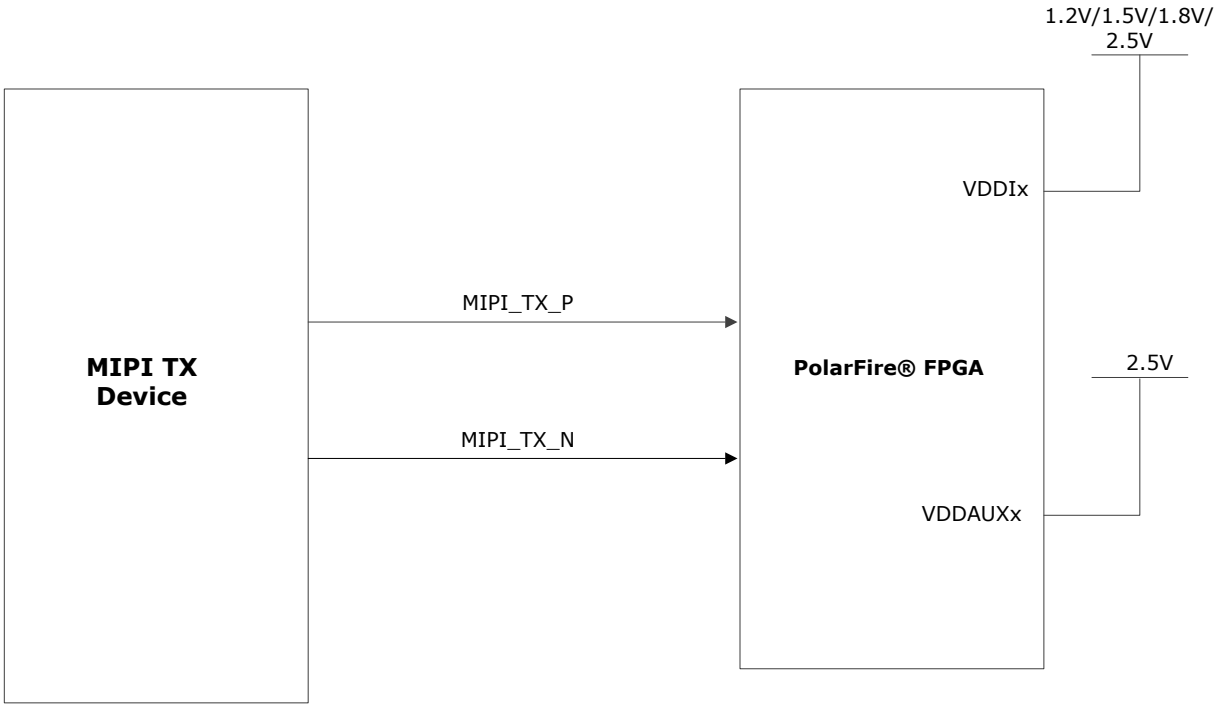
## 1.9 MIPI Hardware Design Guidelines (Ask a Question)

The following sections discuss the guidelines for MIPI RX and TX interface with PolarFire device.

### 1.9.1 MIPI RX (Ask a Question)

The MIPI RX is supported only in GPIO Bank. The corresponding Bank voltage (VDDI) and VDDAUX voltage must be connected as shown in the following figure.

**Figure 1-9.** MIPI RX Connection




Following is the list of MIPI RX signal connections:

- Four data and clock must be within one DDR_Lane.
- Connect the data signals to adjacent DDR_Lanes, if more than four data signals are available.
- The MIPI RX clock must be connected to a CLKIN pin.

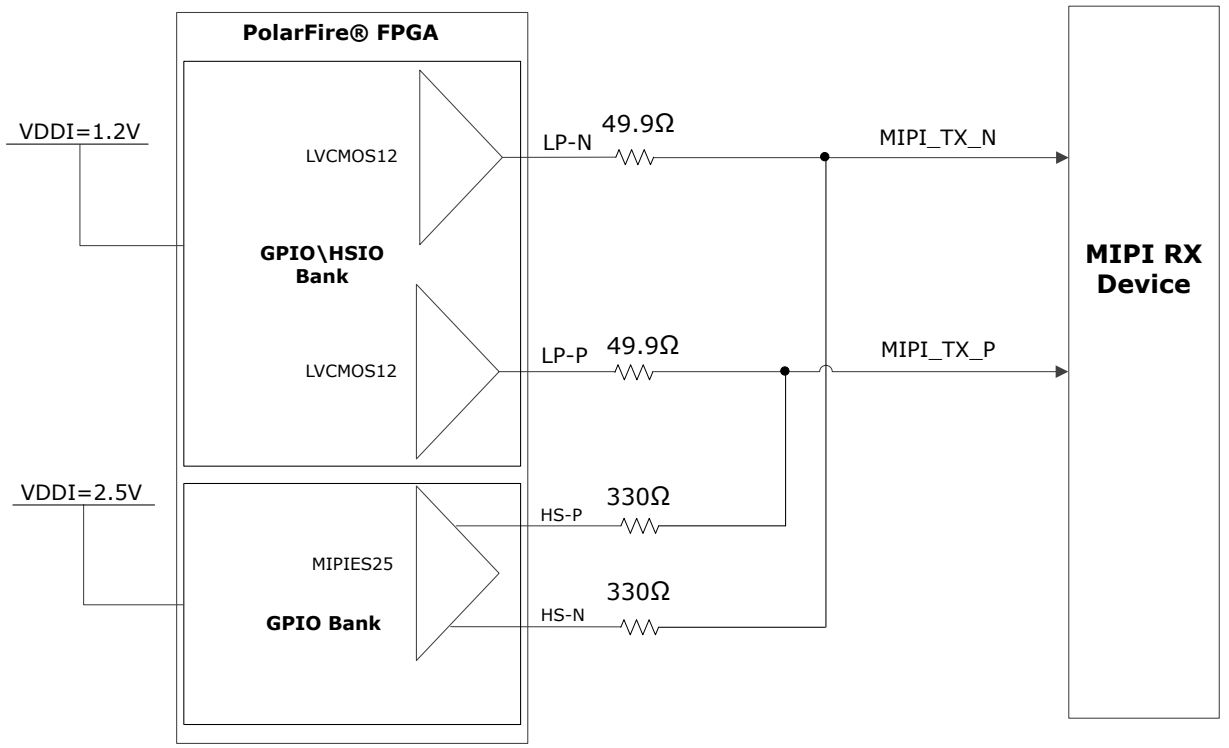
For more information about DDR_Lane, see the Package Pin Assignment Tables (PPAT).

### 1.9.2 MIPI TX (Ask a Question)

The MIPI LP (Low Power) signals must be connected to a 1.2V GPIO/HSIO Bank supply and High-speed signals must be connected to a 2.5V GPIO Bank supply. Select the High Speed (HS) and Low Power (LP) pins in adjacent pins to minimize the LP stub. The HS data and clock signals must be in one DDR_Lane. For more information about DDR_Lane information, see the Package Pin Assignment Tables (PPAT).

The MIPI TX standard is implemented by using the resistor divider network for LP and HS signals, as shown in the following figure. The resistor values mentioned in the following provide a throughput upto of 1 Gbps.

**Figure 1-10.** MIPI TX Connections




**Important:** Run the PDC verification in the Libero tool before moving to layout. For more information about MIPI RX electrical characteristics, see PolarFire FPGA Datasheet.

For information about the MIPI layout guidelines, see 3.1. MIPI.

## 1.10 AC and DC Coupling (Ask a Question)

Each transmit channel of a PCIe lane must be AC-coupled to allow the link detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops when the data signal contains a long string of consecutive identical bits. For non-PCIe applications, Microchip recommends that a PolarFire device receives inputs that are AC-coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 µF) for AC-coupling capacitors must be used to maximize link signal quality and must conform to PolarFire FPGA Datasheet electrical specifications.

For lower data rates as per the data sheet, DC coupling is supported by PolarFire Transceiver TX and RX interfaces through a configuration option. If a PolarFire transmitter is used to drive a PolarFire receiver in DC-coupled mode, select the lowest common mode setting for the transmitter.

## 1.11 Brownout Detection (Ask a Question)

The PolarFire FPGA functionality is guaranteed only if VDD is above the recommended level specified in the Datasheet. Brownout detection occurs when VDD drops below the minimum recommended operating voltage. When this occurs, the device operation may not be reliable. The design might continue to malfunction even after the supply is brought back to the recommended values because parts of the device might have lost functionality during brownout. The VDD supply is protected by a built-in brownout detection circuit.

# 2. Board Design Checklist (Ask a Question)

This chapter provides a set of hardware board design checks for designing hardware using Microchip® PolarFire FPGAs. The checklists provided in this chapter are a high-level summary checklist to assist the design engineers in the design process.

## 2.1 Prerequisites (Ask a Question)

Ensure that you have gone through the following chapters before reading this chapter:

- Introduction
- 3. Appendix: General Layout Design Practices

This checklist is intended as a guideline only. The PolarFire family consists of FPGAs ranging from densities of 100K to 500K Logic Elements (LEs).

## 2.2 Design Checklist (Ask a Question)

The following table lists the various checks that design engineers must take care while designing the system.

**Table 2-1.** Design Checklist

| Guideline | Yes/No | Remarks |
|---|---|---|
| **Prerequisites** | | |
| See PolarFire FPGA Datasheet<br>See UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide | | |
| See the board-level schematics of PolarFire Evaluation Kit. | | |
| **Device Selection** | | |
| Check for available device variants for PolarFire FPGA.<br>Select a device based on I/O pin count, transceivers, package, phase-locked loops (PLLs), and speed grade. | | |
| Check device errata in PolarFire Documentation. | | |
| **Design Checklist** | | |
| **Power Analysis**<br>Download the PolarFire Power Estimator and check for the power budget. | | |
| **Power Supply Checklist**<br>See 1.1. Power Supplies for used power rails, and Figure 1-3 and Figure 1-4 for unused rails. | | |
| **Decoupling Capacitors**<br>Follow 1.1.1. PolarFire Decoupling Capacitors. Perform PI Analysis for any deviation from the recommended capacitors. | | |
| **Clocks** | | |
| For more information about dynamic phase shift ports, see the “Dynamic Phase Shift Ports” table in PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide.<br>The XCVR reference clock ranges from 20 MHz to 400 MHz. | | |

| .....continued | | |
|---|---|---|
| **Guideline** | **Yes/No** | **Remarks** |
| The global clock network is driven by any of the following:<br>• Preferred clock inputs (CLKIN_z_w)<br>• On-chip oscillators<br>• CCC (PLL/DLL)<br>• XCVR interface clocks<br>For information about the preferred clock inputs connectivity to PLLs, DLLs, and global clock network, see the Packaging Pin Assignment Table (PPAT).<br>**High-Speed I/O Clocks**<br>High-speed I/O clock networks are driven by I/O or CCCs. The high-speed I/O clocks feed reference clock inputs of adjacent CCCs through hardwired connections.<br>**CCC**<br>The CCC is configured to have a PLL or DLL clock output, driving a high-speed I/O clock network. | | |
| Global Buffer (GB) is driven through the dedicated global I/O, CCC, or fabric (regular I/O) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets.<br>A dedicated global I/O drives the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network.<br>For more information about global clock network, see PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide. | | |
| **Reset** | | |
| For more information about DEVRST_N and user reset, see 1.5. Reset. | | |
| **DDR Interface** | | |
| For more information about DDR routing and topology, see PolarFire FPGA and PolarFire SoC Memory Controller User Guide. | | |
| Check Programming and Debugging Scheme.<br>For programming and debugging information, see 1.7. Device Programming. | | |
| **XCVR** | | |
| For more information about XCVR, see PolarFire Family Transceiver User Guide. | | |
| See the bank location diagrams in the PolarFire FPGA Packaging and Pin Descriptions User Guide to assess the preliminary placement of major components on PCB. | | |
| **IOD** | | |
| For I/O gearing interfaces, place the clocks and data based on the defined requirements by selecting the correct I/O. For more information about the placement of User I/O, see PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide. | | |
| See the information about implementing Generic IOD Interface in PolarFire FPGA and PolarFire SoC FPGA User I/O User Guide. | | |
| See the Consolidated IOD Rules for pre-place and route guidance. | | |

## 2.3 Layout Checklist (Ask a Question)

The following table provides the layout checklist.

**Table 2-2.** Layout Checklist

| Guideline | Yes/No |
|---|---|
| **Power** | |
| Are the 0402 or lesser size capacitors used for all decapacitors? | |
| Is the required copper shape provided to core voltage? | |
| Are the required copper shape and sufficient vias provided to voltages? | |

| .....continued | |
|---|---|
| **Guideline** | **Yes/No** |
| Are VREF planes for the DDRx reference supply isolated from the noisy planes? | |
| Are sufficient number of decoupling capacitors used for the DDRx core and VTT supply? | |
| Is one 0.1 µF capacitor for two VTT termination resistors used for DDRx? | |
| Is the VTT plane width sufficient? | |
| **DDR Memories** | |
| Are the length-match recommended by the vendor followed for DDR memories? | |
| **XCVR** | |
| Are the length-match recommendations for XCVR followed? | |
| Are DC blocking capacitors required for PCIe interface? | |
| Is tight-controlled impedance maintained along the XCVR traces? | |
| Are differential vias well designed to match XCVR trace impedance? | |
| Are DC blocking capacitor pads designed to match XCVR trace impedance? | |
| **Dielectric Material** | |
| Is proper PCB material selected for critical layers? | |

# 3. Appendix: General Layout Design Practices (Ask a Question)

This chapter provides guidelines for the hardware board layout that incorporates PolarFire devices. Good board layout practices are essential to achieve the expected performance from PCBs and PolarFire devices. They help achieve high-quality and reliable results such as low-noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This chapter is intended for the readers who are familiar with the PolarFire FPGA chip, experience in digital board layout, and know about line theory and signal integrity.

## 3.1 MIPI (Ask a Question)

This section discusses the MIPI RX and TX guidelines.

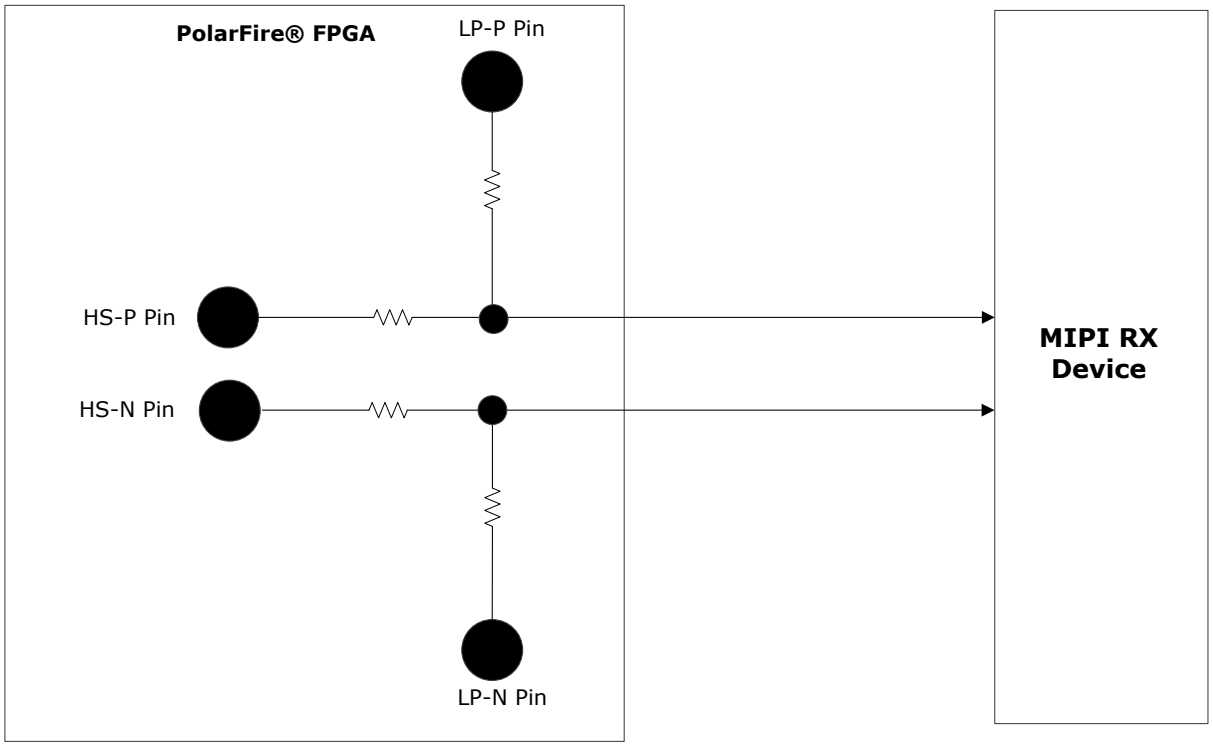
### MIPI RX Layout Guidelines

The data and clock must be matched within 20 mils in PCB.

### MIPI TX Layout Guidelines

As shown in Figure 3-1, the LP and HS resistors must be close to the PolarFire device pin. The HS signals must be routed to LP resistors to minimize the LP signals PCB stub length. The LP signals stub must be less than 500 mils. The data lane and clock must be length matched within 20 mils. 8 inches is the maximum length supported.

**Figure 3-1.** MIPI TX Layout




## 3.2 Transceiver (Ask a Question)

Collateral material of the PolarFire FPGA transceiver enables the system implementation easier for the designer by providing the system solution. Transceivers are high-speed serial connectivity with built-in, multi-gigabit, and multi-protocol transceivers from 250 Mbps to 12.7 Gbps. For these transceiver-based interfaces, the system designer must be familiar with the industry specifications,

transceivers technology, or RF/microwave PCB design. However, the PCB design is evaluated by a knowledgeable high-speed digital PCB designer.

### 3.2.1 Layout Considerations (Ask a Question)

This section describes differential traces and skew matching, which must be taken care while designing the PCB layout.

#### 3.2.1.1 Differential Traces (Ask a Question)

A well-designed differential trace must have the following qualities:

- No Mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points must be considered while routing the high-speed differential traces to meet the previous qualities.

- The traces must be routed with tight length matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals in Common Mode Signals.
- The differential pair must be routed such that the skew within the differential pairs is less than 5 mils. The length match must be used by matching techniques.

#### 3.2.1.2 Skew Matching (Ask a Question)

The length of differential lanes must be matched within the TX and RX group. This applies only to specific protocols such as XAUI.

Differential pairs must be routed symmetrically in-to and out of structures, as shown in Figure 3-3.

The following figure shows the skew matching.

**Figure 3-2.** Skew Matching

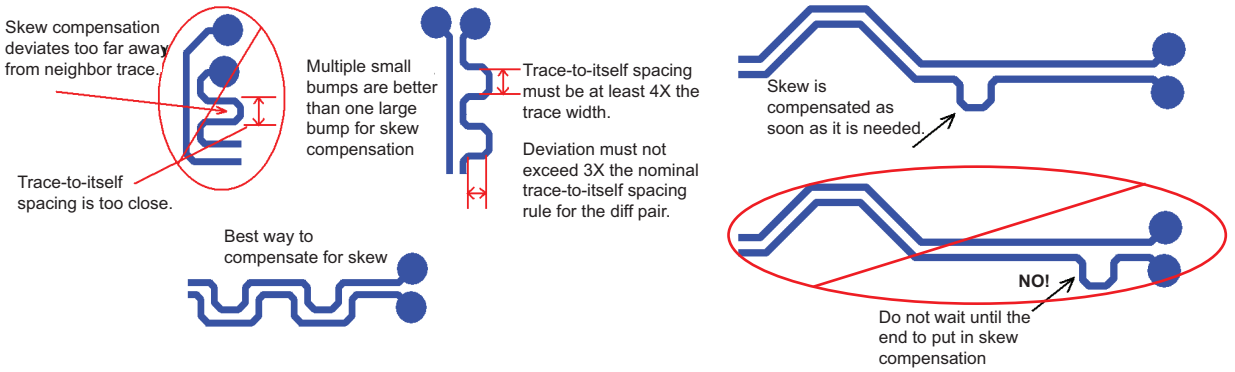



**Figure 3-3.** Example of Asymmetric and Symmetric Differential Pairs Structure

Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace must be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To minimize dielectric loss, use low Dissipation Factor (DF) PCB materials such as Nelco 4000-13EP SI. Cost is significantly higher than FR4 PCB material, but FR4 PCB material cannot provide increased eye-opening when longer trace interconnections are required. Ensure that a 85–100 Ω differential impedance is maintained. This is an important guideline to be followed if the data rate is 5 Gbps or higher.

Far end crosstalk is eliminated by using stripline routing. However, this type of routing in stripline causes more dielectric loss. In order to minimize dielectric loss, it is better to route as a microstrip if there is enough space between differential pairs (>4 times the width of the conductor). Simulations are recommended to see the best possible routing.

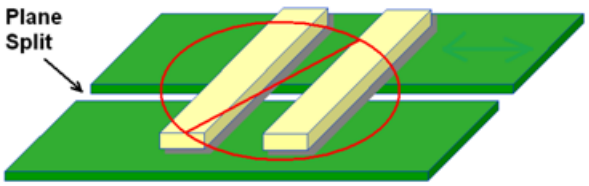
Instruct the fabrication vendor to use these PCB materials before manufacturing.

Transceiver traces must be kept away from the aggressive nets or clock traces. For example, on MPF300 devices, the transceiver and DDR traces must not be adjacent to each other. Trace stubs must be avoided.

It is recommended to use low roughness, that is, smooth copper. As the speed increases, insertion loss due to the copper roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. Microchip recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

Split reference planes must be avoided. Ground planes must be used for reference for all transceiver lanes.

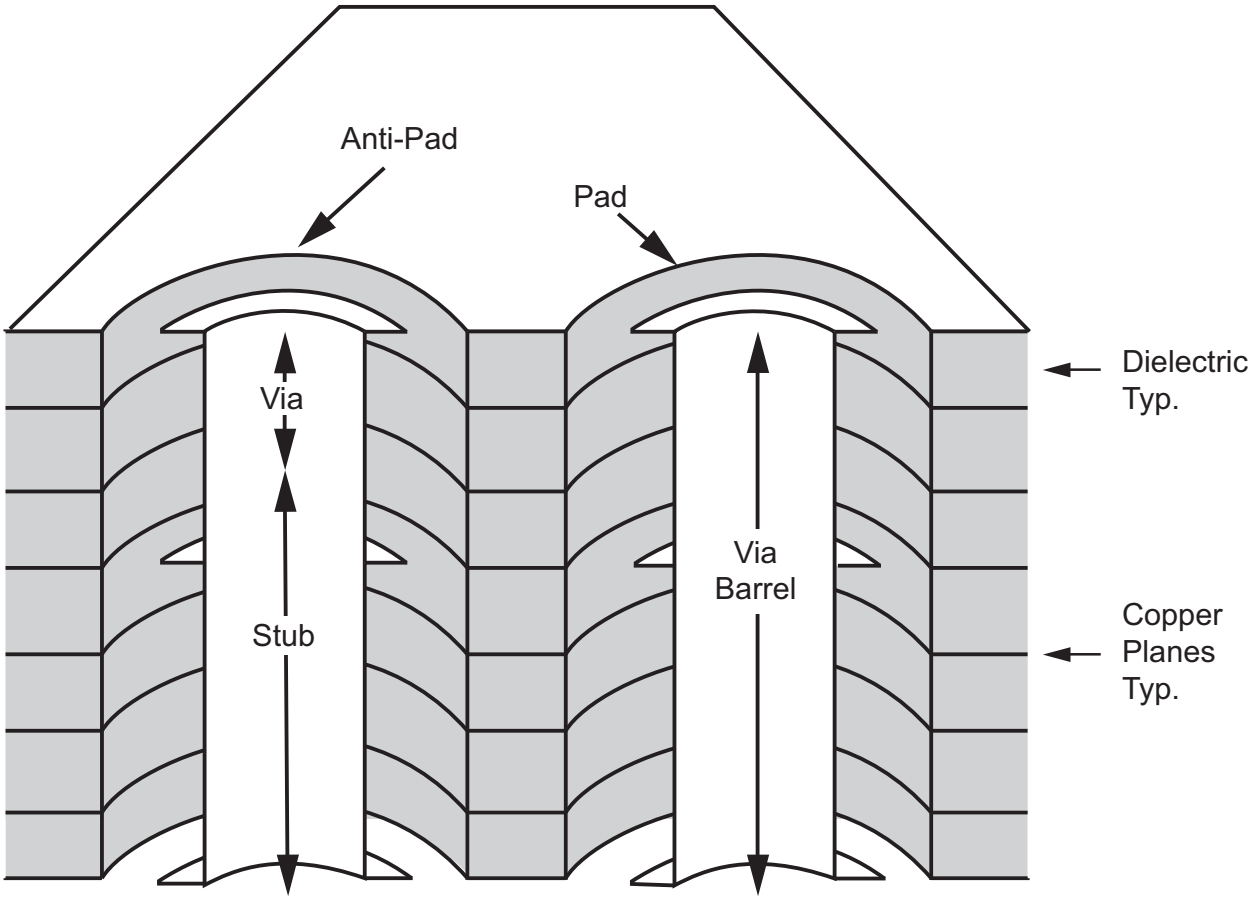
**Figure 3-4.** Ground Planes for Reference




### 3.2.1.3 Via (Ask a Question)

The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver must be used to optimize the via according to the stack-up.

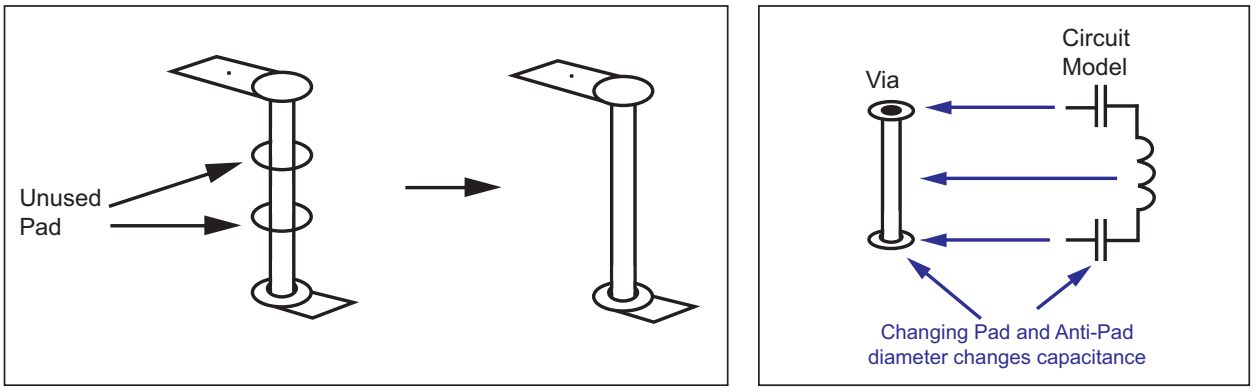
**Figure 3-5.** Via Illustration




Follow these guidelines:

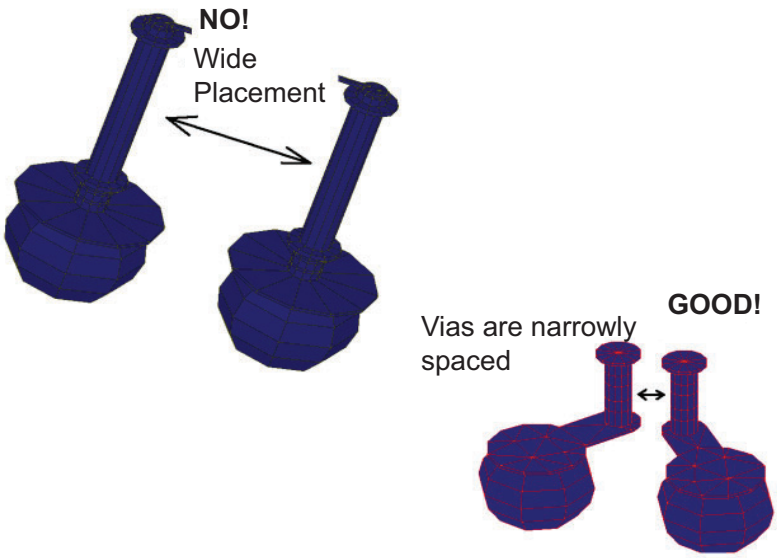
- Many vias on different traces must be avoided, or minimized as much as possible.
- The length of via stubs must be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried vias. Using blind-vias and back drilling are good methods to eliminate via stubs and reduce reflections.
- If feasible, non-functional pads must be removed. Non-functional pads on-via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

**Figure 3-6.** Non-Functional Pads of Via



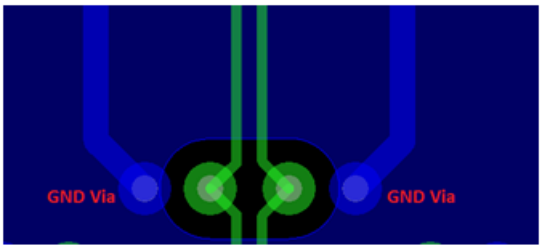

Using tight via-to-via pitches helps reducing the effect of crosstalk, as shown in the following figure.

**Figure 3-7.** Via-to-Via Pitch




Symmetrical ground vias (return vias) must be used to reduce discontinuity for Common mode signal components, as shown in the following figure. Common mode of part of the signal requires continuous return path for TX and RX to GND. Return vias help maintain the continuity.

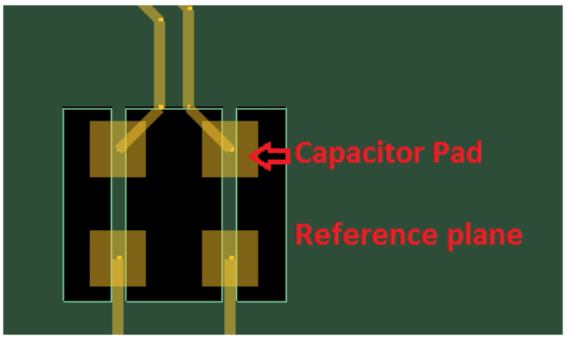
**Figure 3-8.** GND Via or Return Via




### 3.2.2 DC Blocking Capacitors (Ask a Question)

The plane underneath the pads of DC blocking capacitors must be removed, as shown in the following figure, to match the impedance of the pad to 50Ω.

**Figure 3-9.** Capacitor Pad Reference Plane



# 4. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

| Revision | Date | Description |
|---|---|---|
| A | 11/2023 | The following is a summary of changes made in this revision.<br>• Converted user guide document to Microchip template.<br>• Changed the document number to DS50003612 from UG0726.<br>• Updated Table 1-12 with the following changes:<br>– Replaced “VDDAUX” with “VDD18”.<br>– Changed the power-down sequencing requirement from “Power down VDDI before VDD18, VDD, and VDD25 of that bank” to “Power down VDDI before VDD18, VDD, and VDD25”.<br>– Added a footnote mentioning that separate power sources must be used when VDDI = 1.8V and VDD18 = 1.8V.<br>• Rephrased 1.5. Reset to mention that DEVRST_N is not mandatory to be used for warm resets.<br>• Added information about the calculation of target impedance in 1.1. Power Supplies.<br>• Added a note regarding I/O glitch during JTAG programming in 1.2. I/O Glitch.<br>• Added a new row for IOD in Table 2-1.<br>• Removed the following line from **XCVR** and placed it under **Reset** in Table 2-1: “There is one IO_CFG_INTF pin available, which can be used as input”. |
| 11.0 | — | The following is a summary of changes made in this revision.<br>• Updated 1.4. Clocks to highlight regional clock implications while migrating designs to different device sizes.<br>• Updated Figure 1-9.<br>• Added link to PPAT in 1.4. Clocks for preferred clock inputs connectivity to PLLs, DLLs, and global clock network.<br>• Added a note about hot socketing exceptions in 1.3.2. Hot Socketing (GPIO Only).<br>• In 1.1. Power Supplies, added a note about power sequencing requirement for I/O calibration.<br>• Updated 1.2. I/O Glitch.<br>• Updated 1.1.1. PolarFire Decoupling Capacitors. |
| 10.0 | — | The following is a summary of changes made in this revision.<br>• Added more information in new footnotes for VDD and VDDA in Table 1-1.<br>• Added footnote in Table 1-2 to Table 1-8 to specify the objective of decoupling capacitors.<br>• Updated 1.2. I/O Glitch and Table 1-11 for power-up and power-down sequencing requirements for mitigating I/O glitch. |
| 9.0 | — | The following is a summary of changes made in this revision.<br>• Updated the glitch information in 1.2. I/O Glitch.<br>• Updated Figure 1-5 to power VDDI3 (JTAG Bank) required for cold sparing. |
| 8.0 | — | The following is a summary of changes made in this revision.<br>• Updated the glitch information in 1.2. I/O Glitch.<br>• Added more information on the VDDI and VDDAUX in 1.1. Power Supplies. |

| .....continued | | |
|---|---|---|
| **Revision** | **Date** | **Description** |
| 7.0 | — | The following is a summary of the changes made in this revision:<br>• Added 1.9. MIPI Hardware Design Guidelines.<br>• Added reset guidelines in 1.5. Reset.<br>• Added power-supply decoupling capacitors for the following device packages:<br>– MPF200T-FCG484 (0.8 mm).<br>– MPF200T-FCSG536 (0.5 mm).<br>– MPF200T-FCG325 (0.5 mm).<br>– MPF100T-FCG325 (0.5 mm).<br>– MPF100T-FCG484 (0.8 mm). |
| 6.0 | — | The following is a summary of the changes made in revision 6.0 of this document:<br>• Reference Voltage (VREFx) information updated in 1.1. Power Supplies.<br>• Added basic information about 1.1.4. Pin Assignment Tables.<br>• Updated Power-Supply Decoupling Capacitors—MPF300T - FCG1152/FCG784/FCG484.<br>• Added Power-Supply Decoupling Capacitors—MPF500T - FCG1152/FCG784 (1mm), Power-Supply Decoupling Capacitors—MPF200T - FCG784/FCG484 (1mm), and MPF100T - FCG484 (1mm).<br>• Added 1.9. MIPI Hardware Design Guidelines.<br>• Added 1.5. Reset. |
| 5.0 | — | The following is a summary of the changes made in revision 5.0 of this document:<br>• Details of power supply decoupling capacitors for MPF300-FCG1152, MPF300-FCG484, MPF300-FCG784, MPF300-FCVG484, and MPF300-FCSG536 devices were updated.<br>• XCVR_REF and VDD_XCVR_CLK supply pins details were added. For more information, see 1.1. Power Supplies).<br>• Information about VDDIx and VDDAUXx power supplies was updated. For more information, see 1.1.3. Unused Power Supply.<br>• A note about the power supply constraint of VDDI3 and VDD_XCVR_CLK pins was added. For more information, see 1.1. Power Supplies.<br>• Details of decoupling capacitors in PolarFire devices were added. For more information, see Table 1-9.<br>• Additional information about VDDIx, VDDAUXx, and VDD_XCVR_CLK pins was added. For more information, see 1.1.3. Unused Power Supply.<br>• The design checklist for XCVR pins was updated. For more information, see Table 2-1.<br>• Information about VREF was added to core power supply operation details. For more information, see 1.1. Power Supplies.<br>• Information about cold sparing was updated. For more information, see 1.3.1. Cold Sparing.<br>• JTAG pin details were updated. For more information, see Table 1-15.<br>• The SPI master mode programming connectivity diagram was updated. For more information, see Figure 1-7.<br>• Information about device reset was updated. For more information, see 1.5. Reset.<br>• DDR3 and DDR4 placement and routing guidelines were removed. These guidelines are available in PolarFire FPGA and PolarFire SoC FPGA Memory Controller User Guide. |
| 4.0 | — | Revision 4.0 was published in September 2017. The sections Termination Schemes and PCB Capacitor Placement and Mounting Techniques were removed from this document. |

**.....continued**

| Revision | Date | Description |
|---|---|---|
| 3.0 | — | Following is a summary of changes made in this revision.<br>• Added 2. Board Design Checklist.<br>• Added the 1.7.4. Special Pins section in the Introduction chapter.<br>• Updated the Power-up sequence for core supplies. For more information, see 1.1. Power Supplies and 1.1.2. Power-Supply Topology.<br>• Removed a note related to XCVR_TX and RX signals under the 1.1.3. Unused Power Supply section.<br>• Updated the VDDI pin name from VDDIx to VDDI3 in the Device Programming section. For more information, see 1.7. Device Programming. |
| 2.0 | — | Following was a summary of changes made in revision 2.0 of this document.<br>• Values in the Power-Supply Decoupling Capacitors—MPF300-FCG484 table were updated.<br>• Values and parameters were updated in the SPI Master Mode Programming Pins table. For more information, see Table 1-16.<br>• Updated Figure 2. For more information, see Figure 1-2. |
| 1.0 | — | The first publication of this document. |

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