CR0028
Characterization Report
RTG4 FPGA Characterization Report for XAUI

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated Figure 6, page 10.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 RTG4 FPGA Characterization Report for XAUI

Microsemi® RTG4® FPGA device family provides a fully embedded 10 Gigabit Attachment Unit Interface (XAUI) specialized 10 Gigabit Ethernet optical modules and system backplanes. It supports four SerDes transmit and four SerDes receive channels for 8B/10B encoding. XAUI is commonly used as backplane in networking switches to connect line cards to switch cards. The embedded XAUI block is part of the SerDes block, which supports four lanes of SerDes with data rates supported up to 3.125 Gbps. XAUI is available on all -1 speed grade RTG4 devices in all temperature grades. For more information about the RTG4 family devices, see http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4.

2.1 Scope

This test report provides a summary of completed RTG4 FPGA tests to meet compliance with the XAUI standards specified by IEEE 802.3ae 10 Gigabit Ethernet Task Force. The tests were conducted to analyze voltage, temperature, and process variations for XAUI electrical validation.

2.2 Sample Device Tests

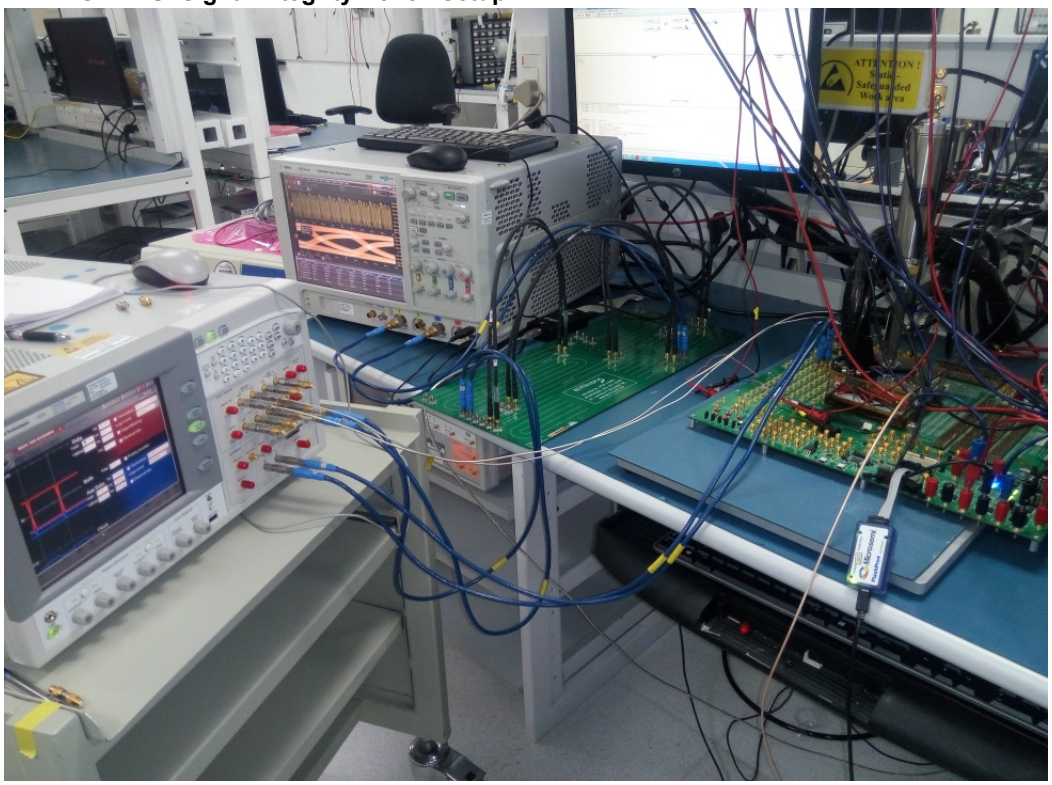
Sample device tests were conducted on sample devices to represent process variations across silicon fabrication. These devices were separated and tested from a larger group of devices representing the worst-case corners and conditions that are used to report the results.

2.3 Test Boards

Testing is performed on the Microsemi signal integrity (SI) board that has a test socket and provides connections to vary power supply conditions. To ensure the integrity of the characterization measurements, special attention is given to the signal integrity of the high-speed serial channels. Detailed analysis of the printed circuit board (PCB) ensures that the board performs to the desired results. The transmitter (Tx) and receiver (Rx) signal paths for each SerDes are routed to high-bandwidth SMP connectors to ensure good signal integrity and performance. The PCB channel is measured and de-embedded while performing tests.

The following figure shows the XAUI signal integrity bench setup.

Figure 1 • **RTG4 XAUI Signal Integrity Bench Setup**



2.4 XAUI 802.3 Electrical Compliance Test

XAUI electrical test was completed based on IEEE Standard 802.3-2008 http://standards.ieee.org/getieee802/download/802.3-2008_section4.pdf. This document describes physical layer specifications to achieve the 10 GBs sublayer requirements. This also highlights the procedures and conditions tested within the Microsemi factory to validate the device performance as per XAUI specifications.

2.4.1 Transmitter Tests

Process, voltage, and temperature variations tests were performed at the 3.125 GBs data rate to test XAUI speeds per XAUI specification on RT4G150 PROTO(LG1657) three sample devices. De-embedding mathematically removes the effects of unwanted PCB routing portions that will impede on the measured data by subtracting their contribution. This de-embedding provides a portrayal of the devices actual performance. The S-Parameter de-embedding for Tx was applied during the measurements to remove board trace impairments.

Table 1 • **XAUI Test Specifications**

Parameter	IEEE 802.3 Definition	Specifications	Unit
	Transmitter Near-End Tests		
XAUI baud	The baud rate of the device is within the specified limits in 47.3.3.	3.125 GBaud +/- 100 ppm	GBaud, ppm
XAUI unit interval	The serial bit rate per 47.3.3.	320	pS

Table 1 • **XAUI Test Specifications *(continued)***

Parameter	IEEE 802.3 Definition	Specifications	Unit
Transmitter Near-End Tests			
Driver single-ended output swing maximum absolute test (Tx+ and Tx-)	The single-ended output swing of the device is within the specified minimum and maximum limits in 47.3.3.2.	2.3	V
Driver single-ended output swing minimum absolute test (Tx+ and Tx-)		–400	mV
Transmitter differential return loss (output impedance)	The output impedance is within the specified limits in 47.3.3.4.	<3	dB
Transmitter Far-End Tests			
Driver output amplitude test	The driver differential output amplitude of the device is within the specified limits in 47.3.3.2.	800-1600	mVp-p
Driver eye template test	The device transmitter meets the eye template requirements as specified in 47 (multiple sub-clauses).	Complies to all eye mask parameters including rise and fall times	
Total jitter test	The device conforms to the jitter requirements specified in 47.3.3.5.	<550	mUI
Deterministic jitter test		<370	mUI

2.4.2 Receiver Tests

XAUI receiver electrical tests conform to the XAUI specification. Process, voltage, and temperature variations were tested at the 3.125 GBs data rate to cover XAUI speeds per XAUI Specification on RT4G150 PROTO(LG1657) units. To provide the required amount of ISI, this test includes running the signal through several inches of board trace that is connected through SMP connectors. The additional ISI from the board traces ensures that the signal as measured at the DUT is stressed enough to meet XAUI requirements.

Table 2 • **Receiver Tests**

Parameter	IEEE 802.3 Definition	Specifications	Unit
Jitter tolerance margin	The XAUI compliance interconnect definition as specified in 47.4.1, for the purposes of this test suite, by stressing the input receiver.	0.65 T_J amplitude	UIp-p
		0.37 DJ minimum	
		0.55 RJ minimum	
Receiver coupling	AC coupled as specified in 47.3.4.4	Included for all tests	
Sinusoidal jitter (Sj)		As needed to achieve T_J 650	mUIp-p
Receiver input return loss	The receiver's differential mode input impedance is within the specified limits in 47.3.4.5.	>10	dB
	The receiver's common mode input impedance is within the specified limits in 47.3.4.5.	>6	

2.5 Electrical Device Tests

Bench test equipment was used for both Rx and Tx jitters and amplitude measurements.

2.5.1 Electrical Test Equipment/Software

- Agilent DSA91304A, 13 GHz real time scope
- Agilent N5431A XAUI automation test application, v1.24 or later
- Agilent N4903B J-BERT 12.5 Gb/s with complete jitter tolerance
- Agilent E3631A 80 W triple output power supply
- Agilent E3633A 200 W DC power supply
- Agilent 81133A pulse/pattern generator
- Silicon thermal temperature control unit
- Silicon thermal chiller CH5050
- Silicon thermal linear power supply PS190-L
- Silicon thermal temperature controller LB1000-i
- Silicon thermal 31 × 31 (mm) thermal head adapter
- SMA-to-SMA cables
- SMA-to-SMP cables
- Microsemi engineering signal integrity board
- Agilent 11742A DC blocks

2.5.2 Electrical Test Environment

Device electrical test was conducted by Microsemi using various power supply voltages and temperatures. Minimum (V_{min}) and maximum voltages (V_{max}) were varied by +/-5% of the typical voltage (V_{typ}) supply for the supplies related to the XAUI and SerDes blocks of the device. These devices were also tested at the industrial temperature limits (-40 ºC to + 125 ºC) on Rev A TYP corner devices.

Table 3 • **Temperature Specifications**

Specification	Temperature Range
Military temperatures	-55 ºC to 125 ºC
Industrial temperatures	-40 ºC to 100 ºC

2.5.3 Test Conditions

The following table lists the power supply and temperature test conditions.

Table 4 • **Power Supply and Temperature Test Conditions**

	Voltage and Temperature						
Voltage Dependencies	**1.2 V V_{DD} Range**						**Unit**
xDDR_PLL_VDDA	3.135	3.3	3.465	3.15	3.3	3.45	V
CCC_xyz_PLL_VDDA	2.375	2.5	2.625	3.15	3.3	3.45	V
SERDES_x_PLL_VDDA	2.375	2.5	2.625	3.15	3.3	3.45	V
SERDES_x_L[0:3]VDDAPLL	2.375	2.5	2.625	2.375	2.5	2.625	V
SERDES_x_L[0:3]VDDAIO	1.14	1.2	1.26	1.14	1.2	1.26	V
SERDES_x_VDD	1.14	1.2	1.26	1.14	1.2	1.26	V
V_{DD} (core supply)	1.14	1.2	1.26	1.14	1.2	1.26	V

Table 4 • **Power Supply and Temperature Test Conditions *(continued)***

Voltage Dependencies	Voltage and Temperature 1.2 V V_{DD} Range						Unit
Temperature	-55	-55	-55	-55	-55	-55	ºC
	-40	-40	-40	-40	-40	-40	ºC
	-25	-25	-25	-25	-25	-25	ºC
	-100	-100	-100	-100	-100	-100	ºC
	-125	-125	-125	-125	-125	-125	ºC

2.6 Test Summary

The following table shows the XAUI test summary.

Table 5 • **Summary of Test Results**

Test[1]	Parameter	IEEE 802.3 Specification	RT4G150 Worst Case Test Results	Unit
Transmitter Testing				
Baud rate	Within range	-100.000 Bd ppm <= VALUE <= 100.000 Bd ppm	-4.8	ppm
Driver single-ended output swing maximum absolute test (Tx+) (near-end)	Maximum	VALUE <= 2300	590	mV
Driver single-ended output swing minimum absolute test (Tx+) (near-end)	Minimum	VALUE >= -400	280	mV
Driver single-ended output swing maximum absolute test (Tx-) (near-end)	Maximum	VALUE <= 2300	-390	mV
Driver single-ended output swing minimum absolute test (Tx-) (near-end)	Minimum	VALUE >= -400	-280	mV
Driver output amplitude test (far-end)	Within range	200 <= VALUE <= 1600	790	mV
Driver eye template test (far-end)		Zero mask failures		N/C
Total jitter test (far-end)	Maximum	VALUE <= 550	429	mUI
Deterministic jitter test (far-end)	Maximum	VALUE <= 370	349	mUI
Differential return loss	Maximum	VALUE <3	<3	dB
Receiver Testing				
Total jitter (T_J)	Maximum	650 mUIp-p	<650	mUI
Deterministic jitter (D_J)	Maximum	370 mUIp-p	<370	mUI
Deterministic + random jitter (Dj + Rj)	Maximum	550 mUIp-p	<550	mUI
Sinusoidal jitter (S_J)		As needed to achieve T_J 650 mUIp-p		mUI
Differential return loss	Minimum	>10	>10	dB
Common mode return loss	Minimum	>6	>6	dB

1. All the specified tests in the table are passed.

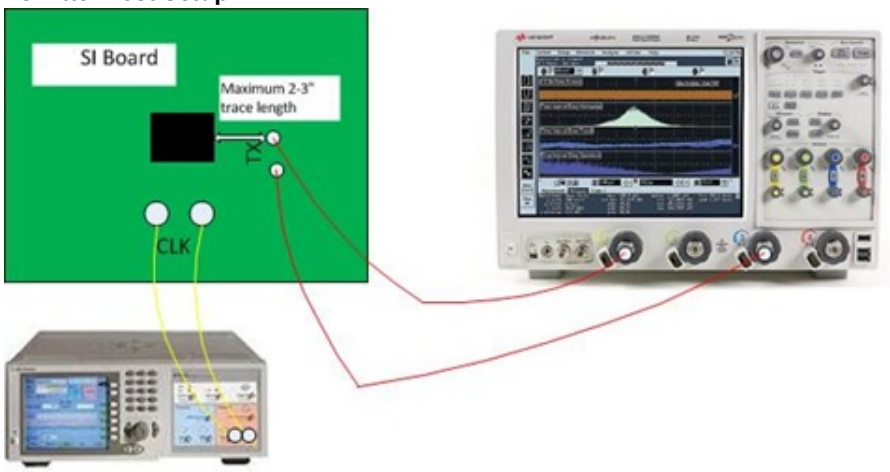
2.6.1 Transmitter Tests

2.6.1.1 Test Setup

The characterization test was performed in accordance with XAUI specification for Near-End and Far-End measurements. The transmitter far-end jitter and eye template is measured. The XAUI RefCLK is taken from the external clock source generator. The signal is driven from a test signal source generating a CJPAT test pattern. CJPAT is a binary pattern sequence that exposes a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns.

The worst-test condition identified was determined to be at -55 ºC temperature and at V_{max} voltage. It must be 125 ºC at V_{min}.

Figure 2 • **Transmitter Test Setup**



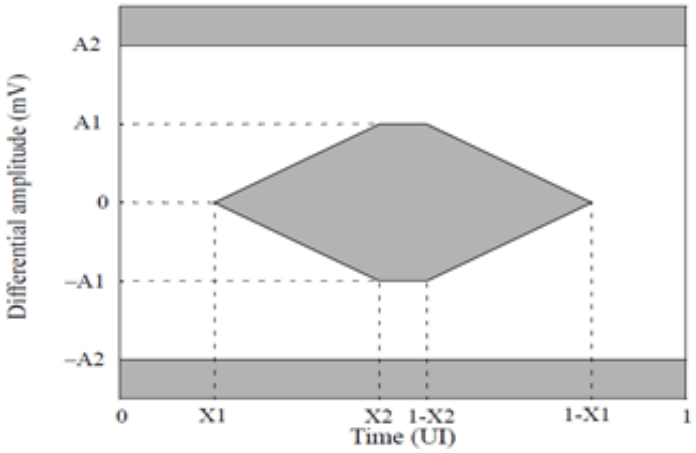
The following table lists the worst-case data for Tx parameters

Table 6 • **Tx Worst-Case Data Summary**

	Worst case Data		Specifications		
Test[1]	**Min**	**Max**	**Min**	**Max**	**Unit**
Baud rate	-4.8	22.4	-100	100	Bd ppm
Driver single-ended output swing maximum absolute test (Tx+) near-end		590		2300	mV
Driver single-ended output swing maximum absolute test (Tx-) near-end	-390		–400		mV
Driver single-ended output swing minimum absolute test (Tx+) near-end		280		2300	mV
Driver Single-ended Output swing minimum absolute test (Tx-) near-end	-280	-150	-400		mV
Driver output amplitude test (far-end)	790	970	200	1600	mV
Driver eye template test (far-end)			Zero mask failures		
Total jitter test (far-end)		429		550	mUI
Deterministic jitter (far-end)		349		370	mUI

1. All the tests specified in the table are passed.

Figure 3 • **Transmit Eye Mask**

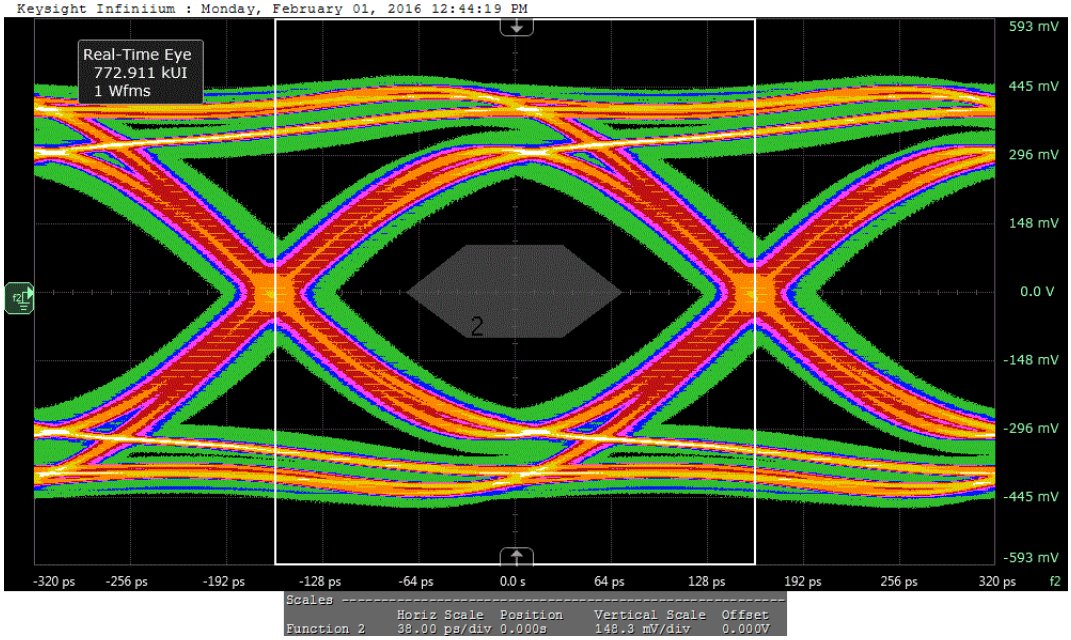


The following table lists the transmit eye intervals.

Table 7 • **Transmit Eye Intervals**

Symbol	Far-end Value	Unit
X1	0.275	UI
X2	0.400	UI
A1	100	mV
A2	800	mV

Figure 4 • **Transmit Eye Diagram with Far-End Mask**



2.6.2 Receiver Test

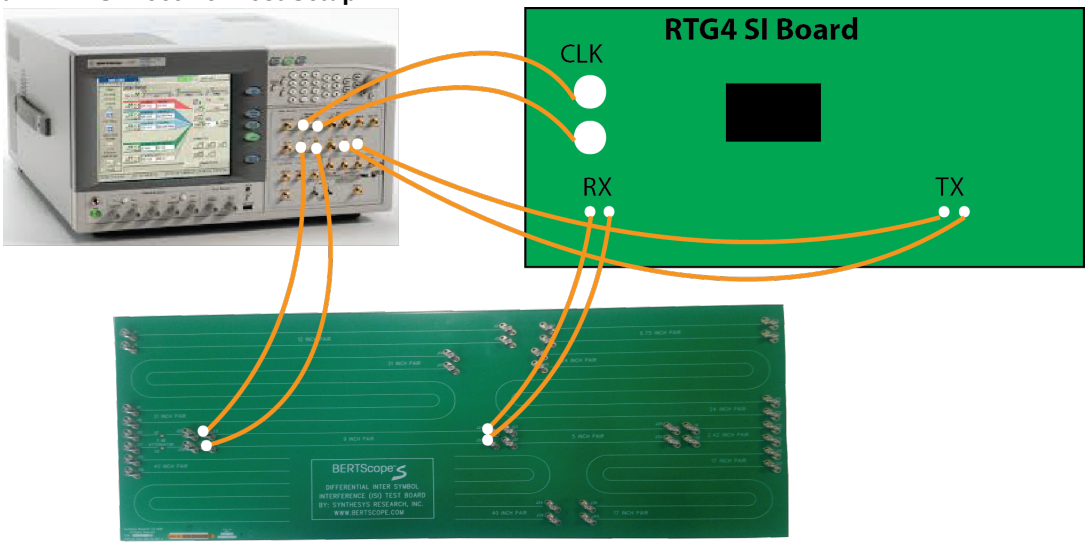
2.6.2.1 Test Setup

A XAUI compliance channel setup is used for the XAUI receiver testing as specified in 47.3.4.2. The objective of the test is to provide a stressed input signal to the device and still have the receiver operate with a bit-error rate (BER) of better than 10-12.

The JBERT is interconnected together to provide a necessary signal generator for XAUI receiver testing. The XAUI receiver channel is pre-conditioned with a calibrated setup including a 55" (ISI) backplane trace that is combined with test board trace between SMP and DUT's package to generate required 370 mUI of Dj. This setup guarantees calibration of the XAUI compliant stressed eye to the Rx package balls of the device.

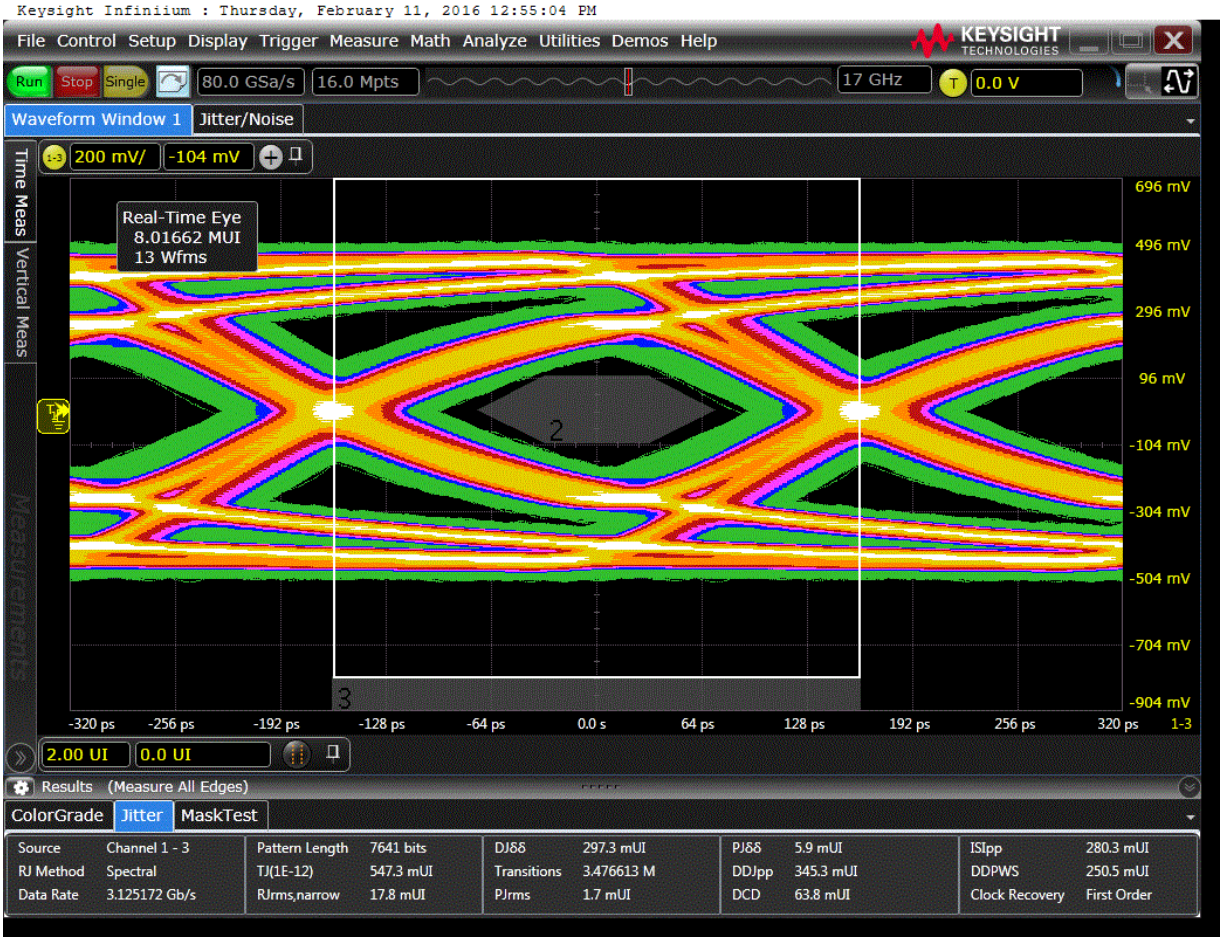
The XAUI receiver setup uses common RefCLK topology by having RefCLK driven by the JBERT.

Figure 5 • **XAUI Receiver Test Setup**



Note: ISI channel = 55 inches

Figure 6 • **Stress Input Signal with Eye Mask Height of 200mV pk-to-pk**



The following table list the stressed input eye jitter components.

Table 8 • **Stressed Input Eye Jitter Components**

Jitter Measurement	Value	Unit
Data rate	3.125	Gb/s
TJ(1E-12)	625.1	mUI
RJ-rms	17.3	mUI
PJ-rms	3.5	mUI
DJ-dual-dirac	380.6	mUI
DDJ-pp	422.5	mUI
ISI-pp	252.2	mUI
DCD	195	mUI

The stressed input signal must meet the far-end eye mask while introducing the required jitter components. Figure 6, page 10 shows the stressed eye and the reported jitter components. The signal is driven from a test signal source generating a CJPAT test pattern. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns. The purpose of the test is to feed in a jittery signal while observing the receiver's lock status, stability, and data BER. The receiver must be AC coupled, and the input is measured at the pin of the receiver.

Additional sinusoidal jitter is added from the JBERT tester and swept as a function of frequency to the point where the device starts to fail. The BER is compared to a jitter tolerance mask where jitter is applied to the stressed input channel.

The following figure plots the results of the sample devices in comparison with the XAUI specified mask.

Figure 7 • **Single Tone Sinusoidal Jitter Mask**

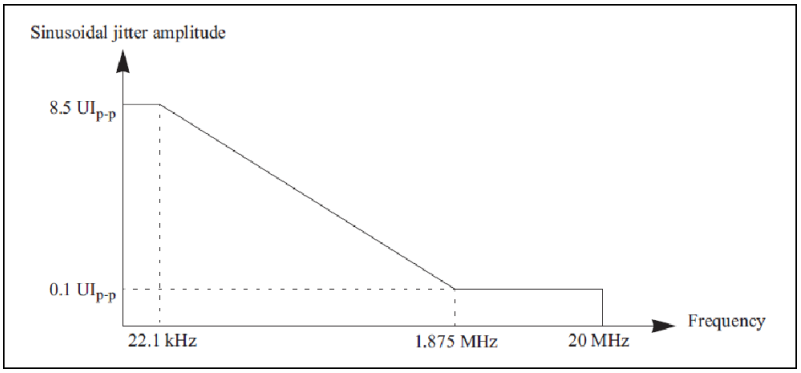
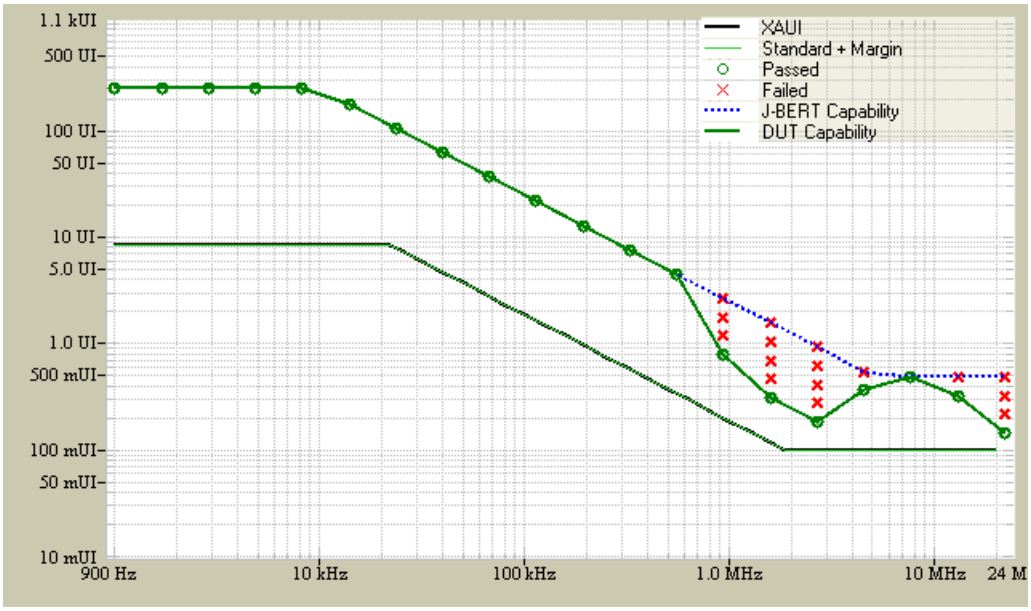


Figure 8 • **Sinusoidal Jitter Tolerance Test Plot**



2.6.2.2 Return Loss

The primary effect of return loss relates to the amount of signal being transferred to the receiver causing closure of the eye. Multiple reflections, caused by the finite return loss of driver in conjunction with the channel, introduce additional amplitude distortion as well as jitter. Return loss measurements of the RTG4 and IGLOO2 devices include the additional losses from the on-chip, off-chip, and package components of both the receiver and the transmitter. The receiver tests included AC coupling capacitors. The tests used frequency domain return loss measurements, where the loss is measured while sweeping the frequency from 100 MHz to 5 GHz.

Figure 9 • **Tx Return Loss Plot**

Figure 10 • **Rx Return Loss**

2.7 Conclusion

The test results demonstrate that the capabilities of the RTG4 XAUI solution systems require high-reliability requiring devices to be robust. The report provides a baseline summary of the thorough tests performed by Microsemi to assure users that the device will meet the performance and functional requirements in their customized XAUI system.