

UG0735
User Guide
Resolver Interface v4.2



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 2.1

The following is a summary of the changes made in revision 2.0 of this document

- [Figure 1](#), page 3 is updated to add the input port: `direction_config_i`.
- [Table 1](#), page 4 is updated to add new signal name: `direction_config_i` and its description. Also, updated description for the signal name: `pp_ratio_i`.

1.2 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document

- [Figure 1](#), page 3 is updated to add the input ports, `clear_buffer_i` and `pp_ratio_i`.
- [Table 1](#), page 4 is updated to add new signal names, `clear_buffer_i`, `pp_ratio_i` and their descriptions.
- The configuration parameter `g_PP_RATIO` is deleted in [Table 2](#), page 4.
- The count value of the resource, "Sequential elements" is changed from 960 to 980 in [Table 3](#), page 5.
- The equation to calculate `theta_factor` constant is edited in [Hardware Implementation](#), page 3.

1.3 Revision 1.1

The following is a summary of the changes made in revision 1.1 (Published in January 2017) of this document.

- Key features were added. For more information, see [Key Features](#), page 2.
- Supported family information was added. For more information, see [Supported Families](#), page 2.
- Information on scaling the calculated speed using the theta factor was added. For more information, see [Hardware Implementation](#), page 3.
- The description for the `calib_angle_i` input signal was updated. For more information, see [Table 1](#), page 4.
- The `PP_RATIO` configuration parameter was added. For more information, see [Table 2](#), page 4.

1.4 Revision 1.0

Revision 1.0 (Published in November 2016) was the first publication of this document.

2 Overview

A resolver is a position sensor or transducer which measures the absolute angular position of the rotating shaft to which it is attached.

2.1 Key Features

The resolver interface IP block supports the following features:

- Provides a high frequency signal for excitation
- Demodulates sine and cosine winding inputs
- Computes angle and speed

2.2 Supported Families

The resolver interface IP block supports the following families:

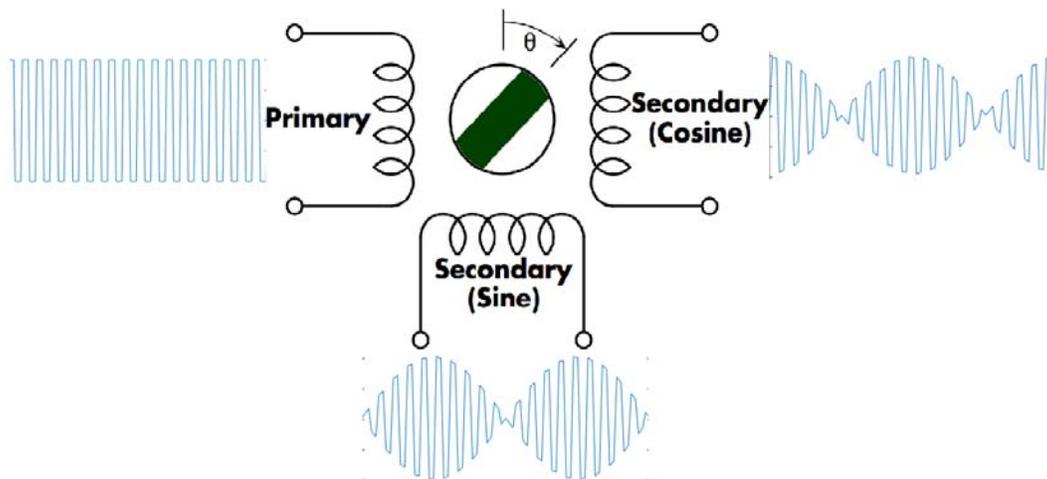
- SmartFusion[®]2
- IGLOO[®]2
- RTG4[™]

2.3 Theory of Operation

The operating principle of a resolver is similar to the operating principle of a synchro. Resolvers are typically built like small motors with a rotor (attached to the shaft whose position is to be measured) and a stator (stationary part) which takes the excitation signals and produces the output signals. A resolver typically consists of a primary winding, also called excitation winding and two secondary windings called cosine and sine windings. The secondary windings are geometrically placed such that winding signals are cosine and sine function of rotor angle.

The following figure shows the signals generated by resolver.

Figure 1 • Signal Generation in Resolver

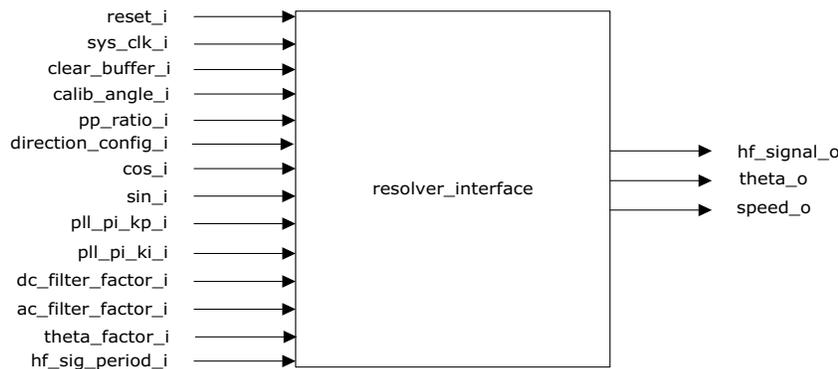


The device used to process the resolver signals and convert them in to a digital angle format is called a resolver to digital converter (RDC). The resolver IP implements the functionality of a RDC. The IP provides excitation signal in the form of a square wave to the primary winding whose frequency can be configured. The IP processes the secondary signals, demodulates them and calculates the angle and speed of the rotor.

3 Hardware Implementation

The following figure shows the block diagram of the resolver interface.

Figure 1 • System-Level Block Diagram of Hardware Implementation



The resolver interface IP generates a square wave that is fed to the primary winding of the resolver. The frequency of the square wave can be configured through hf_sig_period_i input. The cos_i and sin_i signals from the secondary windings are demodulated and filtered to get effective cosine and sine signals. A phase-locked loop (PLL) is used to extract angle and speed from cosine and sine signals.

The PLL uses a PI controller whose gains pll_pi_kp_i and pll_pi_ki_i can be tuned to get required response time. A higher value for gains results in quick response to angle and speed changes but can also induce noise in angle and speed outputs.

In motor control application, the resolver zero position must be aligned with motor magnetic zero position. To achieve this, a calib_angle_i signal is used. During calibration process, the signal goes high and the motor is forced to align its rotor to magnetic zero position. The angle output is reset to zero during this period and is taken as reference for measuring absolute angle. A motor and resolver can have multiple pole pairs in which the motor control algorithm needs multiple theta transitions (3600) for one mechanical rotation of the rotor. This feature can be configured through the pp_ratio_i port, listed in [Table 1](#), page 4.

The theta_factor constant is calculated by using the following equation. The calculated speed can be scaled to per unit using theta_factor_i.

$$\text{theta_factor} = \frac{18.12 * \text{Rated Motor Speed(RPM)}}{\text{System Clock (MHz)}}$$

EQ1

The hf_sig_period input determines the frequency of square wave injected into resolver primary, calculated by using the following equation.

$$\text{hf_sig_period_i} = \frac{f_{\text{sys_clk}}}{\text{hf_freq} \times 2}$$

EQ2

where,

hf_freq = Frequency of the square wave injected into resolver primary

fsys_clk = Frequency of the system clock provided at sys_clk_i input

3.1 Inputs and Outputs

The following table describes the input and output ports of the resolver interface block.

Table 1 • Inputs and Outputs of Resolver Interface Block

Signal Name	Direction	Description
reset_i	Input	Active low asynchronous reset signal to design
sys_clk_i	Input	System clock
clear_buffer_i	Input	When 1, internal speed filter buffer is cleared When 0, buffer is normally operated
calib_angle_i	Input	The IP enters calibration state when this signal goes high. The angle offset between the resolver zero and the motor magnetic zero is calculated in this state
direction_config_i	Input	Specifies the direction of motor rotation
pp_ratio_i	Input	The ratio of number of motor poles to number of resolver poles expressed as exponent of 2. Example for motor poles 16, resolver poles 2, pp_ratio_i = 3; For motor poles 8, resolver poles 2, pp_ratio_i = 2; For motor poles 4, resolver poles 4, pp_ratio_i = 0
cos_i	Input	Cosine winding input (from ADC)
sin_i	Input	Sine winding input (from ADC)
pll_pi_kp_i	Input	Proportional gain of PI controller used for PLL
pll_pi_ki_i	Input	Integral gain of PI controller used for PLL
dc_filter_factor	Input	Filter time constant of high-pass filter used to eliminate DC value from Sine and Cosine signals
ac_filter_factor	Input	Filter time constant of low-pass filter used to eliminate modulation wave frequency component for Sine and Cosine signals
theta_factor_i	Input	Theta factor constant, as calculated from EQ1
hf_sig_period_i	Input	Half the value of the high frequency square wave time period, as calculated from EQ2
hf_signal_o	Output	Square wave signal used to drive primary winding of resolver
theta_o	Output	Angle output of resolver; equivalent to motor electrical angle
speed_o	Output	Speed output of resolver IP

3.2 Configuration Parameters

The following table describes the configuration parameters used in the hardware implementation of the resolver interface. These are generic parameters and can be varied as per the application requirements.

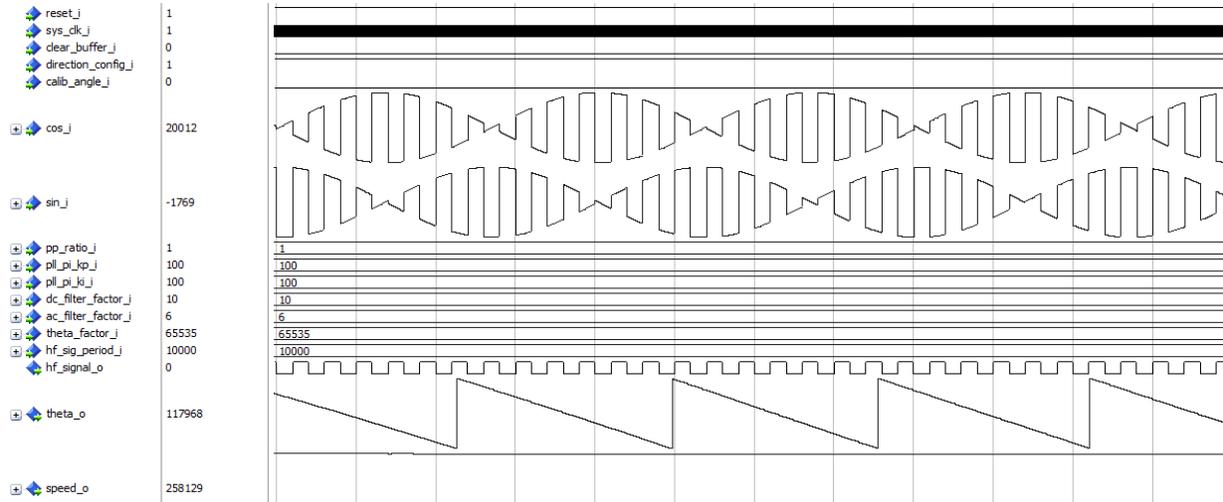
Table 2 • Configuration Parameters

Name	Description
g_NO_MCYCLE_PATH	The number of clock delays required before the multiplication product ready signal is asserted

3.3 Timing Diagram

The following figure shows the timing diagram of the resolver interface block. The timing diagram represents a typical use case of the resolver interface block.

Figure 2 • Timing Diagram



3.4 Resource Utilization

The following table lists the resource utilization of the resolver interface block after synthesis.

Table 3 • Resource Utilization of Resolver Interface Block

Resource	Count
Sequential elements	980
Combinational logic	1090
MACC	2
RAM1kx18	0
RAM64x18	0