Abstract

The total ionizing dose and single event effects hardening and testing of the first radiation hardened analog mixed-signal telemetry controller IC, the LX7730, are presented. TID and SEE characterizations were performed on the regulated currents and voltage, scan chain, full analog telemetry acquisition chain - analog input MUX to ADC chain- and supporting circuitry.

Total Dose and Single Event Effects Hardening and Testing on Mixed Signal Telemetry LX7730 Controller

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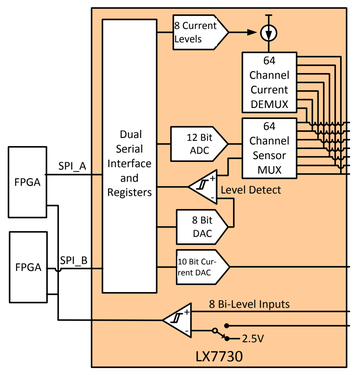
Conclusion

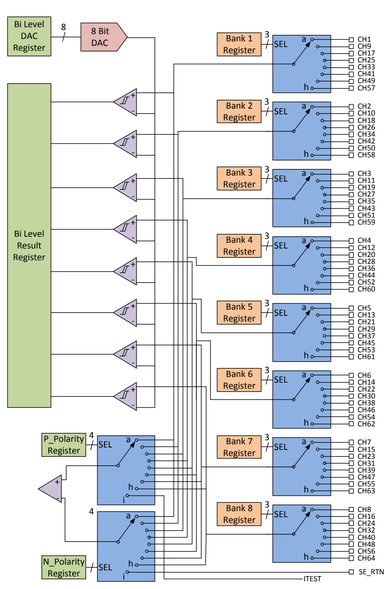
Total dose testing and heavy ion beam testing to investigate the single-event effects of the LX7730 have been performed. The results exhibit the hardening goals for the device. The performance at 100krad of the different blocks of this highly integrated device is consistent with the pre-radiation results. The design is SEL immune up to 87 MeV.cm²/mg and 125°C (fluence of 1e8 particles/cm²). In addition, the LX7730 shows strong performance under the beam up to 83 MeV.cm²/mg of all evaluated blocks including the internally regulated currents and voltages as well as the complete telemetry chain .

I. INTRODUCTION

- The LX7730 is a spacecraft telemetry manager that functions as a companion to an FPGA.
- Contains a 64 universal input multiplexer configured as a mix of differential and single ended sensor inputs.
  - For input conditioning, a programmable current source can be directed to any of the 64 universal inputs.
  - The universal inputs can be sampled with a 12-bit ADC.
  - Internal gain for conversion is settable to accommodate for a wide range of input voltages.
  - The universal inputs can also be set as variable bi-level inputs with a threshold set by an internal 8-bit DAC.
  - Additional 10-bit current DAC with complementary outputs.
  - 8 fixed threshold bi-level inputs.
- The telemetry manager is register-programmable with 17 addressable 8-bit registers.
- Two options are available for communication with the host FPGA,
  - 8-bit parallel bus with 5 address bits and a read/write bit that can communicate at a speed of up to 25MHz
  - A pair of 12.5MBPS SPI interface that can support redundant communication to two different hosts.
- Powered out of a single supply VCC nominally at 15V in addition to the VDD supply used by the FPGA. .
- Manufactured as a dual die MCM solution in a 132-pin CQFP package.

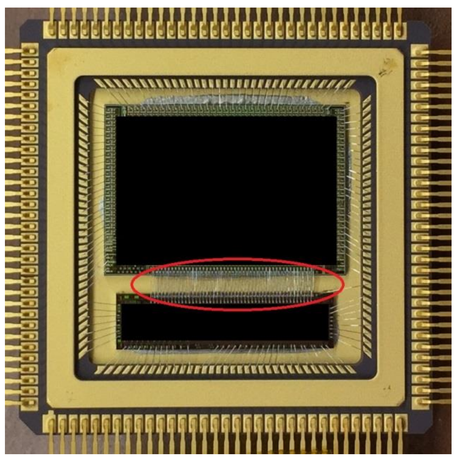
- The first round of radiation tests on the initial version of the LX7730 confirmed the hardening goals:
  - TID tolerance is greater than 100krad (SiO2);
  - SEL immunity as well as strong SET performance is demonstrated.
- Some sensitivity to single event upset has been seen on the initial design. This was corrected in the latest version that is currently going through qualification under MIL-PRF-38535 with QML-Q completion in November 2016 and QML-V in March 2017.





II. LX7730 TID HARDENING AND TEST RESULTS

- The LX7730 Controller is designed using two technology processes.
  - BI-CMOS process for analog precision circuitry;
  - Dielectric Isolated technology process capable of high voltage operation up to 350V which is well beyond the absolute max rated operating voltage of the LX7730 of 20V.
- The LX7730 embeds a variety of diverse functions.
- The design is partitioned to take advantage of both processes in terms of accuracy requirements and high voltage device rating requirements.
- Process selection is an important part in the radiation hardening approach.
- The device is manufactured as a dual-die solution with interconnect bonds between the two dice, co-packaged in a single package.



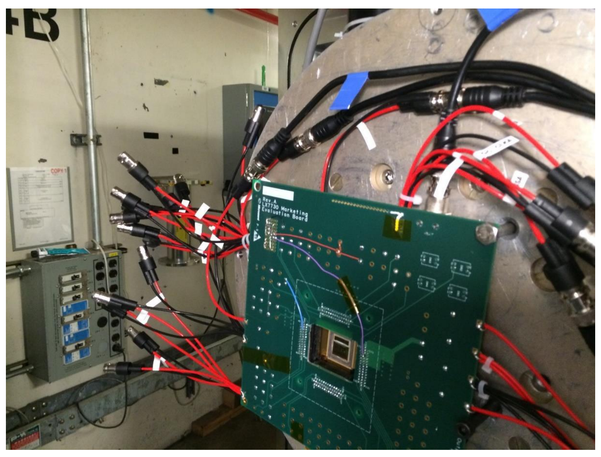
Note: All Data taken at 25C

Parameters	Min	Typ	Max	Units	SN 500 Pre	SN 500 100kR Post	SN 501 Pre	SN 501 100kR Post	Comment
Operating Current									
VCC Normal Current	38	73	84	mA	54.265	52.424	54.822	52.273	Pass
VCC Standby Current	2.0	3.9	5.5	mA	4.126	3.578	3.757	3.531	Pass
VEE Current	-2.5	-5.0	-6.0	mA	-4.956	-4.579	-4.994	-4.598	Pass
Under Voltage Detection									
VCC UVLO	9.5	10	10.5	V	9.970	9.980	9.960	9.970	Pass-very stable
VCC UVLO Hyst	150	200	250	mV	180	205	180	205	Pass-very stable
VEE UVLO	-7.5	-8.00	-8.20	V	-7.995	-8.000	-8.015	-8.015	Pass-very stable
VEE UVLO Hyst	150	200	250	mV	200	205	205	200	Pass-very stable
+5V UVLO	3.9	4.15	4.40	V	4.155	4.155	4.170	4.170	Pass-very stable
+5V UVLO Hyst	150	200	250	mV	195	195	195	195	Pass-very stable
Internally Regulated Voltages and Currents									
VCC to VEE voltage drop	1.5	2.5	3.0	V	2.414	2.395	2.413	2.387	Pass-very stable
+5V voltage	4.75	5.00	5.25	V	5.077	5.068	5.075	5.053	Pass-very stable
VREF voltage	4.95	5.00	5.05	V	5.038	5.060	5.031	5.063	Pass-very stable
IREF pin voltage	1.56	1.60	1.64	V	1.619	1.612	1.608	1.600	Pass-very stable
Analog MUX									
Differential Range	0		5	V	PASS	PASS	PASS	PASS	Pass
Common Mode Range	-5		5	V	NT	NT	NT	NT	
Voltage Clamp power applied	15	17	22	V	20.645	20.707	20.502	20.607	Pass-very stable
	-22	-17	-15		-20.647	-20.707	-20.506	-20.573	Pass-very stable
Voltage Clamp (VCC=VEE=0)	15	17	22	V	20.481	20.555	20.347	20.421	Pass-very stable
	-22	-17	-15		-20.477	-20.551	-20.332	-20.415	Pass-very stable

- The Microsemi hardening solution involves a series of test chips and careful device characterization prior to being used in analog designs.
- In addition, some primitive devices on a given process or inadequate biasing of devices can yield poor total dose results.
- Microsemi has developed a series of block design IP and a components library to overcome these issues.
- Total Dose radiation testing was performed on the LX7730.
- The testing was completed at the Defense Microelectronics Activity (DMEA) Test Facility in McClellan, California.
- The devices were characterized pre-radiation and post radiation.
- Testing was performed up to a total dose of 100 krad on two DUTs, SN#500 and SN#501.
- The TID testing followed MIL-STD-883 Test Method 1019, Condition A with a dose rate of 50rad/s.
- The test results show minimal change in device performance up to a total dose of 100 krad.
- Results show very good results on all key blocks of the design, stable supply current consumptions, and regulated voltages.
- Results also show a shift in telemetry conditioning current drifting less than 10% from pre-radiation values.
- This shift is mitigated at the system level by using a reference channel for calibration.
- In addition, negligible added leakage on channel MUX inputs remains well within the specification of 200nA on all channel inputs over the full voltage range.
- Thus, we conclude that the performance of the LX7730 is TID tolerant up to 100 krad.

III. LX7730 SEE HARDENING AND TEST RESULTS

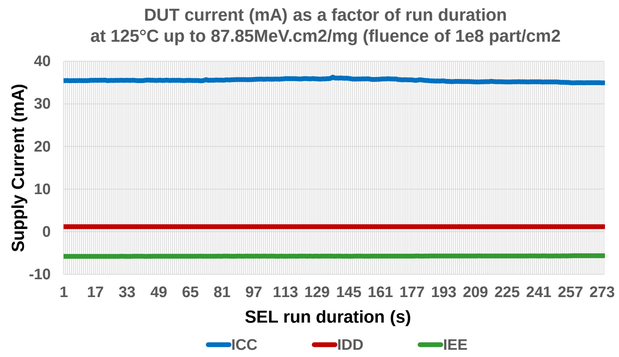
- Similar to TID hardening, process selections and layout optimization are key in achieving good resiliency for both SEL and SET conditions.
- In addition to layout isolation techniques, SET can be reduced by design techniques such as
  - adequate biasing currents,
  - filtering for analog circuits
  - and the use of TMR flip-flops for digital designs.
- Single Event Effect tests were performed on the LX7730 at the Lawrence Berkeley National Laboratory (LBNL) in Berkeley, CA using a 10MeV/n cocktail beam.
- The SEE results demonstrate the strong radiation performance of the device.
- The LX7730 is SEL immune and SET immune on currents and voltages regulated by the device.
- The device shows a strong resiliency of the complete telemetry chain (DC and AC) and current sources.



III. LX7730 SEE HARDENING AND TEST RESULTS (CONT.)

Single Event Latchup

- SEL tests were performed at a temperature of up to 125°C on 3 DUTs.
- No SEL events were observed when tested to a fluence of 1x108 particles/cm² and a LET = 87.85 MeV.cm²/mg.
- The LX7730 is powered out of a nominal VCC supply of 15V in addition to VDD also used for the FGPA supply.
- The LX7730 internally generates a negative charge pump Voltage VEE of nominally -12.5V, which can be externally bypassed.
- In this SEL test, the charge pump voltage is externally forced as a worst-case condition to monitor current jumps.



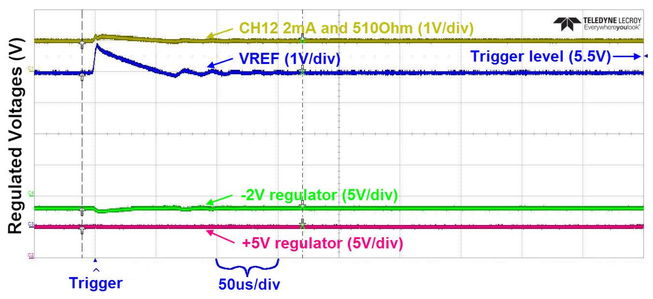
LX7730 Sub Circuit Testing and Performance

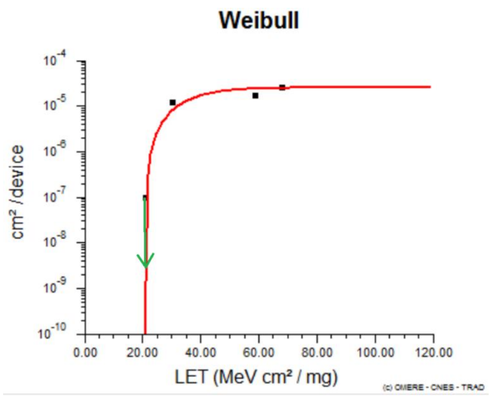
Power On Reset

- Testing on the initial version of silicon showed single event sensitivity with the Power On Reset (POR) circuitry, which required a design fix.
- Subsequent testing on the current revision of the design shows that the POR issue was fixed.
- Two tests were conducted to verify this.
  - With the current source turned-on, a value is loaded into the current source register. The current source test with POR shows no reset up to LET = 67.87 MeV.cm²/mg.
  - The reset pin was monitored and no event is observed up to LET = 79.10 MeV.cm²/mg and fluence = 2.5x10⁷ particles/cm².

Regulators

- This test checks for single event transients on the regulated supplies of the module, +5V, VREF, the -2V and the negative charge pump -13V outputs.
- Test results for GEO orbit suggest that the mean time between failures (MTBF) is 1 SET (positive trigger) on the 5V reference every 265 years.



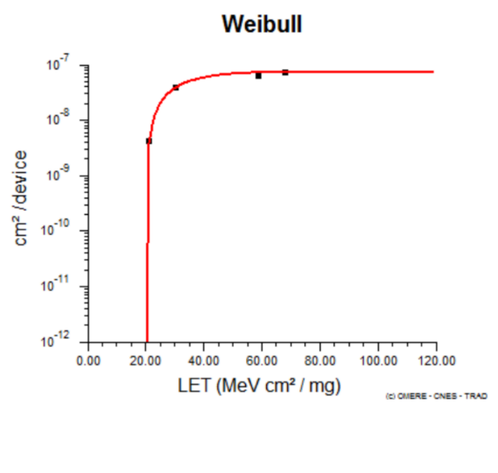


- The +5V regulator, -2V regulator and Ch12 with 2mA and 510Ω load curves show essentially no single event transient.
- Only upsets observed was on VREF with a 10% upset for 50us.
- The upsets are minimal and do not affect the operation of the device.
- The VREF bypass capacitor is 100nF versus the +5V bypass capacitor which is 1uF.
- This is one possible reason for no noticeable upsets on the +5V generated supply.

Scan Chain

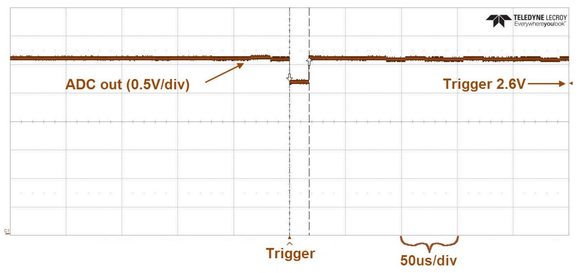
- All 269 flip-flops in the registers and digital busses are included in the scan chain.
- A 1 MHz clock and 250kHz input pattern are used to test the flip-flop chain.
- The scan chain test shows good SEU performance from the TMR flip-flops.

Run #	Ion	LET (MeV.cm²/mg)	Tilt	Effective LET (MeV.cm²/mg)	Flux (cm-2.s-1)	Effective Fluence (cm-2)	TID (krad)	SEUs	# events	X-section
42	Xe	58.78	30	67.87	6.40E+04	1.00E+07	10.94	X	211	7.84E-08
40	Xe	58.78	0	58.78	3.60E+04	1.00E+06	0.95	X	16	5.95E-08
41	Xe	58.78	0	58.78	3.60E+04	1.00E+07	9.48	X	193	7.17E-08
				58.78						6.56E-08
43	Kr	30.23	0	30.23	7.00E+04	1.00E+07	4.87	X	108	4.01E-08
44	Cu	21.17	0	21.17	7.00E+04	1.00E+07	3.41	X	12	4.46E-09



Telemetry Chain

- The analog input MUX, Differential Amplifier, Anti-Aliasing Filter, and the ADC are included in the telemetry chain.
- AC and DC signals are sent through the telemetry chain.
- The digital output of the SPI bus is observed by rebuilding the output with a DAC.
  - A DC voltage of 1V is input to CH9 while CH10 is grounded.
  - The amplifier is set to a gain of 2.
  - The ADC samples every 170uS.
  - The FPGA reads the ADC through the SPI bus and outputs the value to a DAC to show the digital outputs on the oscilloscope.
- Upsets noted in this test are triggered when the DAC output is 500mV below the typical output of 3.2V.



Run #	Ion	LET (MeV.cm²/mg)	Tilt	EffectiveLET (MeV.cm²/mg)	Flux (cm-2.s-1)	Effective Fluence (cm-2)	TID (krad)	SEUs	SETs	# events	X-section
58	Cu	21.17	0	21.17	1.20E+05	1.00E+07	3.41		X	19	1.90E-06
59	Cu	21.17	0	21.17	1.20E+05	1.00E+07	3.41		X	0	0.00E+00
60	Cu	21.17	0	21.17	1.20E+05	1.00E+07	3.41		X	0	0.00E+00
				21.17							6.33E-07
57	Kr	30.23	0	30.23	1.30E+05	4.17E+06	2.03		X	16	3.84E-06
56	Kr	30.23	30	34.91	1.30E+05	5.35E+06	3.01		X	28	5.23E-06
55	Xe	58.78	30	67.87	6.50E+04	3.59E+06	3.93		X	21	5.85E-06