

Integrated Instrumentor User Guide

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Contents

Chapter 1: Design Setup

Instrumenting and Saving a Design	7
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Chapter 2: IICE Configuration

Multiple IICE Units	10
Common IICE Parameters	11
Individual IICE Parameters	13
IICE Sampler Tab	13
IICE Clock Tab	15
IICE Controller Tab	16
IICE Options Tab	18
DTD Tab	19
RTD Tab	19

Chapter 3: Using the Instrumentor

Instrumentor Windows and Views	21
Data View Instrumentor GUI	22
Hierarchy Browser	22
RTL Tab	23
Instrumentation Tab	24
Commands and Procedures	25
Opening Designs	25
Selecting Signals for Data Sampling	25
Instrumenting Buses	27
Partial Instrumentation	30
Multiplexed Groups	32
Sampling Signals in a Folded Hierarchy	33
Instrumenting the Verdi Signal Database	35
Instrumenting Signals Directly in the idc File	35
Selecting Breakpoints	37
Selecting Breakpoints Residing in Folded Hierarchy	38

Configuring the IICE	39
Real-time Debugging	39
Writing the Instrumented Design	43
Synthesizing Instrumented Designs	45
Listing Signals	45
Searching for Design Objects	46
TCL Script Window	48
Chapter 4: HAPS Deep Trace Debug	
External Memory Instrumentation and Configuration	50
DTD Tab	51
Running Deep Trace Debug with DDR3 Memory	53
Running Deep Trace Debug with SRAM Memory	55
SRAM Clocks	56
Sample Depth Calculation	57
Sample Clock Calculation	57
Chapter 5: Support for Instrumenting HDL	
VHDL Instrumentation Limitations	60
Verilog Instrumentation Limitations	62
SystemVerilog Instrumentation Limitations	65

CHAPTER 1

Design Setup

After your HDL is successfully created, the instrumentor is used to define the specific signals to be monitored. Saving the instrumented design generates an *instrumentation design constraints* (idc) file and adds constraint files to the HDL source for the instrumented signals and break points. The design is synthesized and then run through the remainder of the process. After the device is programmed with the debuggable design, the debugger is launched to debug the design while it is running in the target system. For information on using the debugger, see the *Debugger User Guide*.

The information required to instrument a design includes references to the HDL design source, the user-selected instrumentation, the settings used to create the Intelligent In-Circuit Emulator (IICE™), and other system settings. Additionally, you can save the original design in either an encrypted or non-encrypted format, which is then used to reproduce the exact state of the design.

Instrumenting and Saving a Design

After setting up the IICE as described in [Chapter 2, IICE Configuration](#) and after defining the instrumentation (selecting the signals for sampling, and setting breakpoints) as described in [Chapter 3, Using the Instrumentor](#), the design is instrumented and saved. To save your instrumented design, select File->Save All from the main instrumentor menu.

Saving a design generates an *instrumentation design constraints* (.idc) file and adds compiler pragmas in the form of constraint files to the design RTL for the instrumented signals and break points. This information is then used to incorporate the instrumentation logic (IICE and COMM blocks) into the synthesized netlist.

CHAPTER 2

IICE Configuration

An important part preparing a design for debugging is setting the parameters for the Intelligent In-Circuit Emulator or “IICE” in the instrumentor. The IICE parameters determine the implementation of one or more IICE units and configure the units so that proper communication can be established with the debugger. The IICE parameters common to all IICE units are set in the Instrumentor Preferences dialog box and apply to all IICE units defined for that design; the IICE parameters unique to each IICE definition in a multi-IICE configuration are interactively set on the Edit IICE Settings dialog box tabs. Tabs are available to support deep-trace debug for Virtex-based designs, real-time debugging with a Mictor card, and the cross-triggering feature.

- [IICE Sampler Tab](#) – includes sample depth selection and defines the external memory configuration.
- [IICE Clock Tab](#) – defines the sample clock and clock edge.
- [IICE Controller Tab](#) – includes complex counter trigger width specification and selection of state machine triggering.
- [IICE Options Tab](#) – controls trigger-signal export and cross triggering.

This chapter describes how to configure one or more IICE units.

Note: IICE configurations set in the instrumentor impact the operations available in the debugger.

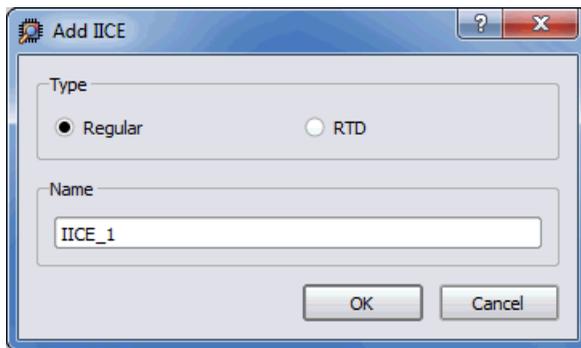
Multiple IICE Units

Multiple IICE units allow triggering and sampling of signals from different clock domains within a design. Each IICE unit is independent and can have unique IICE parameter settings including sample depth, sampling/triggering options, and sample clock and clock edge. During the subsequent debugging phase, individual or multiple IICE units can be armed.

Adding an IICE Unit



The instrumentor graphical window includes an Add IICE icon to define an additional IICE unit for the current design. When you click the icon, the Add IICE dialog box opens to allow you to define the type and name of the new IICE unit.



When you click OK, the HDL source code in the RTL window is redisplayed without any signals instrumented, the Instrumentation window is cleared, and the Select field directly above the icon is updated with the name of the IICE unit. When creating a new IICE unit:

- Select Regular (the default) to add a normal IICE unit or select RTD to add a HAPS[®]-based real-time debug IICE unit; see [Real-time Debugging, on page 39](#).
- Optionally enter a name for the IICE unit. By default, the IICE name is formed by adding an `_n` suffix to IICE (for example, IICE_0, IICE_1, etc.)

Deleting an IICE Unit

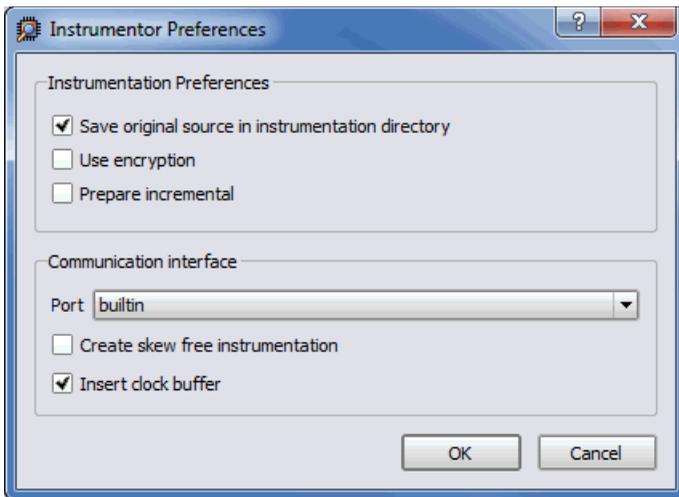


To delete an IICE unit from the design, click the Remove IICE icon. When more than one IICE unit is defined, select the IICE unit in the Select field before you click the icon.

Common IICE Parameters



The IICE parameters common to all IICE units in a multi-IICE configuration include the communication port setting and if the optional skew-free hardware is to be used. The parameters are set on the Instrumentor Preferences dialog box (click the Instrumentor Preferences icon to display).



Communication Port

The Communication port parameter specifies the type of connection to be used to communicate with the on-chip IICE. The connection types are:

- **builtin** – indicates that the IICE is connected to the JTAG Tap controller available on the target device.
- **soft** – indicates that the Synopsys Tap controller is to be used. The Synopsys FPGA Tap controller is more costly in terms of resources

because it is implemented in user logic and requires four user I/O pins to connect to the communication cable.

- `umrbus` – indicates that the IICE is connected to the target device through the UMRBus.

See [Chapter 5, *Connecting to the Target System*](#) in the *Debugger User Guide*, for a description of the communication interface.

Create Skew Free Instrumentation

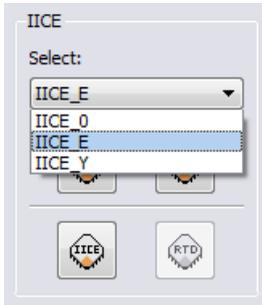
The Create skew free instrumentation check box, when checked, incorporates skew-free master/slave hardware to allow the instrumentation logic to operate without requiring an additional global clock buffer resource for the JTAG clock.

When no global clock resources are available for the JTAG clock, this option causes the IICE to be built using skew-free hardware consisting of master-slave flip-flops on the JTAG chain which prevents clock skew from affecting the logic. Enabling this option also causes the instrumentor to NOT explicitly define the JTAG clock as requiring global clock resources.

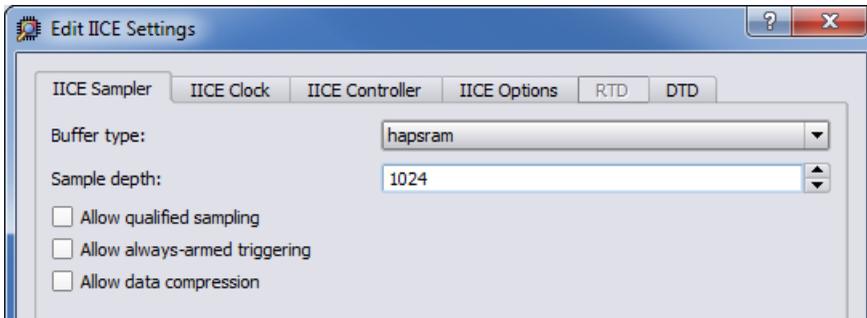
Individual IICE Parameters



The individual parameters for each IICE are defined on a series of tabs of the Edit IICE settings dialog box. Before you display this dialog box, make sure that the name of the target IICE unit appears in the the Select field (use the drop-down menu).



With the target IICE selected, click the Edit IICE settings icon to display the Edit IICE settings dialog box.



IICE Sampler Tab

The IICE Sampler tab shown above is the default tab and defines:

- Buffer type
- Sample depth
- Sampling/triggering options

Buffer Type

The Buffer type parameter specifies the type of RAM to be used to capture the on-chip signal data. The default value is FPGA Memory; the hapsram setting configures the IICE to use extended daughter board DDR3 or SRAM memory. For more information, see [Chapter 4, HAPS Deep Trace Debug](#).

Sample Depth

The Sample depth parameter specifies the amount of data captured for each sampled signal. Sample depth is limited by the capacity of the FPGAs implementing the design, but must be at least 8 due to the pipelined architecture of the IICE.

Sample depth can be maximized by taking into account the amount of RAM available on the FPGA. As an example, if only a small amount of block RAM is used in the design, then a large amount of signal data can be captured into block RAM. If most of the block RAM is used for the design, then only a small amount is available to be used for signal data. In this case, it may be more advantageous to use logic RAM. The sample depth increases significantly with the deep-trace debug feature.

Allow Qualified Sampling

The Allow qualified sampling check box, when checked, causes the instrumentor to build an IICE block that is capable of performing qualified sampling. When qualified sampling is enabled, one data value is sampled each time the trigger condition is true. With qualified sampling, you can follow the operation of the design over a longer period of time (for example, you can observe the addresses in a number of bus cycles by sampling only one value for each bus cycle instead of a full trace). Using qualified sampling includes a minimal area and clock-speed penalty.

Allow Always-Armed Triggering

The Allow always-armed triggering check box, when checked, saves the sample buffer for the most recent trigger and waits for the next trigger or until interrupted. When always-armed sampling is enabled, a snapshot is taken each time the trigger condition becomes true.

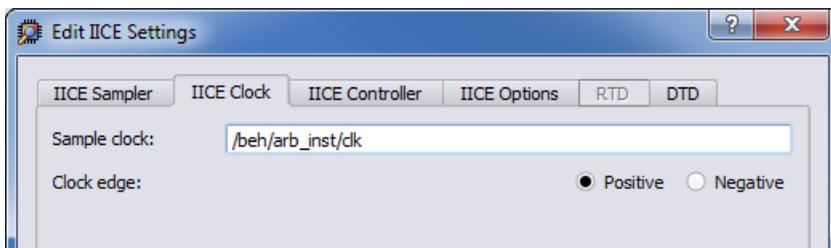
With always-armed triggering, you always acquire the data associated with the last trigger condition prior to the interrupt. This mode is helpful when analyzing a design that uses a repeated pattern as a trigger (for example, bus cycles) and then randomly freezes. You can retrieve the data corresponding to the last time the repeated pattern occurred prior to freezing. Using always-armed sampling includes a minimal area and clock-speed penalty.

Allow Data Compression

The Allow data compression check box, when checked, adds compression logic to the IICE to support sample data compression in the debugger (see [Sampled Data Compression, on page 28](#) in the *Debugger User Guide*). When unchecked (the default), compression logic is excluded from the IICE, and data compression in the debugger is unavailable. Note that there is a logic data overhead associated with data compression and that the check box should be left unchecked when sample data compression is not to be used.

IICE Clock Tab

The IICE Clock tab defines the sample clock.

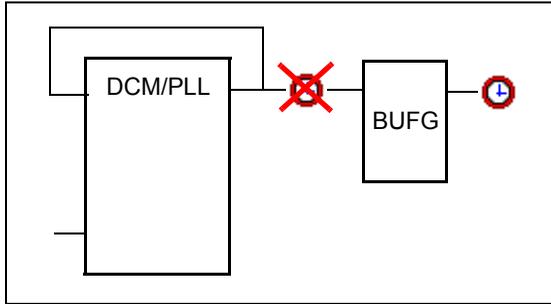


Sample Clock

The Sample clock parameter determines when signal data is captured by the IICE. The sample clock can be any signal in the design that is a single-bit scalar type. Enter the complete hierarchical path of the signal as the parameter value.

Care must be taken when selecting a sample clock because signals are sampled on an edge of the clock. For the sample values to be valid, the signals being sampled must be stable when the specified edge of the sample clock occurs. Usually, the sample clock is either the same clock with which the sampled signals are synchronous or a multiple of that clock. The sample

clock must use a scalar, global clock resource of the chip and should be the highest clock frequency available in the design. The source of the clock must be the output from a BUFG/IBUFG device.



You can also select the sample clock from the RTL window by right-clicking on the watchpoint icon in the source code display and selecting Sample Clock from the popup menu. The icon for the selected (single-bit) signal changes to a clock face as shown in the following figure.

```

54
55     always @(posedge  clk or negedge  clr)
56     begin
57     if ( clr == 1'b0)
58      current_state = s_RESET; /* 4'b0000 */
59     else begin

```

Sample Clock Icon

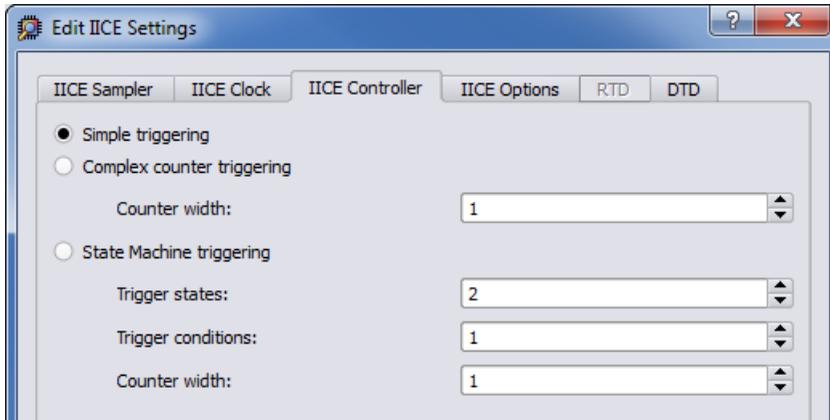
Note: The sample clock edge can only be set from the IICE Clock tab.

Clock Edge

The Clock edge radio buttons determine if samples are taken on the rising (positive) or falling (negative) edge of the sample clock. The default is the positive edge.

IICE Controller Tab

The IICE Controller tab selects the IICE controller's triggering mode. All of these instrumentation choices have a corresponding effect on the area cost of the IICE.



Simple Triggering

Simple triggering allows you to combine breakpoints and watchpoints to create a trigger condition for capturing the sample data.

Complex-Counter Triggering

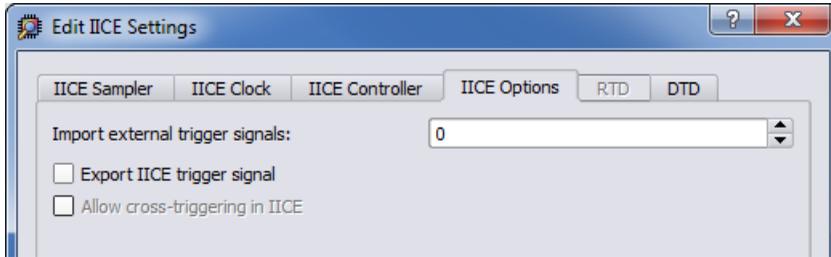
Complex-counter triggering augments the simple triggering by instrumenting a variable-width counter that can be used to create a more complex trigger function. Use the width setting to control the desired width of the counter.

State-Machine Triggering

State-machine triggering allows you to pre-instrument a variable-sized state machine that can be used to specify an ultimately flexible trigger condition. Use Trigger states to customize how many states are available in the state machine. Use Trigger condition to control how many independent trigger conditions can be defined in the state machine. For more information on state-machine triggering, see [State Machine Triggering, on page 88](#) in the *Debugger User Guide*.

IICE Options Tab

The IICE Options tab configures external triggering to allow a trigger from an external source to be imported and configured as a trigger condition for the active IICE. The external source can be a second IICE located on a different device or external logic on the board rather than the result of an instrumentation.



Import External Trigger Signals

The imported trigger signal includes the same triggering capabilities as the internal trigger sources used with state machines. The adjacent field selects the number of external trigger sources with 0, the default, disabling recognition of any external trigger. Selecting one or more external triggers automatically enables state-machine triggering.

Note: When using external triggers, the pin assignments for the corresponding input ports must be defined in the synthesis or place and route tool.

Export IICE Trigger Signal

The Export IICE trigger signal check box, when checked, causes the master trigger signal of the IICE hardware to be exported to the top-level of the instrumented design.

Allow cross-triggering in IICE

The Allow cross-triggering in IICE check box, when checked, allows this IICE unit to accept a cross-trigger from another IICE unit. For more information on cross-triggering, see [Cross Triggering](#), on page 36 in the *Debugger User Guide*.

DTD Tab

The DTD tab configures the deep-trace debug feature. For deep-trace debug configuration and setup information, see [Chapter 4, HAPS Deep Trace Debug](#).

RTD Tab

The RTD tab is active when the selected IICE unit is a type real-time debug. Real-time debugging is a feature that provides scope or logic analyzer access to instrumented signals directly through a Mictor board interface connector installed on the HAPS board. For real-time debug configuration and setup information, see [Real-time Debugging, on page 39](#).

CHAPTER 3

Using the Instrumentor

The instrumentor performs the following functions:

- defines the instrumentation for the user's HDL design
- creates the instrumented HDL design
- creates the associated IICE

The remainder of this chapter describes:

- [Instrumentor Windows and Views](#)
- [Commands and Procedures](#)

Instrumentor Windows and Views

The Graphical User Interface (GUI) for the instrumentor is divided into four major areas:

- Data View Instrumentation GUI
- Hierarchy Browser
- RTL Tab
- Instrumentation Tab

In this section, each of these areas and their uses is described.

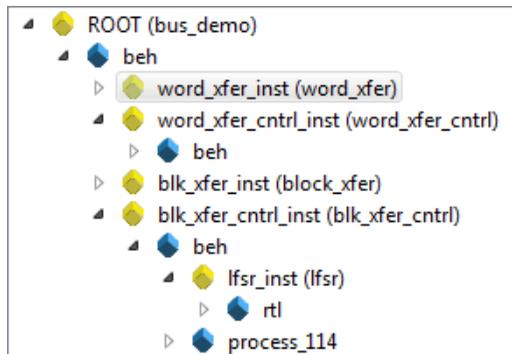
Data View Instrumentor GUI

The instrumentor data view GUI includes the configuration icons as described in [Chapter 2, IICE Configuration](#).

Hierarchy Browser

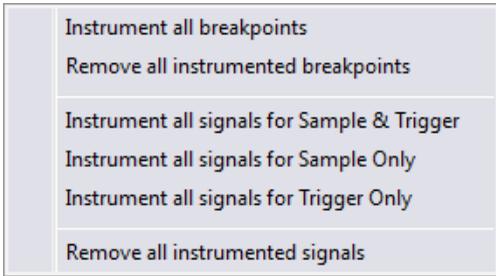
The hierarchy browser on the left shows a graphical representation of the design's hierarchy. At the top of the browser is the ROOT node. The ROOT node represents the top-level entity or module of your design. For VHDL designs, the first level below the ROOT is the architecture of the top-level entity. The level below the top-level architecture for VHDL designs, or below the ROOT for Verilog designs, shows the entities or modules instantiated at the top level.

Double-clicking on an entry opens the entity/module instance so that the hierarchy below that instance can be viewed. Lower levels of the browser represent instantiations, case statements, if statements, functional operators, and other statements.



Single clicking on any element in the hierarchy browser causes the associated HDL code to be visible in the RTL tab display.

A popup menu is available in the hierarchy browser to set or clear breakpoints or watchpoints at any level of the hierarchy. Positioning the cursor over an element and clicking the right mouse button displays the following menu.



The selected operation is applied to all breakpoints or signal watchpoints at the selected level of hierarchy. You cannot instrument signals when a sample clock is included in the defined group.

Black-box modules are represented by a black icon, and their contents can not be instrumented. Also, certain modules cannot be instrumented (see [Chapter 5, Support for Instrumenting HDL](#), for a specific description).

RTL Tab

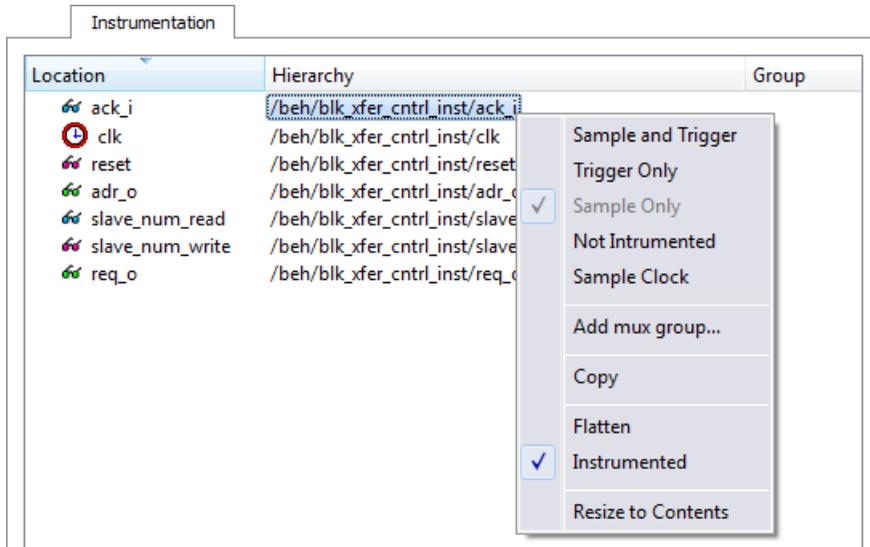
The RTL tab displays the HDL source code and is the default view when you launch the instrumentor. The code is annotated with signals that can be probed and breakpoints that can be selected. Signals that can be selected for probing by the IICE are underlined, colored in blue, and have small watch-point icons next to them. Source lines that can be selected as breakpoints have small circular icons in the left margin adjacent to the line number.

```

113  -- the state-machine
114  process ( st_curr_state, st_ack_i, st_delay_cnt )
115  begin
116    st_req_o <= '0';
117    st_set_delay_cnt <= '0';
118    st_dec_delay_cnt <= '0';
119    case (st_curr_state) is
120      when st_idle =>
121        st_next_state <= st_run;
122      when st_run =>
123        st_req_o <= '1';
124        if ( st_ack_i = '1' ) then
125          st_next_state <= st_delay1;
126        else
  
```

Instrumentation Tab

The Instrumentation tab lists the active watchpoint and breakpoint entries that have been set within the active module or entity. The entries can be modified by selecting the entry and assigning a new value from the popup menu.



Commands and Procedures

The following sections describe basic instrumentor commands and procedures.

Opening Designs

To open the instrumentor from the synthesis tool:

1. Create an Identify implementation by right clicking on an existing synthesis implementation and selecting **New Identify Implementation** from the popup menu.
2. Set/verify any technology, device mapping, or other pertinent options (see the implementation option descriptions in the *Synopsys FPGA Synthesis* or *Certify User Guide*) and click **OK**. A new, Identify implementation is added to the synthesis tool project view.

Launching the instrumentor displays the design hierarchy and the RTL file content with all the potential instrumentation marked and available for selection.

Selecting Signals for Data Sampling



To select a signal to be sampled, simply click on the watchpoint icon next to the signal name on the RTL tab; a popup menu appears that allows the signal to be selected for sampling, triggering, or both.



Scalar Signal Popup



Bus Signal Popup

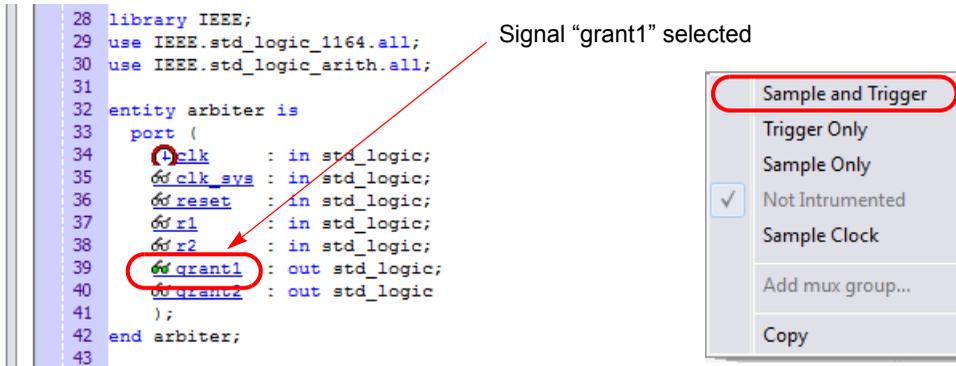
To control the overhead for the trigger logic, always instrument signals that are not needed for triggering with the Sample only selection (the watchpoint icon is blue for sample-only signals).

Qualified clock signals can be specified as the Sample Clock (see [Sample Clock, on page 15](#)) and bus segments can be individually specified (see [Instrumenting Buses, on page 27](#)). In addition, signals specified as Sample and trigger or Sample only can be included in multiplexed groups as described in [Multiplexed Groups, on page 32](#).

When the watchpoint icon is clear (unfilled), the signal has not been instrumented. The colors of the filled icons are described in the following table:

	Red	Signal is enabled for triggering only
	Green	Signal is enabled for both sampling and triggering
	Blue	Signal is enabled for sampling only

The example below shows signal grant1 being enabled for sample and trigger.



The TCL Script window at the bottom displays the Tcl command that implements the selection (signals add -iice {IICE} -sample -trigger {/beh/arb_inst/grant1} and the results of executing the command.

```

%
signals add -iice {IICE} -sample -trigger {/beh/arb_inst/grant1}
added for sampling and triggering to iice: IICE
Total instrumentation in bits: Sample Only 27, Trigger Only 5, Sample and trigger 13
Group wise instrumentation in bits:
Groupdefault:Sample Only 27, Sample and trigger 13

```

To disable a signal for sampling or triggering, select the signal on the RTL tab and then select Not instrumented from the popup menu; the watchpoint icon will again be clear (unfilled).

Note: You can use Find to recursively search for signals and then instrument selected signals directly from the Find dialog box (see [Searching for Design Objects, on page 46](#)).

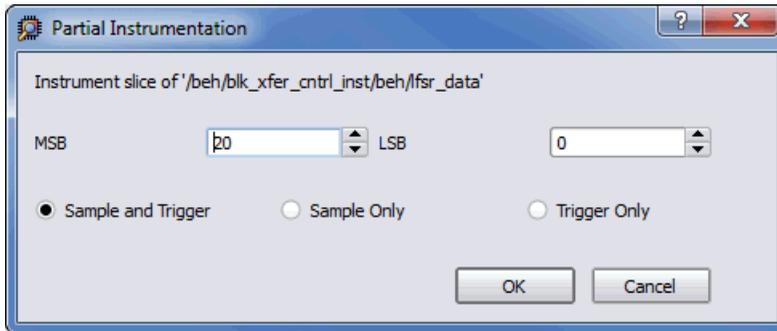
Instrumenting Buses

Entire buses, individual bits, or groups of bits of a bus can be individually instrumented.

Instrumenting a Partial Bus

To instrument a sequence (range) of bits of a bus:

1. Place the cursor over a bus that is not fully instrumented and select Add Partial Instrumentation to display the following dialog box.



2. In the dialog box, enter the most- and least-significant bits in the MSB and LSB fields. Note that the bit range specified is contiguous; to instrument non-contiguous bit ranges, see the section, [Instrumenting Non-Contiguous Bits or Bit Ranges](#), on page 29.

Note: When specifying the MSB and LSB values, the index order of the bus must be followed. For example, when defining a partial bus range for bus [63:0] (or “63 downto 0”), the MSB value must be greater than the LSB value. Similarly, for bus [0:63] (or “0 upto 63”), the MSB value must be less than the LSB value.

3. Select the type of instrumentation for the specified bit range from the radio buttons and click OK.

When you click OK, a large letter “P” is displayed to the left of the bus name in place of the watchpoint icon. The color of this letter indicates if the partial bus is enabled for triggering only (red), for sampling only (blue), or for both sampling and triggering (green).

```

41 port (
42     Ⓜ clk           : in
43     Ⓜ reset        : in
44     Ⓜ P adr_o      : out
45     Ⓜ block_size   : out

```

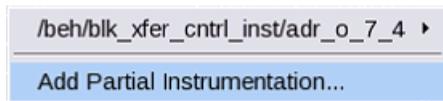
Instrumenting Single Bits of a Bus

To instrument a single bit of a bus, enter the bit value in the MSB field of the Add partial bus dialog box, leave the LSB field blank, and select the instrumentation type from the drop-down menu as previously described.

Instrumenting Non-Contiguous Bits or Bit Ranges

To instrument non-contiguous bits or bit ranges:

1. Instrument the first bit range or bit as described in one of the two previous sections.
2. Re-position the cursor over the bus, click the right mouse button, and again select Add partial instrumentation to redisplay the Add partial bus dialog box. Note that the previously instrumented bit or bit range is now displayed.



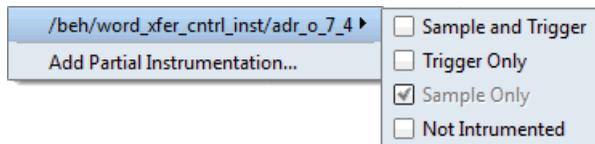
3. Specify the bit or bit range to be instrumented as previously described, select the type of instrumentation from the drop-down menu, and click OK. If the type of instrumentation is different from the existing instrumentation, the letter “P” will be yellow to indicate a mixture of instrumentation types.

Note: Bits cannot overlap groups (a bit cannot be instrumented more than once).

Changing the Instrumentation Type

To change the instrumentation type of a partial bus:

1. Position the cursor over the bus and click the right mouse button.
2. Highlight the bit range or bit to be changed and select the new instrumentation type from the adjacent menu.



Note: The above procedure is also used to remove the instrumentation from a bit or bit range by selecting Not instrumented from the menu.

Partial Instrumentation

Partial instrumentation allows fields within a record or a structure to be individually instrumented. Selecting a compatible signal for instrumentation, either on the RTL tab or through the Instrumentor Search dialog box, enables the partial instrumentation feature and displays a dialog box where the field name and its type of instrumentation can be entered.

When instrumented, the signal is displayed with a P icon in place of the watchpoint (glasses) icon to indicate that portions of the record are instrumented. The P icon is the same icon that is used to show partial instrumentation of a bus and uses a similar color coding:

- Green – all fields of the record are instrumented for sample and trigger
- Blue – all fields of the record are instrumented for sample only
- Red – all fields of the record are instrumented for trigger only
- Yellow – not all fields of the record are instrumented the same way

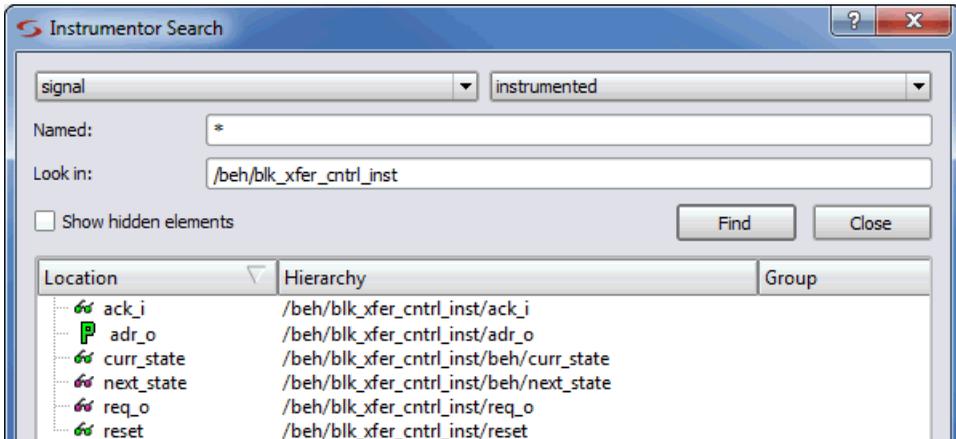
The figure below shows the partial instrumentation icon on signal tt. The yellow color indicates that the individual fields (tt.r2 and tt.c2) are assigned different types of instrumentation.

```

31
32 signal P tt: matrix_element1;
33 begin
34   P tt.r2 <= <<r2;
35   P tt.c2 <= <<c2;
36   P tt.ele.r1 <= <<r1;

```

The Instrumentor Search dialog also uses the partial instrumentation icon to show the state of instrumentation on fields of partially instrumented records.

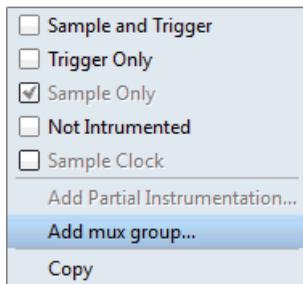


Note: Partial instrumentation can only be added to a field or record one slice level down in the signal hierarchy.

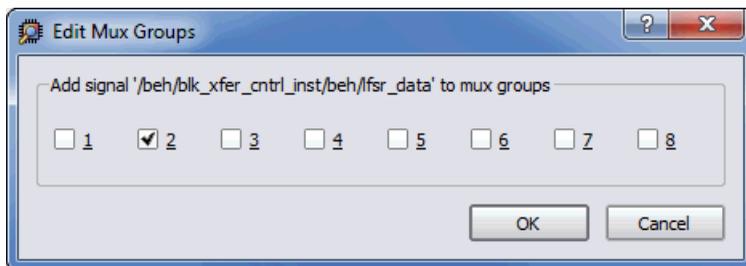
Multiplexed Groups

Multiplexed groups allow signals to be assigned to logical groups. Using multiplexed groups can substantially reduce the amount of pattern memory required during subsequent debugging when all of instrumented signals are not required to be loaded into memory at the same time.

Only signals or buses that are instrumented as either Sample and Trigger or Sample only can be added to a multiplexed group. To create multiplexed groups, right click on each individual instrumented signal or bus and select Add mux group from the popup menu.



In the Add mux group dialog box displayed, select a corresponding group by checking the group number and then click OK to assign to the signal or bus to that group. A signal can be included in more than one group by checking additional group numbers before clicking OK.



When assigning instrumented signals to groups:

- A maximum of eight groups can be defined; signals can be included in more than one group, but only one group can be active in the debugger at any one time.
- Signals instrumented as Sample Clock or Trigger only cannot be included in multiplexed groups.

- Partial buses cannot be assigned to multiplexed groups.
- The signals group command can be used to assign groups from the console window (see [signals](#), on page 78 of the *Reference Manual*). Command options allow more than one instrumented signal to be assigned in a single operation and allow the resultant group assignments to be displayed.

For information on using multiplexed groups in the debugger, see [Selecting Multiplexed Instrumentation Sets](#), on page 23 in the *Debugger User Guide*.

Sampling Signals in a Folded Hierarchy

When a design contains entities or modules that are instantiated more than once, it is termed to have a *folded* hierarchy (folded hierarchies also occur when multiple instances are created within a generate loop). By definition, there will be more than one instance of every signal in a folded entity or module. To allow you to instrument a particular instance of a folded signal, the instrumentor automatically recognizes folded hierarchies and presents a choice of all possible instances of each signal within the hierarchy.



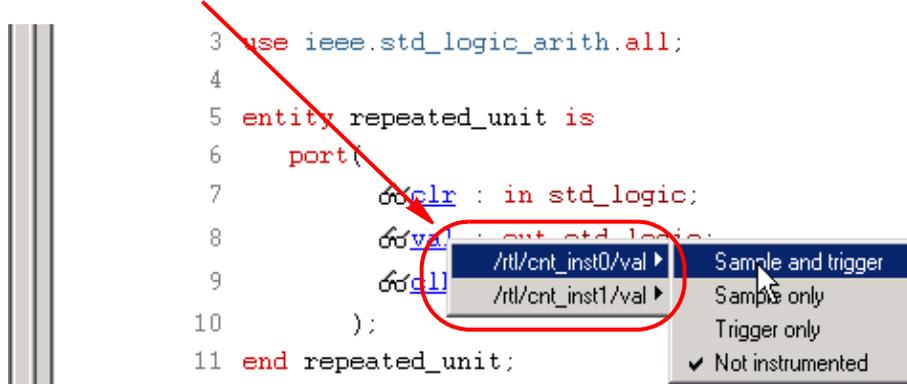
The choices are displayed in terms of an absolute signal path name originating at the top-level entity or module. The list of choices for a particular signal is accessed by clicking the watchpoint icon or corresponding signal.

The example below consists of a top-level entity called `two-level` and two instances of the `repeated_unit` entity. The source code of `repeated_unit` is displayed, and the list of instances of the `val` signal is displayed by clicking on the watchpoint icon or the signal name. Two instances of the signal `val` are available for sampling:

```
/rtl/cnt_inst0/val  
/rtl/cnt_inst1/val
```

Either, or both, of these instances can be selected for sampling by selecting the signal instance and then sliding the cursor over to select the type of sampling to be instrumented for that signal instance.

The list of instrumentable instances of signal **val**



The color of the watchpoint icon is determined as follows:

- If no instances of the signal are selected, the watchpoint icon is clear.
- If some, but not all, instances of the signal are defined for sampling, the watchpoint icon is yellow.
- If all instances are defined for sampling, the color of the watchpoint icon is determined by the type of sampling specified (all instances sample only: blue, all instances trigger only: red, all instances sample and trigger: green, all instances in any combination: yellow).

Alternately, any of the instances of a folded signal can be selected or deselected at the instrumentor console window prompt by using the absolute path name of the instance. For example,

```
signals add /rtl/cnt_inst1/val
```

See the *Reference Manual* for more information.

To disable an instance of a signal that is currently defined for sampling, click on the watchpoint icon or signal, select the instance from the list displayed, and select Not instrumented.

For related information on folded hierarchies in the debugger, see [Activating/Deactivating Folded Instrumentation, on page 24](#) [Displaying Data from Folded Signals, on page 32](#) in the *Debugger User Guide*.

Instrumenting the Verdi Signal Database

The instrumentor can import signals directly from the Verdi platform. After performing behavioral analysis and generating the essential signal database (ESDB), the essential signal list from the Verdi platform is brought directly into the instrumentor where the signals are instrumented. To bring in the essential signal list:

1. Load the project into the instrumentor.
2. Parse the essential signal list from the ESDB using the command:

```
verdi getsignals ESDBpath
```

In the above syntax, *ESDBpath* is the location where `es.esdb++` is installed. For example:

```
verdi getsignals path/es
```

3. Instrument the essential signal list using the command:

```
verdi instrument
```

The signals are automatically instrumented as sample and trigger.

4. Instrument the sample clock (a sample clock is required by the instrumentor).
5. Configure the IICE and instrument the design.

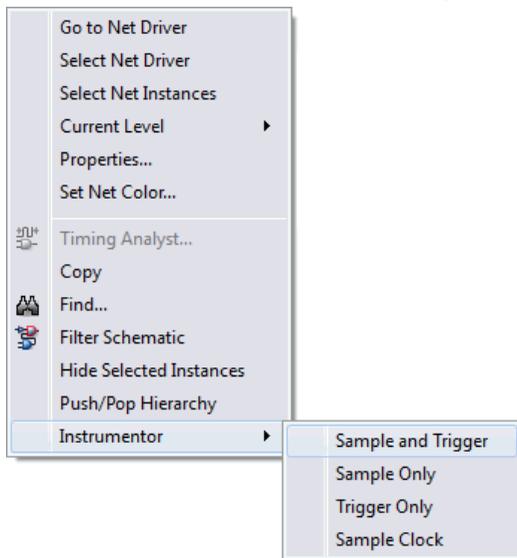
The instrumented design is then synthesized, placed and routed, and programmed into the FPGA. The debugger samples the data and generates the fast signal database (FSDB) which is then displayed in the Verdi nWave viewer. For more information on the fast signal database and using the Verdi nWave viewer, see [Generating the Fast Signal Database, on page 53](#) in the *Debugger User Guide*.

Instrumenting Signals Directly in the idc File

In addition to the methods described in the previous sections, signals can be instrumented directly within the HDL Analyst (SRS file) outside of the instrumentor. This methodology facilitates updates to a previous instrumentation and also allows signals within a parameterized module, which were previ-

ously unavailable for instrumentation, to be successfully instrumented. This technique is referred to as “post-compile instrumentation.” To instrument a signal using this technique:

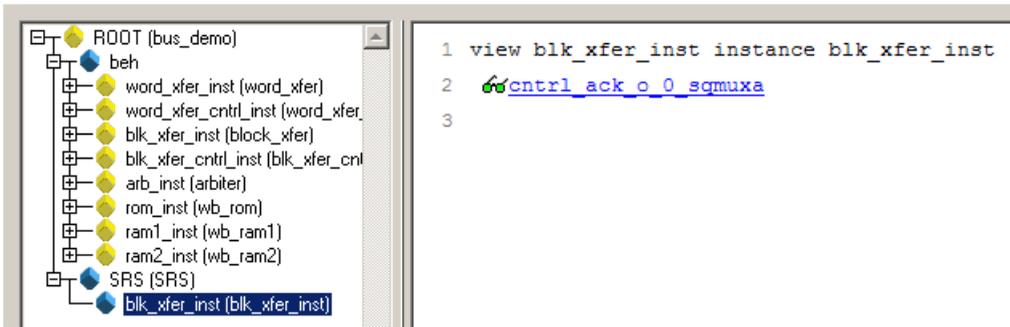
1. Save the instrumented design in the synthesis tool to create the IDC file.
2. Open the RTL view (SRS file) by clicking the View the schematic icon.
3. In the schematic view, highlight the net of the signal to be instrumented.
4. With the net highlighted, click the right mouse button, select Instrumentor from the popup menu, and select the type of instrumentation to be applied.



When selected, the instrumentation is automatically applied to the open instrumentor view.

5. Save the updated instrumentation and rerun compilation.

When you open the debugger, an SRS entry is included in the hierarchy browser; selecting this entry displays the additional signal or signals added to the instrumentation. Selecting a signal in the instrumentation window brings up the Watchpoint Setup dialog box to allow a trigger expression to be assigned to the defined signal.

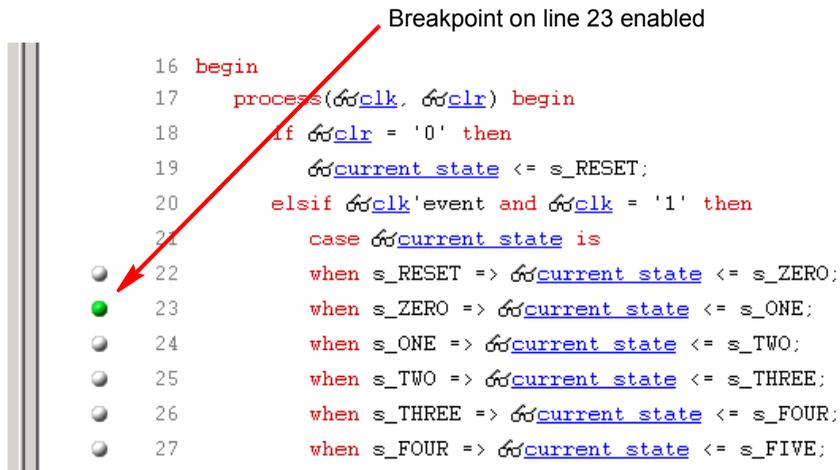


Note that trigger expressions on signals added to the instrumentation must use the VHDL style format.

Selecting Breakpoints



Breakpoints are used to trigger data sampling. Only the breakpoints that are instrumented in the instrumentor can be enabled as triggers in the debugger. To instrument a breakpoint in the instrumentor, simply click on the circular icon to the left of the line number. The color of the icon changes to green when enabled.



Once a breakpoint is instrumented, the instrumentor creates trigger logic that becomes active when the code region in which the breakpoint resides is active.

In the above example, the code region of the instrumented breakpoint is active if the variable `current_state` is state zero (`s_ZERO`) and the signal `clr` is not '0' when the clock event occurs.

Selecting Breakpoints Residing in Folded Hierarchy

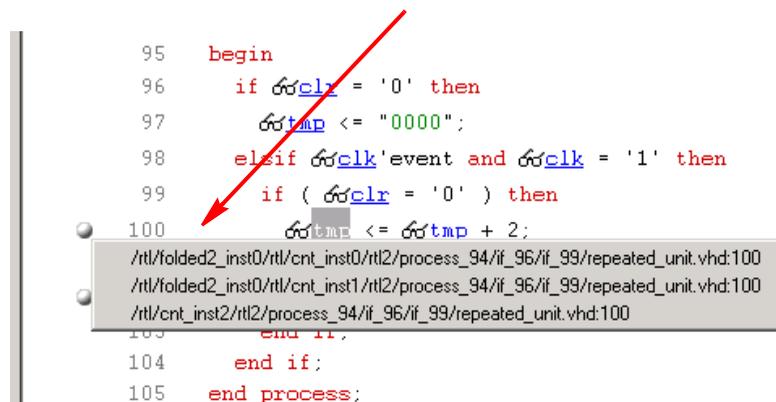
If a design contains entities or modules that are instantiated more than once, the design is termed to have *folded* hierarchy. By definition, there will be more than one instance of every breakpoint in a folded entity or module. To allow you to instrument a particular instance of a folded breakpoint, the instrumentor automatically detects folded hierarchy and presents a choice of all possible instances of each breakpoint.

The choices are displayed in terms of an absolute breakpoint path name originating at the top-level entity or module. The list of choices for a particular breakpoint is accessed by clicking on the breakpoint icon to the left of the line number.

The example below consists of a top-level entity called `top` and two instances of the `repeated_unit` entity. The source code of `repeated_unit` is displayed; the list of instances of the breakpoint on line 100 is displayed by clicking on the breakpoint icon next to the line number. As shown in the following figure, three instances of the breakpoint are available for sampling.

Any or all of these breakpoints can be selected by clicking on the corresponding line entry in the list displayed.

Folded breakpoint on line 100 selected



```

95  begin
96  if clk = '0' then
97  tmp <= "0000";
98  elsif clk'event and clk = '1' then
99  if ( clr = '0' ) then
100 tmp <= tmp + 2;
    /rtl/folded2_inst0/rtl/cnt_inst0/rtl2/process_94/if_96/if_99/repeated_unit.vhd:100
    /rtl/folded2_inst0/rtl/cnt_inst1/rtl2/process_94/if_96/if_99/repeated_unit.vhd:100
    /rtl/cnt_inst2/rtl2/process_94/if_96/if_99/repeated_unit.vhd:100
101  end if;
104  end if;
105  end process;

```

The color of the breakpoint icon is determined as follows:

- If no instances of the breakpoint are selected, the icon is clear in color.
- If some, but not all, instances of the breakpoint are selected, the icon is yellow.
- If all instances are selected, the icon is green.

Alternately, any of the instances of a folded breakpoint can be selected or deselected at the instrumentor console window prompt by using the absolute path name of the instance. For example,

```
breakpoints add
  /rtl/inst0/rtl/process_18/if_20/if_23/repeated_unit.vhd:24
```

See the *Reference Manual* for more information.

The lines in the list of breakpoint instances act to toggle the selection of an instance of the breakpoint. To disable an instance of a breakpoint that has been previously selected, simply select the appropriate line in the list box.

Configuring the IICE



If the IICE configuration parameters for the active IICE need to be changed, use the Edit IICE settings icon to change them.

[Chapter 2, IICE Configuration](#), discusses how to set these parameters for both single- and multi-IICE configurations, and [Chapter 4, HAPS Deep Trace Debug](#) describes setting the parameters for the HAPS deep trace debug feature.

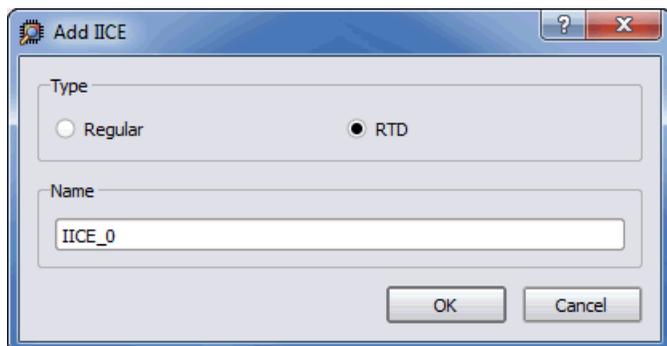
Real-time Debugging

Real-time debugging is a feature that provides scope or logic analyzer access to instrumented signals directly through a Mictor board interface connector installed on the HAPS board.

Enabling the Real-time Debugging Feature

To use the real-time debugging feature, a special IICE is defined in either the user interface or by command entry in the TCL Script shell.

To specify the IICE from the user interface, click the Add IICE icon to display the following dialog box. Select the RTD radio button and click OK.



To define the IICE from the TCL Script shell, enter the `iice new` command:

```
iice new [iiceID] -type rtd
```

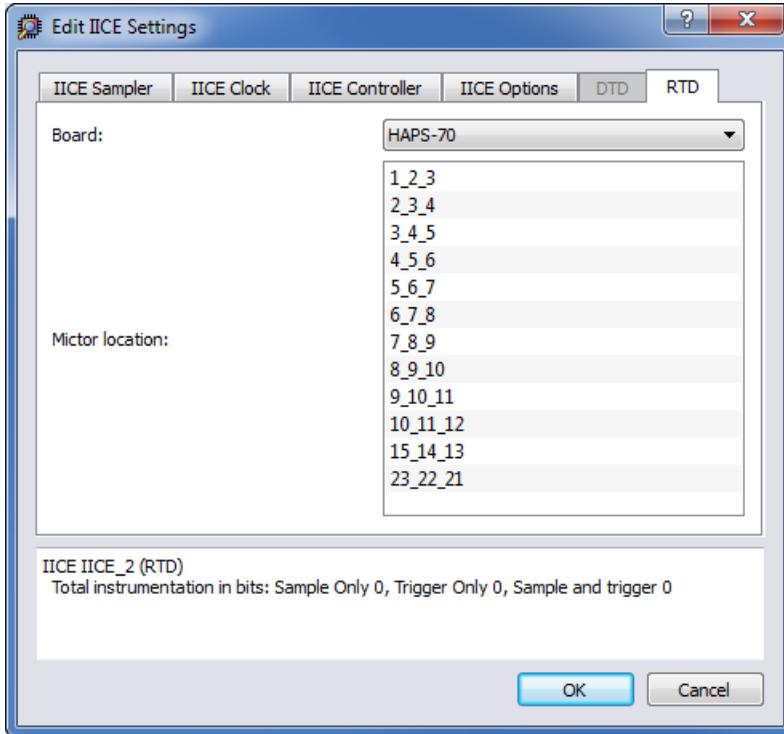
In the command syntax, *iiceID* is the name of the new IICE and, if omitted, defaults to an incremental number (for example, IICE_0).

Either of the above methods creates a new, real-time IICE for the design with all of the signals “not instrumented.”

Before you can instrument any of the signals, you must configure the Edit IICE Settings tab as outlined in the next section.

Edit IICE Settings Tab

The Edit IICE Settings tab for the real-time debugging feature includes a drop-down menu for selecting the Mictor daughter card locations. A HapsTrak[®] 3-to-HapsTrak II adapter is required.



On the EDIT IICE Settings tab:

1. Specify one or more Mictor board HapsTrak II connector locations by clicking on the connector set.
2. When finished with the above entries, click the OK button at the bottom of the tab.

Instrumenting the Real-Time Debug Signals

Instrumenting signals for real-time debugging is similar to normal instrumentation in that signal watchpoints and breakpoints are identified and activated in the instrumentation window. The exception is that the only watchpoint selection available from the popup menu for real-time debugging signals is Sample only.

```

288  00bus_ack1_t 00bus_ack1_t and 00ram1_ack and 00ram2_ack,
289  00ack1_t 00ack1_t d 00grant1,
290  00ack2_t 00ack2_t d 00grant2,
291  00bus_stb1_t 00bus_stb1_t ( 00grant1 = '1' ) else 00stb2,
292  00bus_we1_t 00bus_we1_t ( 00grant1 = '1' ) else 00we2,
293
294  -- bus c

```

Sample only

• Not instrumented

Sample Clock

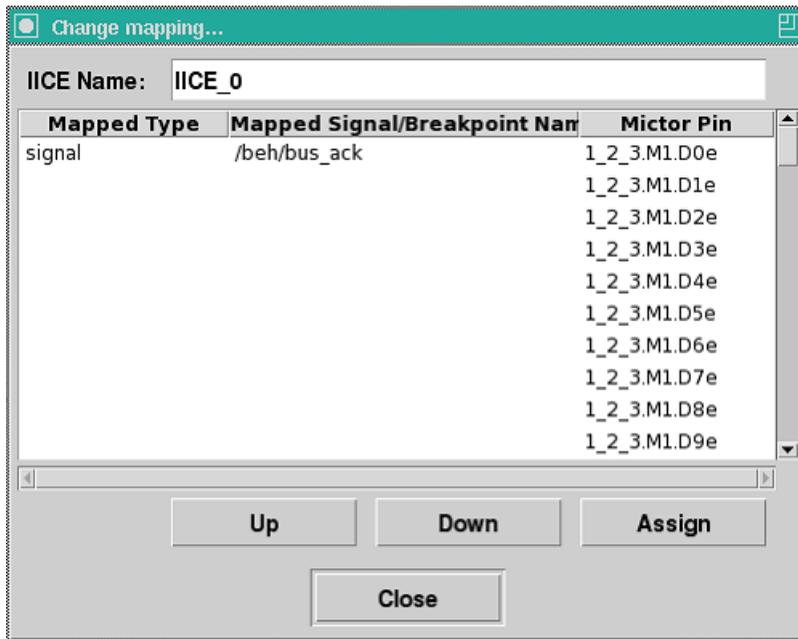
HAPS SRAM Clock

Add mux group...

Viewing the Signal Assignments



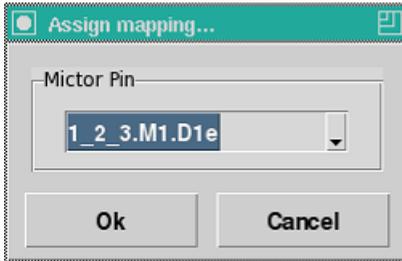
Watchpointed signals are automatically assigned to the specified Mictor daughter board pin locations. These assignments are listed in the Change mapping dialog box. To display the dialog box, click the RTD icon (Change 'RTD' type IICE signals/breakpoints mapping) in the top menu bar.



Individual assignments can be changed by highlighting the assignment to be changed and then either:

- moving the assignment up or down using the Up or Down buttons.

- clicking the Assign button to display the Assign mapping dialog box and then selecting the new pin location from the drop-down menu and clicking OK.



Logic Analyzer Interface

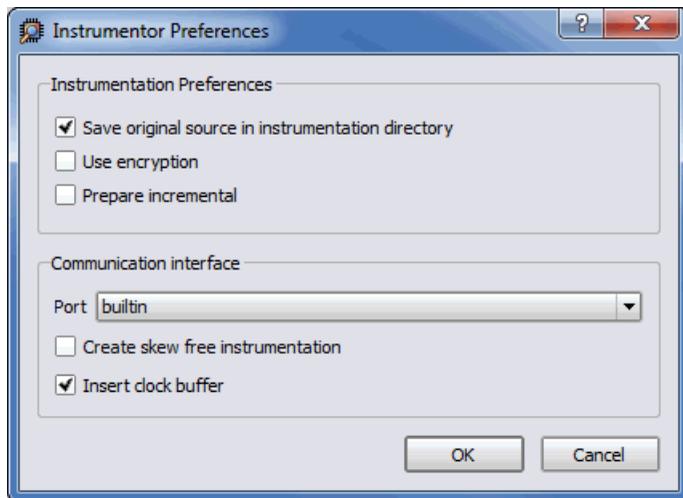
The logic analyzer interface at the Mictor connector is configured in the debugger (see [Logic Analyzer Interface Parameters](#), on page 54 in the *Debugger User Guide*).

Writing the Instrumented Design

To create the instrumented design, you must first complete the following steps:

1. Define a synthesis project with all source files defined
2. Specify IICE parameters/HAPS settings
3. Select signals to sample
4. Select breakpoints to instrument
5. Optionally include the original HDL source

To include the original HDL source with the exported design files, open the Instrumentor Preferences dialog box and enable the Save original source in instrumentation directory check box. If the original source is to be encrypted, additionally check the Use encryption check box.



Finally, select File->Save All from the main synthesis tool menu to capture your instrumentation. Saving a project's instrumentation generates an *instrumentation design constraints* (*idc*) file and adds compiler pragmas in the form of constraint files to the design RTL for the instrumented signals and break points. This information is then used by the synthesis tool to incorporate the instrumentation logic (IICE and COMM blocks) into the synthesized netlist. If you are including an encrypted HDL source (Use encryption box checked), you are first prompted to supply a password for the encryption.

Including Original HDL Source

Including the original HDL source with the instrumented project simplifies design transfer when instrumentation and debugging are performed on separate machines and is especially useful when a design is being debugged on a system that does not have access to the original sources.

To include the original HDL source, select the Save original source in instrumentation directory check box in the Instrumentor Preferences dialog box (click the Instrumentor Preferences icon to display the dialog box) before you save and instrument your project.

When the Use encryption check box is additionally selected, the original sources are encrypted when they are written. The encryption is based on a password that is requested when you write out the instrumented project. Encryption allows you to debug on a machine that you feel would not be sufficiently

secure to store your sources. After you export the files to the unsecure machine, you are prompted to reenter the encryption password when you open the design in the debugger. The decrypted files are never written to the unsecure machine's hard disk.

For maximum security when selecting an encryption password:

- use spaces to create phrases of four or more words (multiple words defeat dictionary-type matching)
- include numbers, punctuation marks, and spaces
- make passwords greater than 16 characters in length

Note: Passwords are the user's responsibility; Synopsys cannot recover a lost or forgotten password.

Synthesizing Instrumented Designs

When you save your instrumentation, the synthesis tool creates the set of files and subdirectories required by the debugger. These files and subdirectories are then exported from the database to an external directory location. This location can be local to your system (when running the debugger on the same machine) or the exported directory can be copied to a remote system using tar or file transfer protocol (FTP).

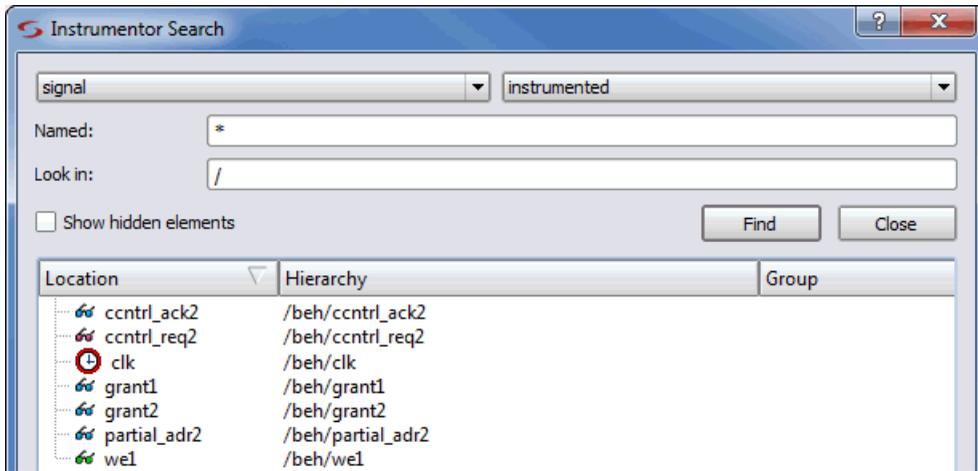
Listing Signals

The instrumentor includes a set of menu commands and, in most cases, icons for listing watchpoint and breakpoint conditions.

List Instrumented Signals



To view all of the signals currently instrumented in the entire design, click the Search instrumented signals icon. The result of listing the signals is displayed in the Instrument Search dialog box.



List Signals Available for Instrumentation



To see only the signals in the design available for instrumentation, click the Search non-instrumented signals icon.

List Instrumented Breakpoints



To list all of the breakpoints that have been instrumented, click the Search instrumented breakpoints icon.

List Breakpoints Available for Instrumentation



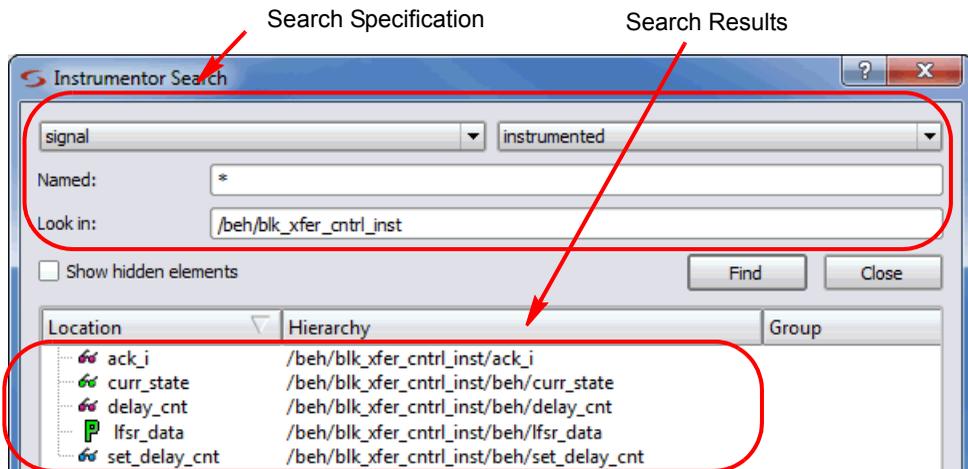
To list all of the breakpoints that are available for instrumentation, click the Search non-instrumented breakpoints icon.

Searching for Design Objects



The Instrumentor Search dialog box is a general utility to search for signals, breakpoints, and/or instances. To invoke the dialog box, click the Search icon.

The Instrumentor Search dialog box includes an area for specifying the objects to find and an area for displaying the results of the search.



The search specification includes these options:

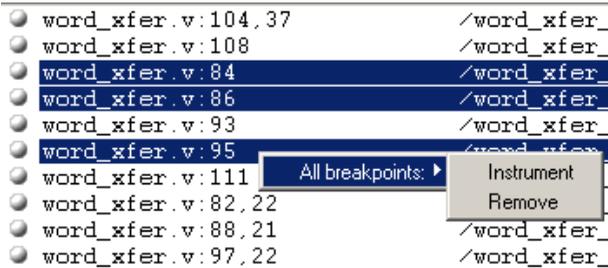
- Object type: – specify the type of object to search for from the drop-down menu: breakpoint, signal, instance, or “*” (any). The default is “*” (any).
- Status: – specify the status of the object to be found from the drop-down menu. The values can be instrumented, sample trigger, sample_only, trigger_only, not-instrumented, or “*” (any). The default is “*” (any).
- Named: – specify a name, or partial name to search for in the design. Wild cards are allowed in the name. The default is “*” (any).
- Look in: – specify the location in the design hierarchy to begin the recursive search. Root (“/”) is the default setting.

The search specification also includes a Show hidden elements check box. When this check box is enabled, the search also includes objects that would not normally be searched such as breakpoints in dead code.

The search results window shows each object found along with its hierarchical location. In addition, for breakpoints and signals, the results window includes the corresponding icon (watchpoint or breakpoint) that indicates the instrumentation status of the qualified signal or breakpoint.

To change the instrumentation status of a signal, click directly on the watchpoint icon and select the instrumentation type from the popup menu. You can use the Ctrl and Shift keys to select multiple signals and then apply the change to all of the selected signals. To toggle the instrumentation status of a

breakpoint, click the breakpoint icon. You also can use the Ctrl and Shift keys to select multiple breakpoints and then apply the change to all selected breakpoints from the popup menu.



TCL Script Window

To capture all text written to the synthesis tool's TCL Script window, use the log console command (see the *Reference Manual*).

To capture all commands executed in the console window use the transcript command (see the *Reference Manual*).

To clear the text from the console, use the clear command.

CHAPTER 4

HAPS Deep Trace Debug

The HAPS Deep Trace Debug feature is available to HAPS system users with Synopsys HAPS-60 and HAPS-70 series prototyping boards using any of the following memory daughter boards:

- DDR3_SODIMM_HT3 (4GB single-rank daughter board)
- DDR3_SODIMM2R_HT3 (8GB dual-rank daughter board)
- HAPS SRAM_HT3 (720MB daughter board)
- HAPS SRAM_1x1_HTII (288MB daughter board for HAPS-60 systems)

Using external memory for the sample buffer provides a significantly deeper, signal-trace buffer.

With the HAPS Deep Trace Debug mode, the Synplify/Identify flow remains unchanged. The only difference is in the configuration of a HAPS memory as the external sample buffer using IICE parameters.

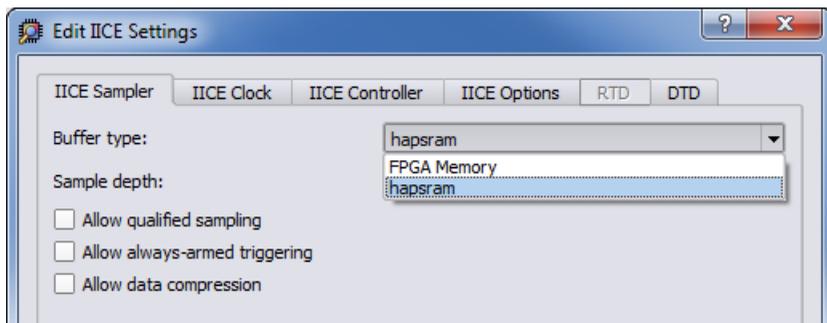
The HAPS deep-trace debug feature is described in the following sections:

- [External Memory Instrumentation and Configuration](#), on page 50
- [DTD Tab](#), on page 51
- [Running Deep Trace Debug with DDR3 Memory](#), on page 53
- [Running Deep Trace Debug with SRAM Memory](#), on page 55

External Memory Instrumentation and Configuration

With the HAPS Deep Trace Debug mode, the flow remains unchanged. The only difference is in the configuration of the additional memory as the sample buffer using IICE parameters.

The deep trace debug feature is enabled in the instrumentor from the IICE Sampler tab by setting the Buffer type to hapsram from the drop-down menu.

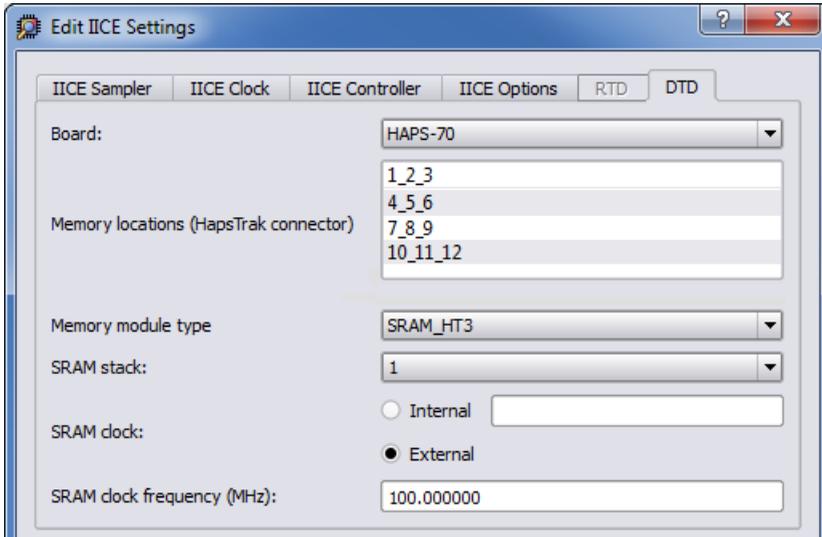


Selecting hapsram enables the DTD tab.

Note: Sample depth can only be set from the instrumentor and cannot be changed from within the debugger.

DTD Tab

The fields on the DTD tab vary according to the Buffer type parameter selected on the IICE Sampler tab and the HAPS board type specified in the synthesis tool (for example, setting the technology to Synopsys HAPS-70). The tab settings determine both the type of external memory to be used and memory configuration.



The individual parameters on the tab are defined in the following table. The parameters can also be set directly from the TCL Script window using the `iice sampler` command (see [Instrumentor iice sampler Options](#), on page 57 in the *Reference Manual* for complete syntax).

Parameter	Description
Board	The Board parameter is determined by the HAPS board configuration being used by the synthesis tool and cannot be changed within the instrumentor.
Memory locations	Specifies the HapsTrak connector location or location matrix where the daughter card or cards are installed. Connector selection where the daughter cards are physically connected is done by selecting one or more HapsTrak locations (locations 1 through 6 for HAPS-60 or a matrix location for HAPS-70) of the daughter cards for the FPGA under debug.
Memory module type	The HapsTrak daughter card type is selected using this drop-down option. The daughter card types available are determined by the Board type.
SRAM stack	Sets the stack depth for the external SRAM memory to allow card stacking. The depth of SRAM on each daughter card is 4M locations of 72-bit words for HTII SRAM cards and 8M locations of 90-bit words for HT3 SRAM cards. To increase the external SRAM memory depth beyond 4M x 72 or 8M x 90, the daughter cards can be stacked. For the HTII type SRAM, 1, 2, or 4 daughter cards can be stacked for the selected SRAM location and for HT3 type SRAM cards 1 or 2 cards can be stacked. The stack number specified applies to all connector locations specified by SRAM locations.
SRAM clock	The clock to the SRAM daughter card can originate from the clock used within the design (Internal) or from an external clock source present on the HAPS board (see SRAM Clocks, on page 56).
SRAM clock frequency	Specifies the frequency of the clock source to the SRAM. The supported SRAM operating frequency ranges for various HAPS board and SRAM card stacks using the FPGA internal PLL output as the SRAM clock are listed in SRAM Clocks, on page 56 .

Running Deep Trace Debug with DDR3 Memory

The following steps provide an overview of running deep trace debug using the memory on either the DDR3_SODIMM_HT3 or DDR3_SODIMM2R_HT3 daughter board.

1. In the synthesis software, compile the design, highlight the implementation, and select New Identify Implementation from the drop-down menu.
2. Highlight the Identify implementation and select Launch Instrumentor from the drop-down menu.
3. In the instrumentor, complete the instrumentation of the design and click the Edit IICE settings icon (); the IICE Sampler tab opens by default.
4. Set the Buffer type to hapsram and make sure that the sample depth is set to the intended depth (once set in the instrumentor, the sample depth setting cannot be changed in the debugger).
5. Select the DTD tab and set the Memory module type from the drop-down menu.
6. Save the IICE settings and save the instrumented design. You can close the instrumentor.
7. Run synthesis on the instrumented design, run place and route, and generate the bit file. If you intend to debug the design on a different system, copy the required files to the target host (see [Debugging on a Different Machine](#), on page 44 in the *Debugger User Guide*).

When you debug the design later, the tool automatically calculates the sample depth and source clock based on the configuration settings you supplied. The configured sample depth can be varied dynamically in the debugger from the minimum depth to the maximum configured depth.

To maximize performance when using DDR3 memory, use the guidelines in the table below to determine the sample frequency based on the number of sample bits being instrumented. The maximum number of instrumented bits that can be sampled with DDR3 memory is 2042.

Instrumented Bits	Max Sample Frequency	Max Sample Depth (4GB single rank)	Max Sample Depth (8GB dual rank)
1 to 250	140 MHz	134,217,727	268,435,455
251 to 506	70 MHz	67,108,863	134,217,727
507 to 1018	35 MHz	33,554,431	67,108,863
1019 to 2042	17.5 MHz	16,777,215	33,554,431

Running Deep Trace Debug with SRAM Memory

To configure the SRAM for deep trace debug:

1. In the synthesis software, compile the design, highlight the implementation, and select **New Identify Implementation** from the drop-down menu.
2. Highlight the **Identify** implementation and select **Launch Instrumentor** from the drop-down menu.
3. In the instrumentor, complete the instrumentation of the design and click the **Edit IICE Settings** icon (); the **IICE Sampler** tab opens by default.
4. Set the **Buffer type** to **hapsram** and make sure that the sample depth is set to the intended depth (once set in the instrumentor, the sample depth setting cannot be changed in the debugger).
5. Select the **DTD** tab and set the following parameters:
 - **Memory locations** – select the HapsTrak connector location where the daughter card is physically installed. On a HAPS-60 system, connector locations are identified as 1 to 6; on a HAPS-70 system, the connector locations are identified as a series of three adjacent locations (e.g., 1-2-3, 4_5_6, 7_8_9, etc.).
 - **SRAM stack** – specify the number of SRAM daughter cards stacked at the connector location.
 - **Memory module type** – specify the board type from the drop-down menu according to your board type as shown in the table below:

System Type	Board Selection
HAPS-60	SRAM_1x1_HTII
HAPS-70	SRAM_HT3

- **SRAM clock** – select either **Internal** or **External**. If **Internal** is selected, enter the name of the internal clock in the adjacent field. For more information on clocks, see [SRAM Clocks](#), on page 56.

- SRAM clock frequency – specify the SRAM clock frequency. For better performance, it is recommended that you use FPGA internal PLL output as the source of the SRAM clock.
6. Save the IICE settings and save the instrumented design. You can close the instrumentor.
 7. Run synthesis on the instrumented design, run place and route, and generate the bit file. If you intend to debug the design on a different system, copy the required files to the target host (see [Debugging on a Different Machine](#), on page 44 in the *Debugger User Guide*).

When you debug the design later, the tool automatically calculates the sample depth and source clock based on the configuration settings you supplied. The configured sample depth can be varied dynamically from the minimum depth to the maximum configured depth.

SRAM Clocks

When the clock source is internal to the design, any clock signal within the design at any hierarchy level can be instrumented as the SRAM clock. When the clock source is external, specify a suitable pin-lock constraint in the synthesis constraint file for the `deepbuf_sclk_iiceName_p` and `deepbuf_sclk_iiceName_n` ports (these ports are created automatically in the instrumented design). Provide the external clock source to this FPGA port.

Because of performance considerations, users are recommended to use FPGA internal PLL output as the source of the SRAM clock. The supported SRAM operating frequency ranges for SRAM card stacks using the internal PLL output as the SRAM clock are:

SRAM Type	SRAM_1x1_HTII (2.5V)	SRAM_HT3 (1.8V)
Board Type	HAPS-60 Series	HAPS-70 Series
1 SRAM stack	96 to 155 MHz	150 MHz
2 SRAM card stack	92 to 116 MHz	100 MHz
3 SRAM card stack	Not Supported	Not Supported
4 SRAM card stack	80to 110 MHz	Not Supported

Sample Depth Calculation

For a given, user-defined SRAM configuration setting, the maximum allowed depth can be calculated based on the formula described below.

- Number of HapsTrak slots used: N_{slot}
- Number of SRAM cards stacked: $NSRAM$
- Number of 72-bit or 90-bit words per SRAM card: N_{word} (4194304 for HapsTrak II; 8388608 for HapsTrak 3)
- Number of signals to be sampled (instrumented): N_{signal}

$$K_{sample} \leq \left\lceil \frac{N_{word} N_{SRAM}}{\frac{N_{signal} + 6}{72 N_{slot}}} \right\rceil$$

HapsTrak II

$$K_{sample} \leq \left\lceil \frac{N_{word} N_{SRAM}}{\frac{N_{signal} + 6}{90 N_{slot}}} \right\rceil$$

HapsTrak 3

For example, if $N_{slot} = 1$, $NSRAM = 1$, $N_{word} = 8M$ (8388608) and $N_{signal} = 1900$, the maximum sampling depth for K samples for the SRAM card is 396k.

Sample Clock Calculation

For a given set of user-defined external memory configuration settings, the sample clock frequency can be estimated using the formula described below.

$$f_{sampling} \leq \left\lceil \frac{f_{SRAM}}{\frac{N_{signal} + 6}{72 N_{slot}}} \right\rceil + 2$$

HapsTrak II

$$f_{sampling} \leq \left\lceil \frac{f_{SRAM}}{\frac{N_{signal} + 6}{90 N_{slot}}} \right\rceil + 2$$

HapsTrak 3

In the above expressions:

- Number of HapsTrak slots used: N_{slot}
- Number of signals to be sampled (instrumented): N_{signal}
- SRAM bus frequency: f_{SRAM}

For example, if $f_{SRAM} = 100MHz$, $N_{slot} = 1$, and $N_{signal} = 1900$, the maximum sampling frequency is 3.44MHz.

CHAPTER 5

Support for Instrumenting HDL

The debug environment fully supports the synthesizable subset of both Verilog and VHDL design languages. Designs that contain a mixture of VHDL and Verilog can be debugged – the software reads in your design files in either language.

There are some limitations on which parts of a design can be instrumented by the instrumentor. However, in all cases you can always instrument all other parts of your design.

The instrumentation limitations are usually related to language features. These limitations are described in this chapter.

- [VHDL Instrumentation Limitations](#), on page 60
- [Verilog Instrumentation Limitations](#), on page 62
- [SystemVerilog Instrumentation Limitations](#), on page 65

VHDL Instrumentation Limitations

The synthesizable subsets of VHDL IIEEE 1076-1993 and IEEE 1076-1987 are supported in the current release of the debugger.

Design Hierarchy

Entities that are instantiated more than once are supported for instrumentation with the exception that signals that have type characteristics specified by unique generic parameters cannot be instrumented.

Subprograms

Subprograms such as VHDL procedures and functions cannot be instrumented. Signals and breakpoints within these specific subprograms cannot be selected for instrumentation.

Loops

Breakpoints within loops cannot be instrumented.

Generics

VHDL generic parameters are fully supported as long as the generic parameter values for the entire design are identical during both instrumentation and synthesis.

Transient Variables

Transient variables defined locally in VHDL processes cannot be instrumented.

Breakpoints and Flip-flop Inferencing

Breakpoints inside flip-flop inferring processes can only be instrumented if they follow the coding styles outlined below:

For flip-flops with asynchronous reset:

```
process (clk, reset, ...) begin
  if reset = '0' then
    reset_statements;
  elsif clk'event and clk = '1' then
    synchronous_assignments;
  end if;
end process;
```

For flip-flops with synchronous reset or without reset:

```
process (clk, ...) begin
  if clk'event and clk = '1' then
    synchronous_assignments;
  end if;
end process;
```

Or:

```
process begin
  wait until clk'event and clk = '1'
    synchronous_assignments;
end process;
```

The reset polarity and clock-edge specifications above are only exemplary. The debug software has no restrictions with respect to the polarity of reset and clock. A coding style that uses wait statements must have only one wait statement and it must be at the top of the process.

Using any other coding style for flip-flop inferring processes will have the effect that no breakpoints can be instrumented inside the corresponding process. During design compilation, the instrumentor issues a warning when the code cannot be instrumented.

Verilog Instrumentation Limitations

The synthesizable subsets of Verilog HDL IEEE 1364-1995 and 1364-2001 are supported.

Subprograms

Subprograms such as Verilog functions and tasks cannot be instrumented. Signals and breakpoints within these specific subprograms cannot be selected for instrumentation.

Loops

Breakpoints within loops cannot be instrumented.

Parameters

Verilog HDL parameters are fully supported. However, the values of all the parameters throughout the entire design must be identical during instrumentation and synthesis.

Locally Declared Registers

Registers declared locally inside a named `begin` block cannot be instrumented and will not be offered for instrumentation. Only registers declared in the module scope and wires can be instrumented.

Verilog Include Files

There are no limitations on the instrumentation of `'include` files that are referenced only once. When an `'include` file is referenced multiple times as shown in the following example, the following limitations apply:

- If the keyword `module` or `endmodule`, or if the closing `'` of the module port list is located inside a multiply-included file, no constructs inside the corresponding module or its submodules can be instrumented.
- If significant portions of the body of an `always` block are located inside a multiply-included file, no breakpoints inside the corresponding `always` block can be instrumented.

If either situation is detected during design compilation, the instrumentor issues an appropriate warning message.

As an example, consider the following three files:

adder.v File

```
module adder (cout, sum, a, b, cin);
  parameter size = 1;
  output cout;
  output [size-1:0] sum;
  input cin;
  input [size-1:0] a, b;
  assign {cout, sum} = a + b + cin;
endmodule
```

adder8.v File

```
`include "adder.v"
module adder8 (cout, sum, a, b, cin);
  output cout;
  parameter my_size = 8;
  output [my_size - 1: 0] sum;
  input [my_size - 1: 0] a, b;
  input cin;
  adder #(my_size) my_adder (cout, sum, a, b, cin);
endmodule
```

adder16.v File

```
`include "adder.v"
module adder16 (cout, sum, a, b, cin);
  output cout;
  parameter my_size = 16;
  output [my_size - 1: 0] sum;
  input [my_size - 1: 0] a, b;
  input cin;
  adder #(my_size) my_adder (cout, sum, a, b, cin);
endmodule
```

There is a workaround for this problem. Make a copy of the include file and change one particular include statement to refer to the copy. Signals and breakpoints that originate from the copied include file can now be instrumented.

Macro Definitions

The code inside macro definitions cannot be instrumented. If a macro definition contains important parts of some instrumentable code, that code also cannot be instrumented. For example, if a macro definition includes the `case` keyword and the controlling expression of a case statement, the case statement cannot be instrumented.

Always Blocks

Breakpoints inside a synchronous flip-flop inferring an always block can only be instrumented if the always block follows the coding styles outlined below:

For flip-flops with asynchronous reset:

```
always @(posedge clk or negedge reset) begin
    if(!reset) begin
        reset_statements;
    end
    else begin
        synchronous_assignments;
    end;
end;
```

For flip-flops with synchronous reset or without reset:

```
always @(posedge clk) begin
    synchronous_assignments;
end process;
```

The reset polarity and clock-edge specifications and the use of `begin` blocks above are only exemplary. The instrumentor has no restrictions with respect to these other than required by the language.

For other coding styles, the instrumentor issues a warning that the code is not instrumentable.

SystemVerilog Instrumentation Limitations

The synthesizable subsets of Verilog HDL IEEE 1364-2005 (SystemVerilog) are supported with the following exceptions.

Typedefs

You can create your own names for type definitions that you use frequently in your code. SystemVerilog adds the ability to define new net and variable user-defined names for existing types using the typedef keyword. Only typedefs of supported types are supported.

Struct Construct

A structure data type represents collections of data types. These data types can be either standard data types (such as int, logic, or bit) or, they can be user-defined types (using SystemVerilog typedef). Signals of type structure can only be sampled and cannot be used for triggering; individual elements of a structure cannot be instrumented, and it is only possible to instrument (sample only) an entire structure. The following code segment illustrates these limitations:

```
module lddt_P_Struc_top (
  input sig sig_clk, sig sig_rst,
  .
  .
  .
  output struct packed {
    logic_nibble up_nibble;
    logic_nibble lo_nibble;
  } sig_oport_P_Struc_data
);
```

Cannot be instrumented
(no sampling and
no triggering)

Instrumentable only for
sampling; no triggering

In the above code segment, port signal sig_oport_P_Struc_data is a packed structure consisting of two elements (up_nibble and lo_nibble) which are of a user-defined datatype. As elements of a structure, these elements cannot be instrumented. The signal sig_oport_P_Struc_data can be instrumented for sampling, but cannot be used for triggering (setting a watch point on the signal is not allowed). If this signal is instrumented for sample and trigger, the instrumentor allows only sampling and ignores triggering.

Union Construct

A union is a collection of different data types similar to a structure with the exception that members of the union share the same memory location. Trigger-expression settings for unions are either in the form of serialized bit vectors or hex/integers with the trigger bit width representing the maximum available bit width among all the union members. Trigger expressions using enum are not possible.

The example below shows an acceptable sample code segment for a packed union; the trigger expression for union d1 can be defined as:

```
typedef union packed {
    shortint u1;
    logic signed [2:1][1:2][4:1] u2;
    struct packed {
        bit signed [1:2][1:2][2:1] st1;
        struct packed {
            byte unsigned st2;
        } u3_int;
    } u3;
    logic [1:2][0:7] u4;
    bit [1:16] u5;
} union_dt;

module top (
    input logic clk,
    input logic rst,
    input union_dt d1,
    output union_dt q1,
    ...

```

Arrays

Partial instrumentation of multi-dimensional arrays and multi-dimensional arrays of struct and unions are not permitted.

Interface

Interface and interface items are not supported for instrumentation and cannot be used for sampling or triggering. The following code segment illustrates this limitation:

```

interface ff_if (input logic clk, input logic rst,
    input logic din, output logic dout);
modport write (input clk, input rst, input din, output dout);
endinterface: ff_if

module top (input logic clk, input logic rst,
    input logic din, output logic dout) ;

    ff_if ff_if_top(.clk(clk), .rst(rst), .*);
    sff UUT (.ff_if_0(ff_if_top.write));
endmodule

```

In the above code segment, the interface instantiation of interface `ff_if` is `ff_if_top` which cannot be instrumented. Similarly, interface item `modport write` cannot be instrumented.

Port Connections for Interfaces and Variables

Instrumentation of named port connections on instantiations to implicitly instantiate ports is not supported.

Packages

Packages permit the sharing of language-defined data types, `typedef` user-defined types, parameters, constants, function definitions, and task definitions among one or more compilation units, modules, or interfaces. Instrumentation within a package is not supported.

Concatenation Syntax

The concatenation syntax on an array watchpoint signal is not accepted by the debugger. To illustrate, consider a signal declared as:

```
bit [3:0] sig_bit_type;
```

To set a watchpoint on this signal, the accepted syntax in the debugger is:

```
watch enable -iice IICE {/sig_bit_type} {4'b1001}
```

The 4-bit vector cannot be divided into smaller vectors and concatenated (as accepted in SystemVerilog). For example, the below syntax is not accepted:

```
watch enable -iice IICE {/sig_bit_type} {{2'b10,2'b01}}
```


Index

A

always-armed triggering 14

B

black boxes 23

breakpoint icon

 color coding 39

breakpoints

 finding 46

 in folded hierarchy 38

 instance selection 39

 listing available 46

 listing instrumented 46

 selecting 37

buses

 instrumenting partial 27

C

clocks

 edge selection 16

 sample 15

complex triggering 17

Configure IICE dialog box 10, 11, 13

 IICE Controller tab 16, 19

 IICE Sampler tab 13

console window operations 48

D

designs

 writing instrumented 43

dialog boxes

 Configure IICE 10, 11, 13

directories

 instrumentation 45

E

encrypting source files 44

essential signal database 35

F

files

 encrypting source 44

 idc 35

 IICE core 45

 project 8

folded hierarchy 33

H

hardware

 skew-free 12

HDL source

 including in project 44

hierarchy

 folded 33

hierarchy browser

 popup menu 22

hierarchy browser window 22

I

idc file

 editing 35

IICE

 configuration 9

IICE Controller tab 16, 19

IICE parameters

 buffer type 14

 common 11

 individual 10, 11, 13

 JTAG port 11

- IICE Sampler tab 13
- IICE settings
 - sample clock 15
 - sample depth 14
- instances
 - finding 46
- instrumentation
 - partial records 30
- instrumentation directory 45
- instrumenting partial buses 27
- J
- JTAG port
 - IICE parameter 11
- L
- limitations
 - Verilog instrumentation 62, 65
 - VHDL instrumentation 60
- M
- mixed language considerations 59
- multi-IICE
 - tabs 10, 11, 13
- multiplexed groups
 - assigning 32
- O
- objects
 - finding 46
- original source
 - including 44
- P
- parameterized modules
 - instrumenting 35
- parameters
 - IICE 9
 - IICE common 11
- partial buses
 - instrumenting 27
- passwords
 - encryption/decryption 44
- project files 8
- projects
 - instrumenting 7
- Q
- qualified sampling 14
- R
- RAM resources 14
- records
 - partially instrumented 30
- S
- sample clock 15
- sample clock calculation
 - SRAM 57
- sampling
 - in folded hierarchy 33
 - qualified 14
- sampling signals 25, 26, 33, 37, 39, 42, 43, 45, 46
- searches
 - objects 46
- settings
 - sample clock 15
 - sample depth 14
- signals
 - disabling sampling 27
 - exporting trigger 18
 - finding 46
 - instance selection 34
 - listing available 46
 - listing instrumented 45, 46
 - sampling selection 25, 26, 33, 37, 39, 42, 43, 45, 46
- simple triggering 17
- skew-free hardware 12

- source files
 - encrypting 44
- SRAM clocks 56
- state-machine triggering 17
- synthesizing designs 45
- T
- trigger signal
 - exporting 18
- triggering
 - always-armed 14
 - complex 17
 - simple 17
 - state machine 17
- V
- Verdi platform 35
- Verilog
 - instrumentation limitations 62, 65
- VHDL
 - instrumentation limitations 60
- W
- watch icon
 - color coding 34
- windows
 - hierarchy browser 22

