LiteFast IP

DG0720 Demo Guide

Power Matters.™

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1 Revision History

The following shows important changes made in this document for each revision.

Revision	Changes
Revision 1 (July 2016)	Initial release

Contents

Figures

Tables

2 Preface

2.1 Purpose

This demo guide is targeted to show the LiteFast IP demonstration on Microsemi SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) Security Evaluation Kit (090). The document gives the details of the configuration of IP and its validation process on the given board. It provides instructions about how to use the corresponding demo design.

The demo guide contains the following sections:

- Demo Design Features
- Validating the Design on SmartFusion2 Security Evaluation Kit

2.2 Intended Audience

This demo guide is intended for:

- FPGA designers
- Embedded designers
- System-level designers

2.3 References

The following documents are referred in this demo guide:

- *SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration*
- *CoreUART v5.4 Handbook*
- *UG0701: LiteFast IP User Guide*
- *CorePCS v3.3 Handbook*
- *UG0541: SmartFusion2 SoC FPGA Evaluation Kit User Guide*

3 Demo Design Features

3.1 Design Overview

LiteFast is a scalable, light weight in terms of utilization, high data rate protocol for high speed serial communication. LiteFast has an inbuilt flow control scheme and physical link is maintained when there is no application data for transmission.

Microsemi LiteFast IP has two distinct sections as transmitter and receiver. The LiteFast demo design includes the LiteFast transmitter and receiver sections, example design as part of the user application for traffic generation and frame checking and other components to demonstrate as validation suit. LiteFast transmitter packs the application data into data frame and initiates the data transmission. LiteFast receiver extracts application data from data frame and delivers the application data to the user interface. An idle frame is transmitted when there is no application data for transmission, the physical link between systems is maintained by idle frames.

For a given system of targeted application, the received data extracted from the data frame is written in to a receiver buffer. If available storage space of receiver buffer approaches to zero, LiteFast receiver notifies the remote LiteFast transmitter to pause data frame transmission, to prevent the overflow of receiver buffers. If available storage space of receiver buffer is greater than a threshold value, the LiteFast receiver would notify the remote LiteFast transmitter to resume data frame transmission.

Threshold value must be at least 128 bytes and upper limit of threshold is fixed by user application.

The following are the main features of LiteFast:

- Idle frame for establishing and maintaining the link and data frame for user data
- Flow control through token exchange
- Supports 1x or 2x or 4x per SERDES
- Supports cumulative speed from 4 Gbps to 10 Gbps for x4 lanes per SERDES
- Word alignment, block alignment, and lane alignment for receive chain
- Independent of user application and device
- Serial full duplex or serial simplex operation
- Supports CRC-32
- Supports hot plug
- Data packet size: 1~128 bytes of application data. The length of payload must be a multiple of eight, otherwise K28.4 bytes are filled to meet the requirement
- Idle packet: 8 byte
- Supports 8B10B encoding mechanism
- Support for little endian

LiteFast transmitter packs user data into data frame and generates idle frame. Frame data are striped on multiple lanes if multiple lanes are configured.

In multiple lanes LiteFast receiver, multiple lanes are aligned according to /A/ order sets, then LiteFast receiver un-strips all lanes together to get LiteFast data frame and idle frame. LiteFast receiver drops idle frame and extracts payload in data frame. LiteFast receiver monitors token field in the data and idle frames and provides the remote token value (used for flow control) to transmitter.

LiteFast IP data width supports 8bits/16bits/32bits/64bits and supports 1/2/4 lanes.

The following table lists the working mode supported by LiteFast IP.

Table 1 • **LiteFast IP Support Mode**

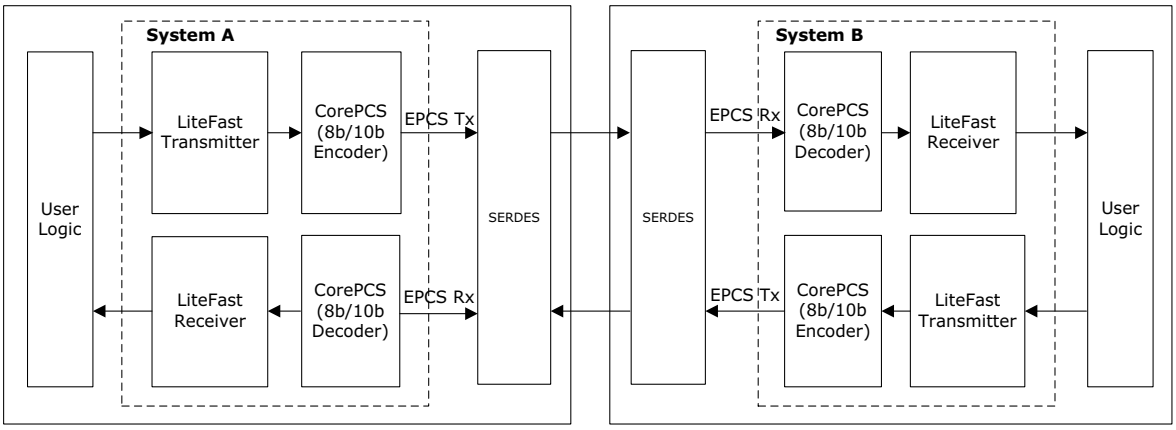
User Application Data Width	1 Lane	2 Lanes	4 Lanes
8 bits	Support	No	No
16 bits	Support maximum 16-bit per lane	Support maximum 8-bit per lane	No
32 bits	No	Support minimum 16-bit per lane	Support maximum 8-bit per lane
64 bits	No	No	Support maximum 16-bit per lane

Because the 8B10B IP (CorePCS) in Libero supports 8 bits or 16 bits data width, each lane data width can only be 8 bits or 16 bits. LiteFast IP supports maximum four lanes per SERDES.

Note: User has to instantiate CorePCS from Libero catalog and configure SERDES through SERDES configurator, for limitation on data width and serial lane bandwidth.

The following figure shows the demo design block diagram of the LiteFast demo.

Figure 1 • **Demo Design Block Diagram**



3.2 Device Family Support

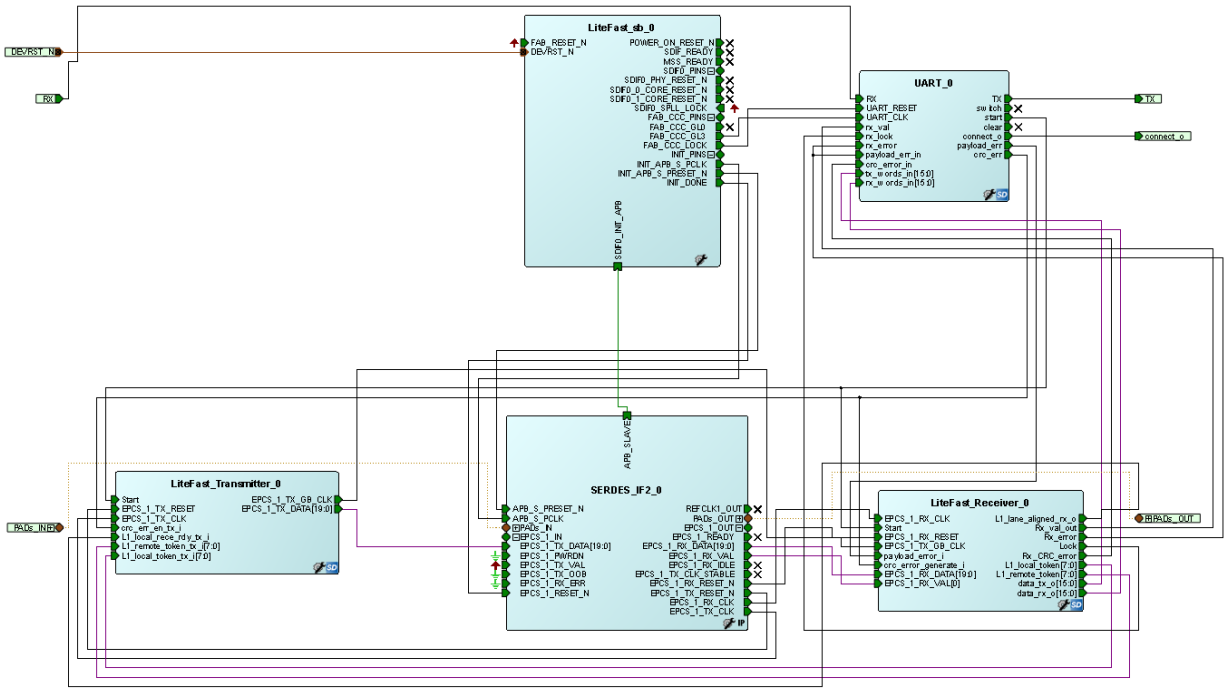
The Microsemi LiteFast IP supports the following FPGA devices:

- SmartFusion2 (All devices with transceivers in this family)
- IGLOO2 (All devices with transceivers in this family)
- RTG4™

3.3 Hardware Design

The hardware design for the implementation includes a LiteFast transmitter and LiteFast receiver blocks connected to the SmartFusion2 SERDES. UART block communicates with the GUI to send data and receive control signals. The top-level Smart Design diagram for the design is shown in Figure 2.

Figure 2 • **LiteFast Smart Design Top-Level Diagram**



3.3.1 CorePCS

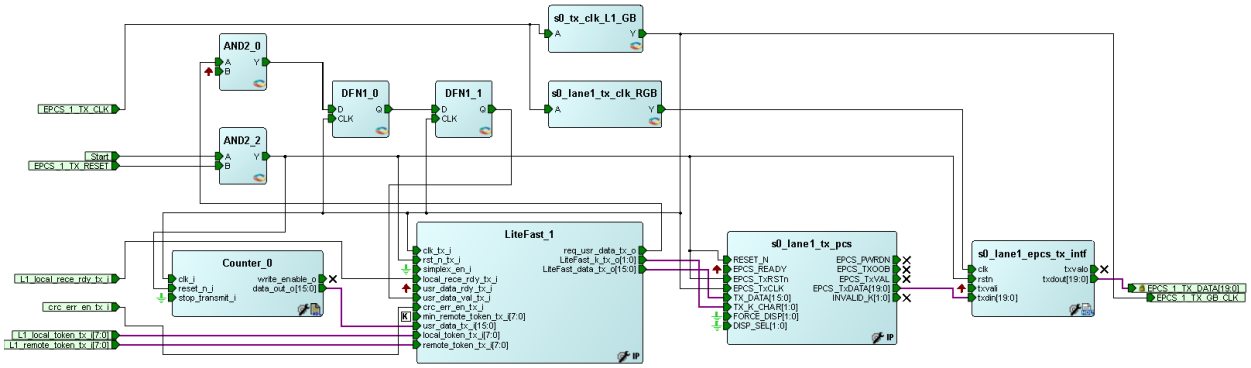
The CorePCS supports programmable 8B10B encoding/decoding. This Core can be configured as a transmitter, receiver, or both transmitter and receiver. Word alignment support is included in receiver. The Core can be configured to support 10-bit or 20-bit external physical coding sublayer (EPCS) data. Refer to *CorePCS v3.3 Handbook* for more information on CorePCS block.

3.4 Block Descriptions

3.4.1 LiteFast Transmitter

The LiteFast transmitter block contains a counter to generate data, LiteFast IP in transmitter mode, CorePCS block configured in transmitter only mode, and transmitter interface for SERDES. Figure 3 shows LiteFast smart design transmitter block.

Figure 3 • **LiteFast Transmitter Smart Design**



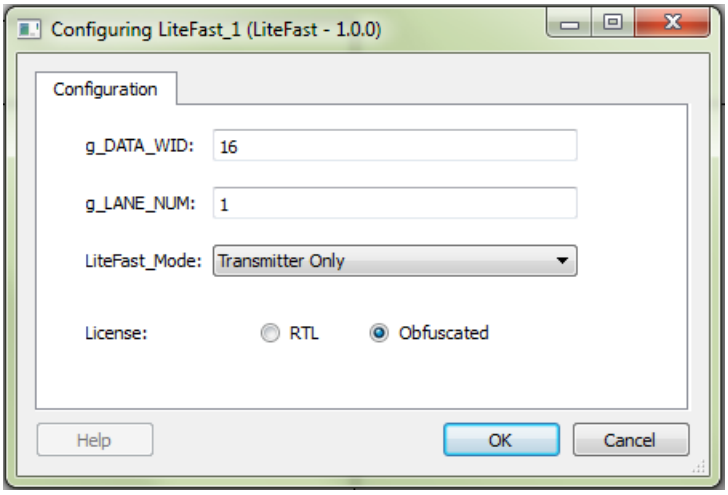
3.4.1.1 Counter

The counter block contains a 16-bit counter that transmits incremental data, each clock cycle.

3.4.1.2 LiteFast IP in Transmitter Mode

The Lite Fast IP is configured in transmitter only mode. The IP can be configured from IP's configurator window, as shown in Figure 4. The g_DATA_WID indicates the data width, g_LANE_NUM indicates the number of lanes to be configured. LiteFast_Mode contains the drop down in which Transmitter Only mode needs to be selected. For exact number of lane and data width choice, refer Table 1 on page 10.

Figure 4 • **LiteFast IP Transmitter Configurator**



3.4.1.3 CorePCS Transmitter

The CorePCS transmitter block multiplexes the control and data inputs on EPCS_TX_DATA. The CorePCS uses running disparity technique for 8B/10B encoding. The CorePCS output transmit interface is connected to SERDES EPCS transmit interface.

3.4.1.4 EPCS Transmit Interface

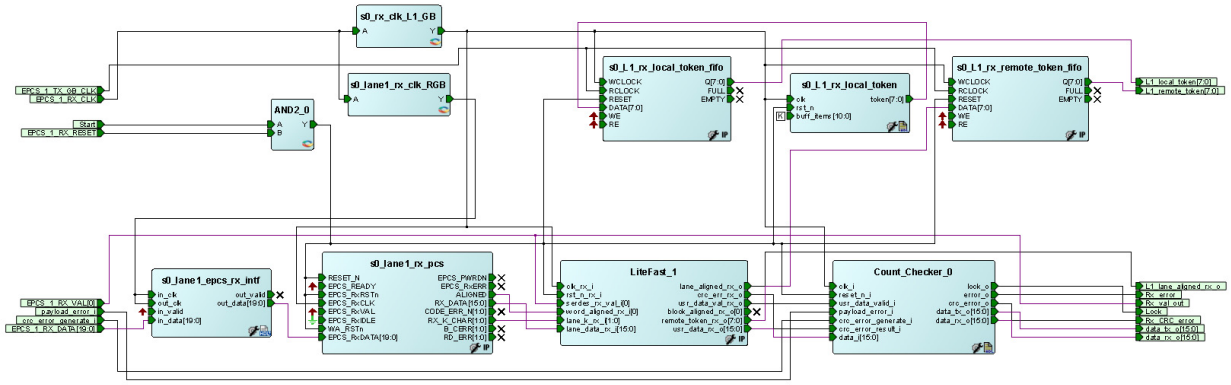
The EPCS transmit interface block is a fabric interface that synchronizes data between SERDES block and fabric modules.

It receives data from the fabric modules and transmits onto the SERDES.

3.4.2 LiteFast Receiver

The LiteFast receiver block contains a receiver interface from SERDES, LiteFast IP in receiver mode, CorePCS block configured in receiver only mode, and count checker block. It contains the local token generation block, remote token first in first out (FIFO), and local token FIFO. The smart design diagram for the LiteFast receiver block is shown in Figure 5.

Figure 5 • **LiteFast Receiver Smart Design**



3.4.2.1 EPCS Receive Interface

The EPCS receive interface block is a fabric interface that synchronizes data between SERDES block and Fabric modules.

It receives the data from SERDES and sends it to the fabric modules.

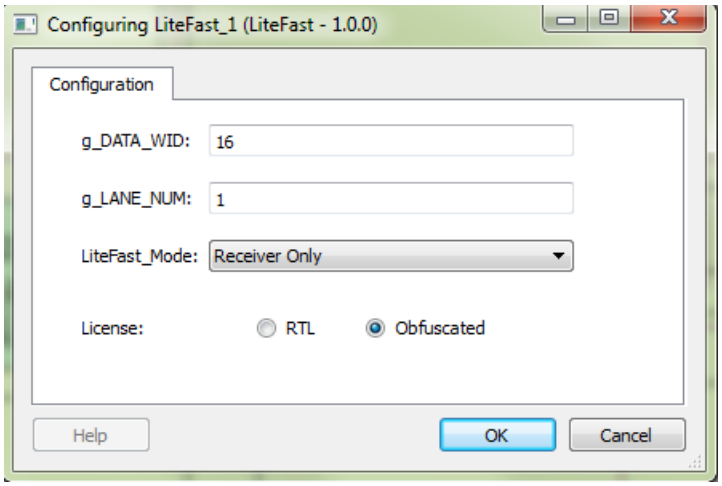
3.4.2.2 CorePCS Receiver

The CorePCS in the Rx chain implements 10B/8B decoding. RX_K_CHAR control signal output of CorePCS is used to indicate a control or data character.

3.4.2.3 LiteFast IP in Receiver Mode

The LiteFast IP is configured in the receiver only mode. In this mode it only receives data. The IP can be configured by double clicking the IP so that the configurator window opens, as shown in Figure 6. The g_DATA_WID indicates the data width, g_LANE_NUM indicates the number of lanes to be configured and LiteFast Mode contains the drop down in which Receiver Only mode needs to be selected. For exact number of lane and data width choice, refer Table 1 on page 10.

Figure 6 • **LiteFast IP Receiver Configurator**



3.4.2.4 Counter Checker

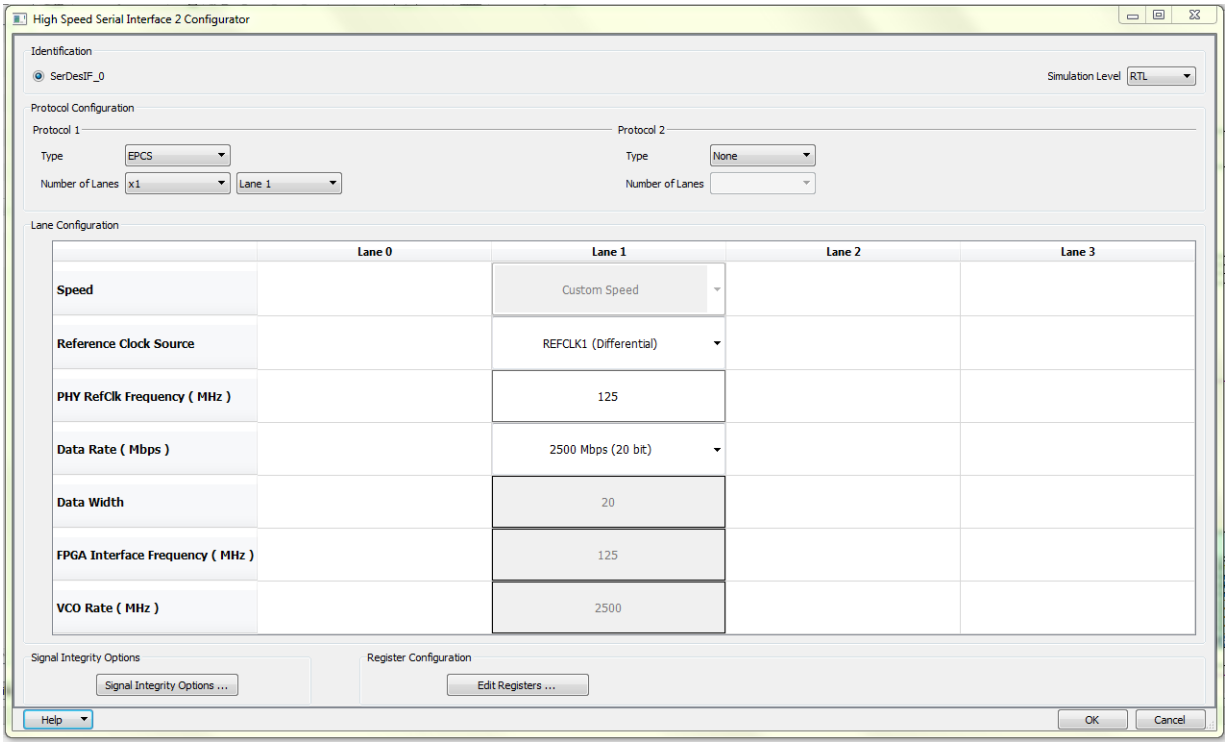
The counter checker block contains a 16-bit count generator and 16-bit checker that checks the incoming data with the self-generated data. Error counter is incremented whenever there is a mismatch between estimated data and captured data.

3.4.3 SERDES

SmartFusion2 SoC FPGA high-speed SERDES is a hard IP block on chip that supports rates up to 5 Gbps. The SERDES block offers embedded protocol support for PCIe, SRIO, XAUI, SGMII and so on. The SERDES block also supports EPCS interface which can be used for custom protocols. There are up to 16 channels of SERDES available in SmartFusion2 devices (refer to the *SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration*).

In this demo design, the SERDES_IF_2 block is configured for EPCS modes on Lanex (Lanex can be Lane1 or Lane2), with 20-bit parallel interface on both transmit and receive side, and external reference clock from on board Oscillator. The configurator window for SERDES in the smart design is shown in Figure 7.

Figure 7 • **SERDES Configurator window**



3.4.3.1 Reference Clock Source

For the given demo, when line speed is working at 2.5 Gbps, the reference Clock to SERDES is 125 MHz and it is given from differential pads (REFCLK1P and REFCLK1N). In SmartFusion2 Security Evaluation Kit, the REFCLK1 differential pads are driven from 125 MHz on board Oscillator.

3.4.4 UART

The UART block contains the CoreUART and FabUART modules. The FabUART module is the wrapper interface that sends/receives commands and data to the GUI through CoreUART block. Refer to *CoreUART v5.4 Handbook* for more information on the CoreUART block.

4 Validating the Design on SmartFusion2 Security Evaluation Kit

4.1 Requirements

The following are the hardware requirements to run the demo:

Table 2 • **Hardware Requirements**

Description	Quantity
SmartFusion2 Security Evaluation Kit	One
FlashPro4 Programmer	One
SMA M to SMA M loopback cables	Two (required if it is Lane 2 demo)
Mini to Micro USB cable	Two
STAPL/PDB file	Included with project
GUI Software	Included with project
Libero	11.7.1.11(11.7 SP1)

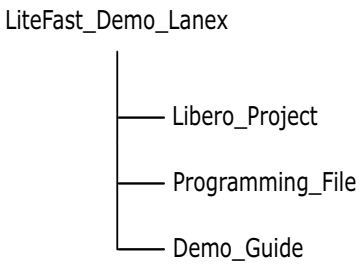
4.2 Design Files Directory Structure

The demo design files are available for download from the following path in the Microsemi website:

- For Lane1:
  http://soc.microsemi.com/download/rsc/?f=LiteFast_Demo_Lane1
- For Lane2:
  http://soc.microsemi.com/download/rsc/?f=LiteFast_Demo_Lane2

The following figure shows the top-level structure of the design files. Which are delivered along with this demo guide:

Figure 8 • **Design Structure**



Note: Lanex can be Lane1 or Lane2.

4.3 Setting the Board

The following steps describe how to set the board for demo:

1. SmartFusion2 090T device consists one SERDES with four lanes. Lane 1 and Lane 2 can be used for external loopback testing on the SmartFusion2 Security Evaluation Kit board. Lane 1 is a PCB trace loopback on board where as Lane 2 is external SMA loopback
2. A pair of SMA-SMA cables are required to loopback SERDES TXP_2 to RXP_2 and TXN_2 to RXN_2, as shown in Figure 10 on page 17. The FlashPro4 needs to be connected to the JTAG header on the board.

3. Connect the micro-USB to USB-A cable to the board, as shown in Figure 10. The USB-A connector needs to be connected to the computer. For more information on SmartFusion2 Security Evaluation Kit board refer to the *UG0541: SmartFusion2 SoC FPGA Evaluation Kit User Guide*.

Figure 9 • **SmartFusion2 SoC FPGA Evaluation Kit Board Overview**

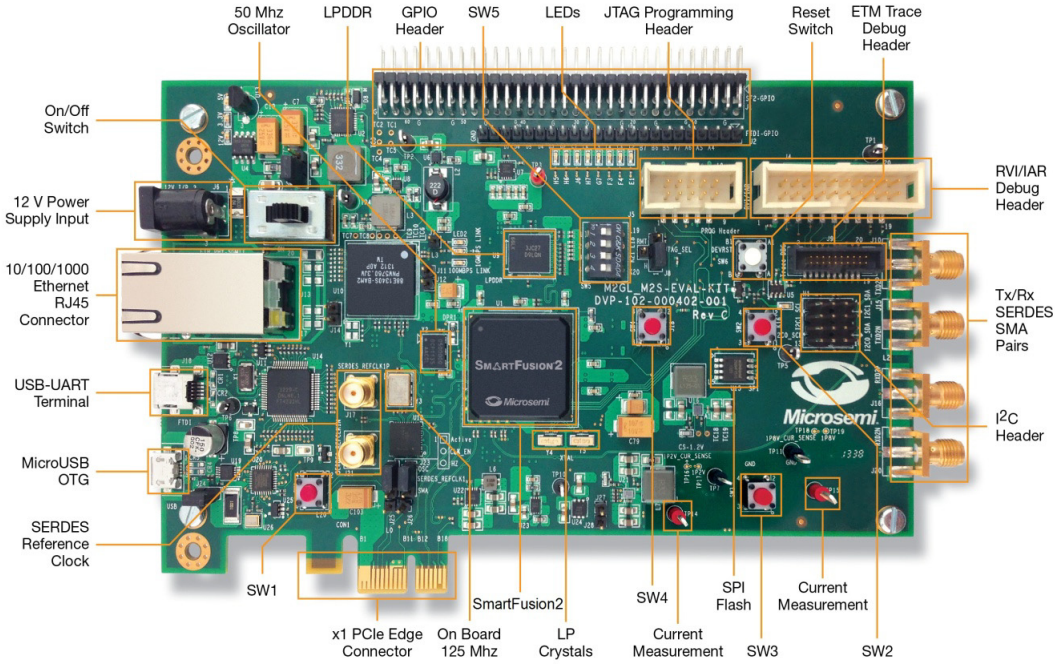
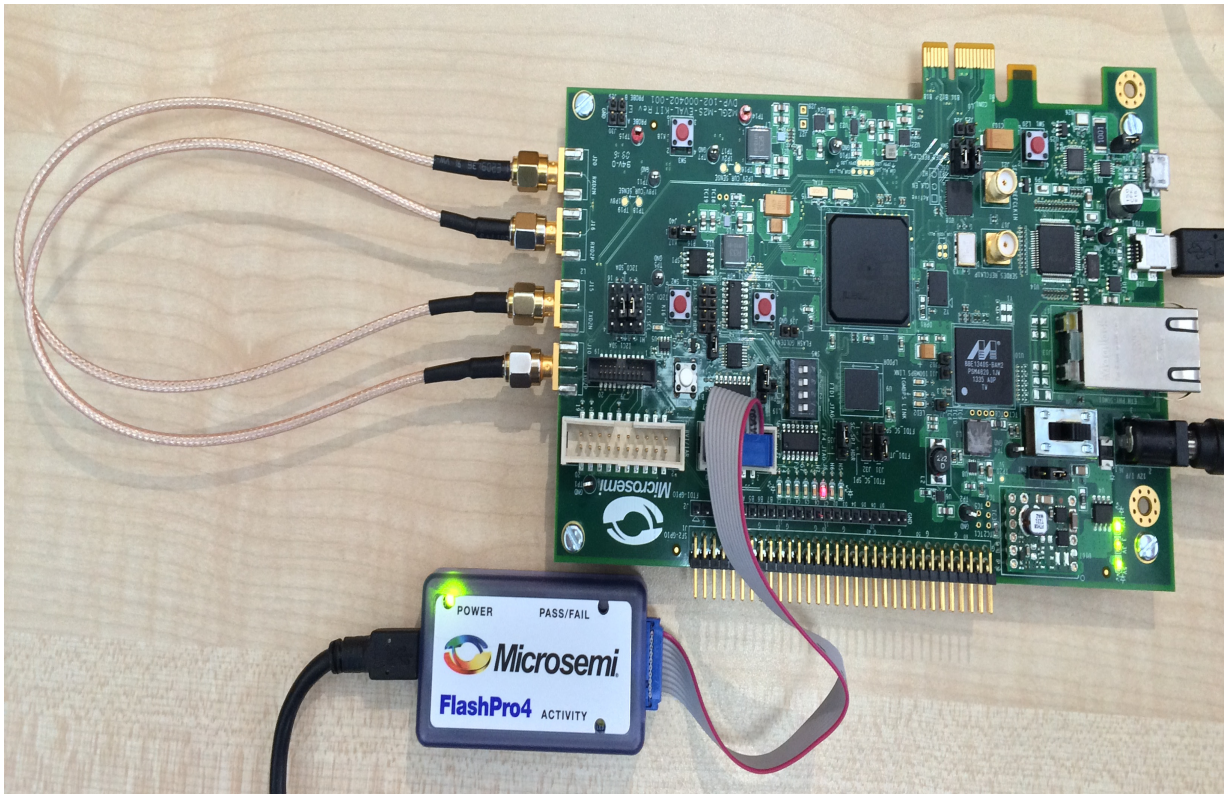


Figure 10 • **Board Setup**



4. Install USB-UART drivers. USB-UART driver files - FT232R are available on Microsemi website.

4.4 Programming the Device

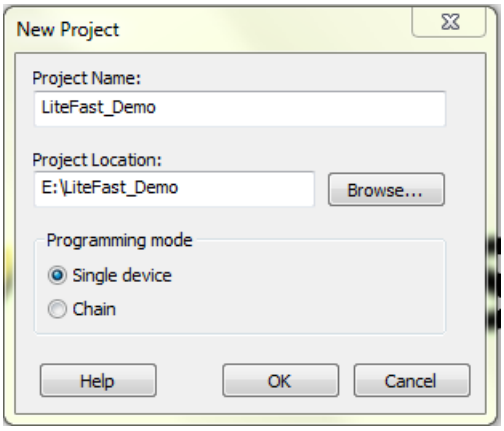
The following steps helps in programming the device:

1. Download the design files:
   - For Lane1:
     http://soc.microsemi.com/download/rsc/?f=LiteFast_Demo_Lane1
   - For Lane2:
     http://soc.microsemi.com/download/rsc/?f=LiteFast_Demo_Lane2

   Programming file (STAPL/PDB) is located in the Programming_Files folder.
2. Connect the Flashpro4 programmer to the SmartFusion2 Evaluation Kit board.
3. Open FlashPro v11.7 SP1 (installed as part of the Libero IDE).
4. Click **New Project** in FlashPro.

5. Enter the project name as **LiteFast_Demo** in the **New Project** window.

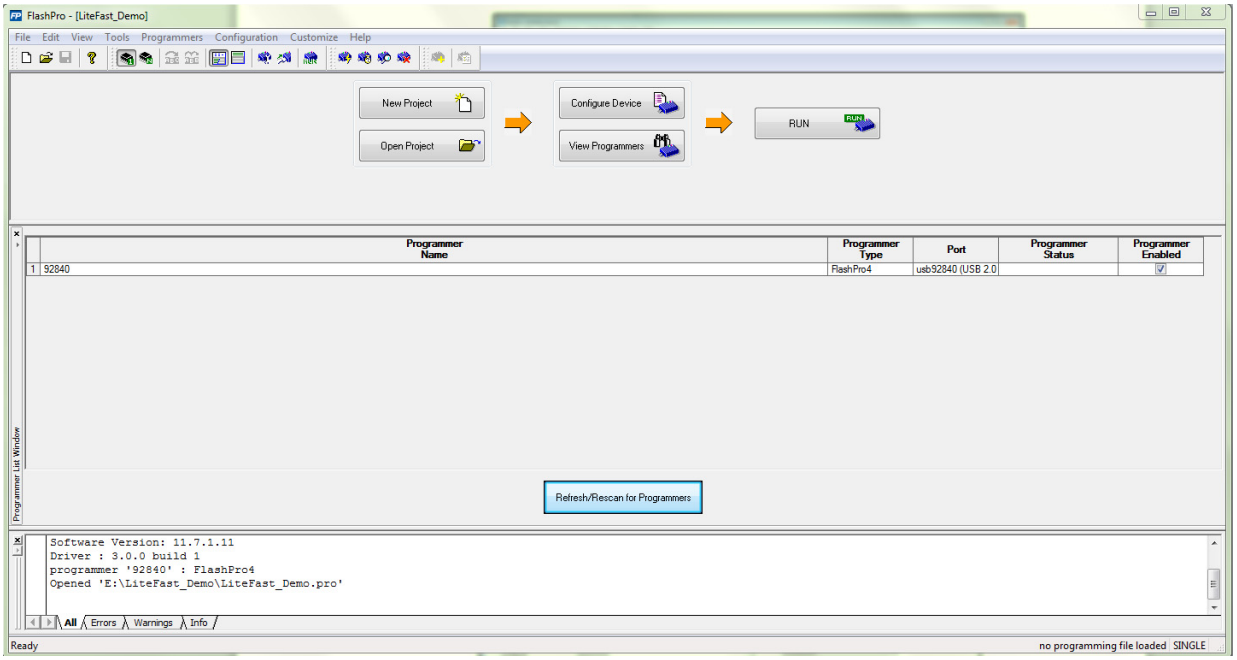
Figure 11 • **New Project Window**



If necessary, change the default location in the Project Location.

6. Select Single Device Programming mode.
7. Click **OK**. The FlashPro GUI window is displayed. The Programmer List Window updates with programmer information.

Figure 12 • **FlashPro GUI Window**

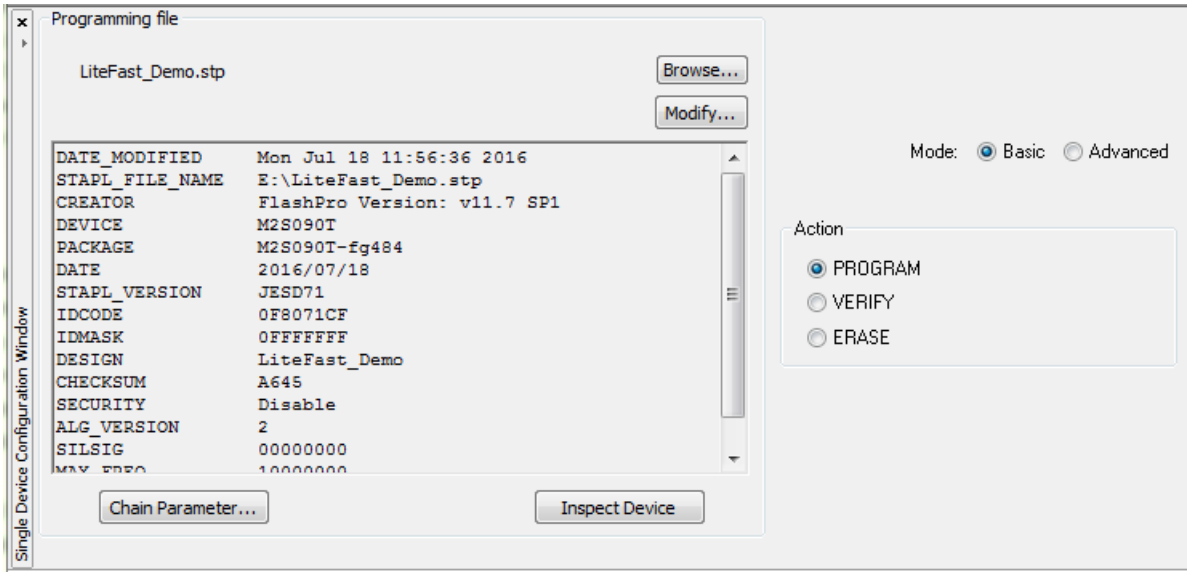


After the project is connected the program is ready to load the STAPL/PDB file downloaded.

8. Click **Configure Device**. The **Single Device Configuration** window is displayed in FlashPro.
9. Click Browse to find the programming file.
10. On the **Load Existing Programming File** window, select the required programming file and click **Open**.

11. The **Single Device Configuration** window updates the programming file information and the actions available with the programming file in the Action list box (see Figure 13).

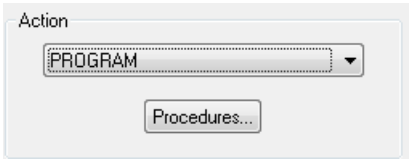
Figure 13 • **Single Device Configuration Window**



Note: Microsemi recommends using the default settings.

12. After loading the programming file, select **Program**.Click **Procedures...** (see Figure 14).

Figure 14 • **Action List Window**

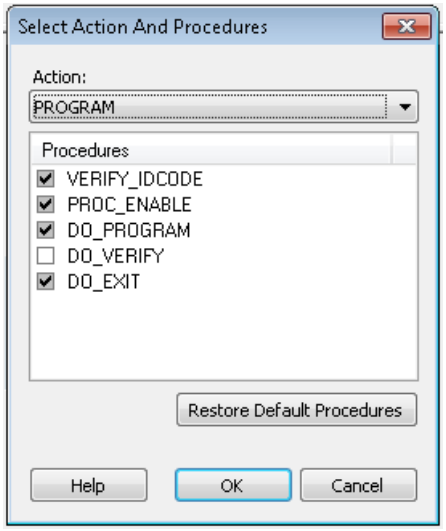


Select Action and Procedures window is displayed, showing the procedures for the programming action (see Figure 15).

Note: Microsemi recommends using the default settings.

13. Click **Restore Default Procedures**.

Figure 15 • **Select Action and Procedures**



14. Click **Program** to program the device.

The programmer list window updates the programmer status column with run passed indicating that the device is successfully programmed.

Note: The status indicator is updated during programming to show the programming progress, then it changes to a pass or fail result when the operation is completed.

15. View the Log window for the details about of the programmed device.
16. Power Cycle the board.

4.5 Executing the Demo Design

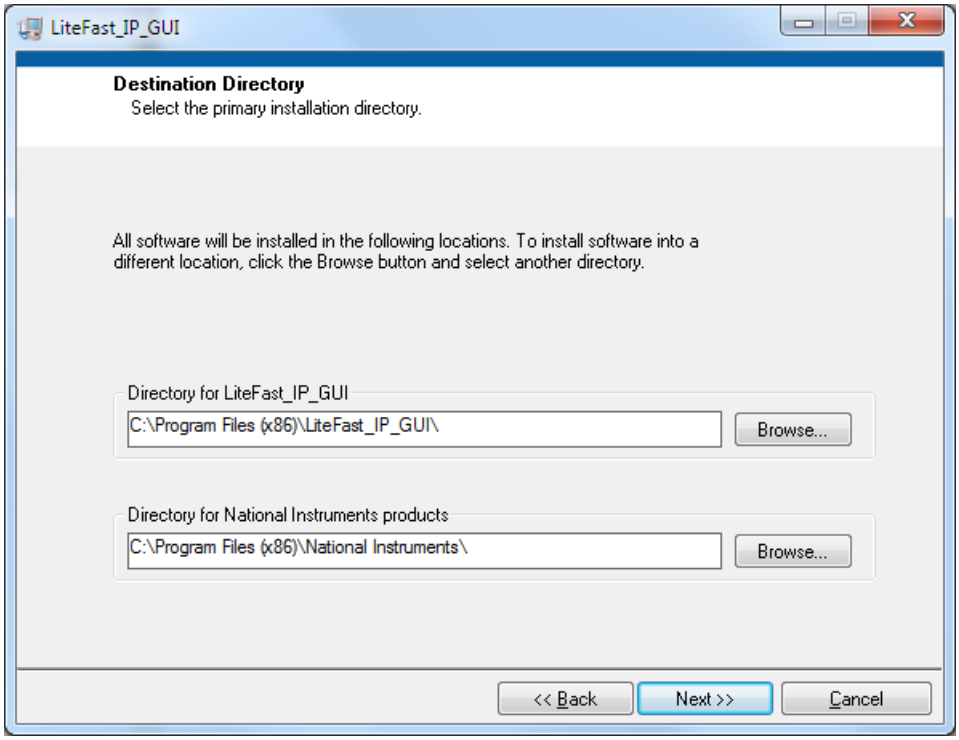
4.5.1 LiteFast Demo GUI Installation

Perform the following steps to install the LiteFast IP Demo GUI:

1. Download the GUI installation files:
   http://soc.microsemi.com/download/rsc/?f=LiteFast_GUI
2. Open **GUI_Installer>Volume>setup.exe**.
3. When prompted, click **Yes**.

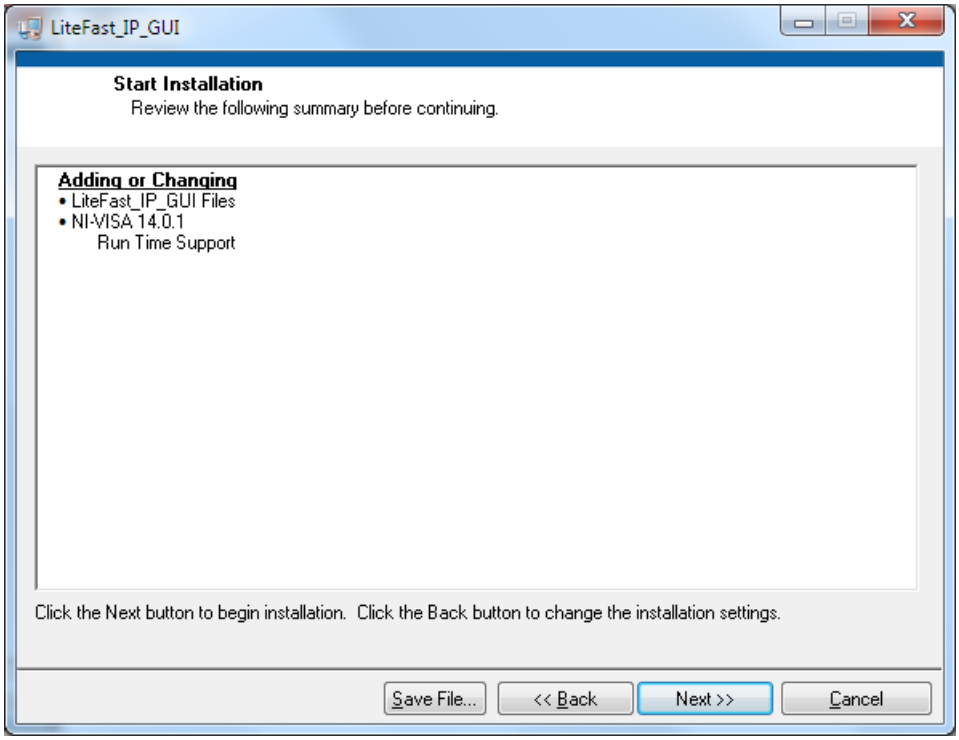
4. On the LiteFast Destination Directory window click **Next**, as shown in Figure 16. Default locations are displayed.

Figure 16 • **LiteFast GUI Setup Window**



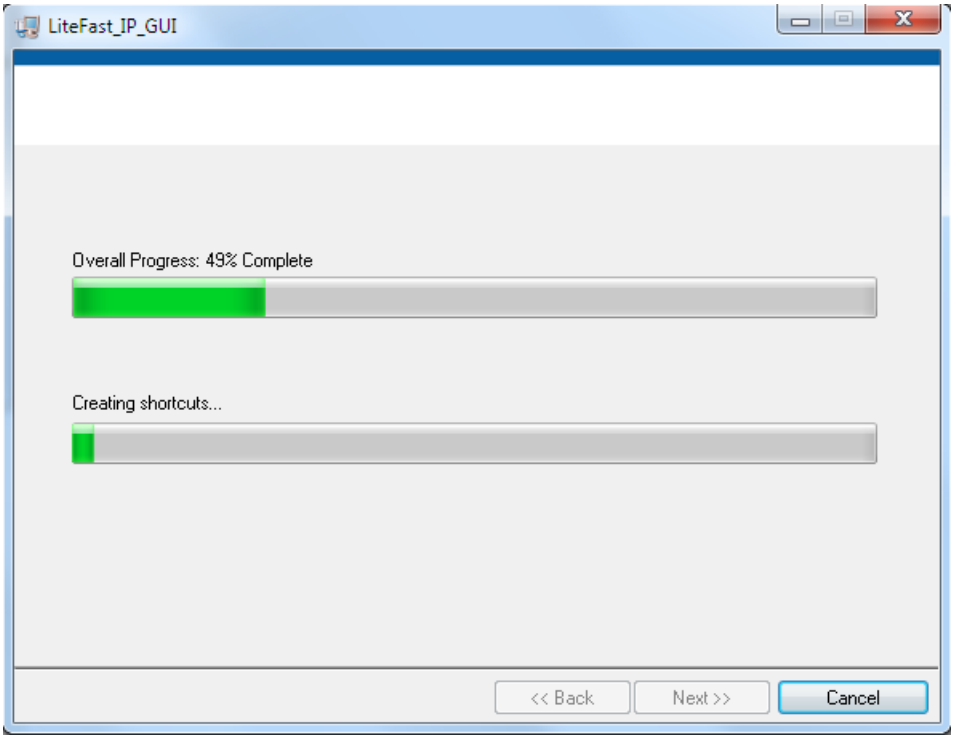
5. On the LiteFast Start Installation window click **Next**, as shown in Figure 17.

Figure 17 • **LiteFast GUI Installation**



A progress bar appears which shows the progress of installation, as shown in Figure 18. Wait for the installation to complete It may take few minutes.

Figure 18 • **LiteFast GUI Setup Progress Bar**



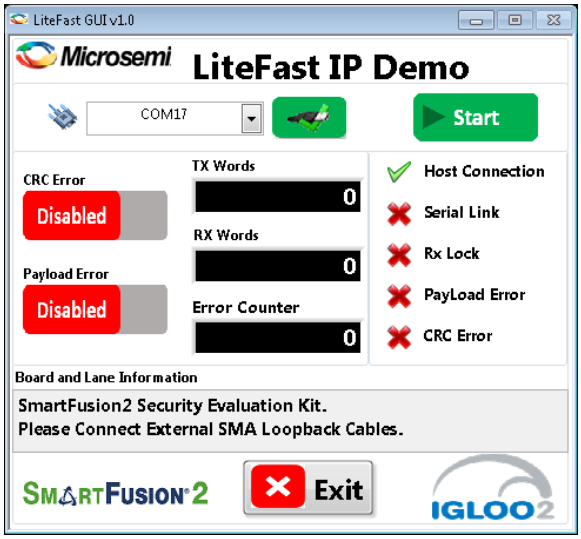
6. If the installation is successful, Installation Complete message appears. Click **Finish**. Restart computer before using the installed GUI.

Note: The GUI given along with this demo design is applicable only for this demo design.

4.5.2 LiteFast Demo GUI Description and Usage

1. Open **Programs>LiteFast_IP_Demo**.
2. The LiteFast GUI window appears, as shown in Figure 19.

Figure 19 • **LiteFast GUI Window**



LiteFast GUI interface description is as follows:

- The drop down menu for ports gives the list of serial ports available on the host PC.
    - The list of serial ports differs for host PC so check the correct port that works.

Note: Default settings for the design are 9600 Baud, No flow control, 1 stop, and no parity.

- After opening the GUI, it auto detects the COM port connected to the device and establishes the communication with board. If there is any issue when connecting the host PC with board, connection can be done manually by selecting the appropriate COM port from drop down list and click connect.
- Status signals indicate the complete system operation.
    - If Host Connection is crossed-red, it means that the GUI failed to open a COM port. It turns green when the GUI software is able to open the selected COM port on the host PC.
    - Serial Link is an indicator of the transmission link for the serial LiteFast data. If the link is up and running, Serial Link turns green. It turns crossed-red if the link goes down.
    - Rx Lock is receiver lock. Rx Lock goes green, when the receiver starts receiving valid and error free data. It means that the receiver has locked to the count sequences and the subsequent transmitted sequences can be successfully received.
    - Payload Error indicates any errors received. When Payload Error goes red, the receiver finds a corrupted packet or detects any error in the received counter sequences.
    - CRC Error indicates any CRC Errors. When CRC Error goes red, the CRC checker in receiver finds a corrupted packet or detects any loss of sequence in the received counter sequences.
- RX Words: Shows the number of received data words. This number rolls over after 65535 words.
- TX Words: Shows the number of transmitted data words. This number rolls over after 65535 words.
- Error Counter: It indicates the packet loss and rolls over after 65535 words.

Note: Error counter may not exactly co-relate to TX words and RX words due to the rollover.

- Payload Error Slider: It is used to introduce errors in the transmission for debug purposes. By enabling this slider it injects the error in the transmitted count sequence which as a result, increments the Error Count display and Payload Error turns Red
- CRC Error Slider: It is used to introduce CRC errors in the transmission for debug purposes. By enabling this slider it injects the CRC error in the transmitted count sequence which as a result, CRC Error indicator turns Red
- Clicking Start: Starts the LiteFast demo. The Counter starts transmitting count data which is sent over serial transmit link. It is then received by the receiver and checked for any errors. The status at any time can be monitored using the status signals in the GUI.
- Clicking Stop: Stops the LiteFast Demo.
- Click Exit: Exits the GUI.

Figure 20 shows how the GUI looks like during an error free operation of the LiteFast demo system.

Figure 20 • **Connected LiteFast GUI**

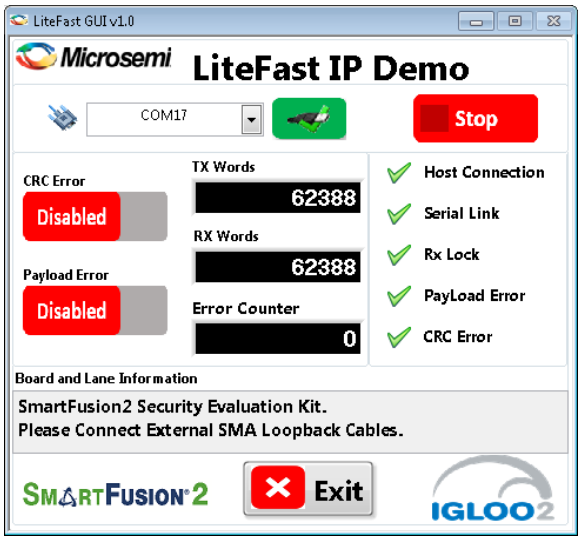


Figure 21 shows how the GUI looks like during payload error injection of the LiteFast demo system.

Figure 21 • **GUI with Payload Error Injection**

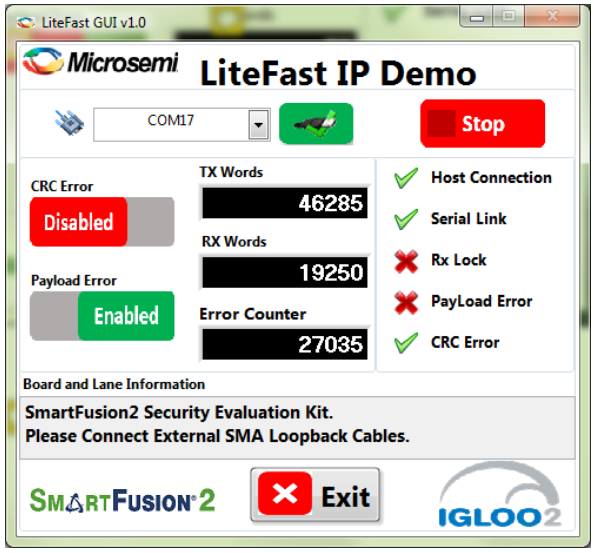
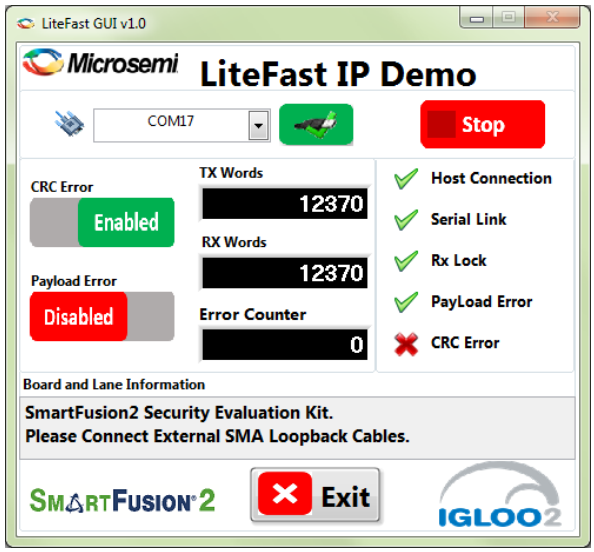


Figure 22 shows how the GUI looks like during CRC error injection of the LiteFast demo system.

Figure 22 • **GUI with CRC Error Injection**



5 Using LiteFast in Customer Application

The demo design consists of LiteFast IP, traffic generator, checker, and other modules. This system is specific to the demo. In case, user likes to use the LiteFast IP in the design, some modifications are needed to be done.

Replace the counter and checker modules with customer design.

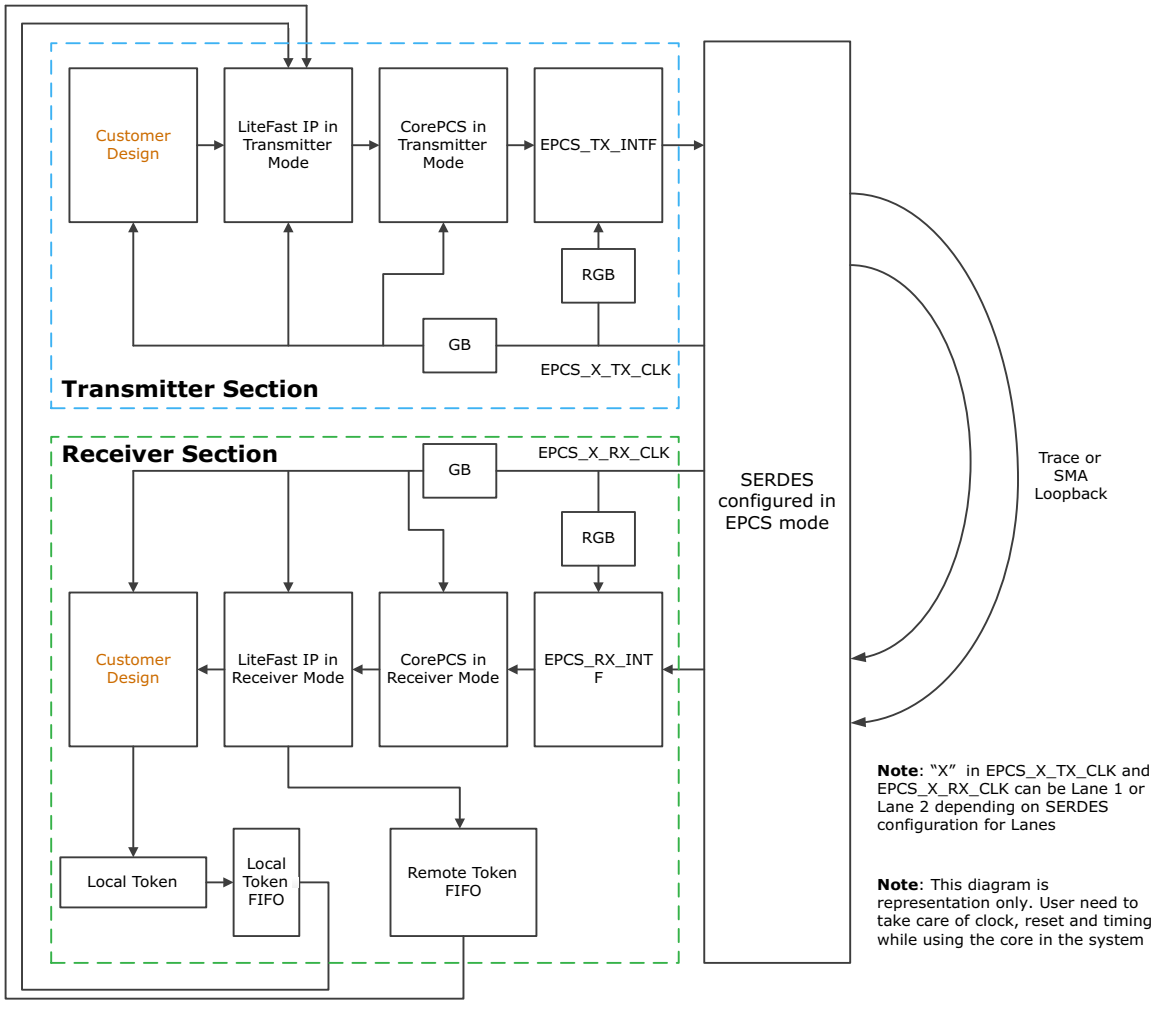
5.1 LiteFast Transmitter Section

The count generator in the transmitter section can be replaced with the user data generator module. The data generator is interfaced with the LiteFast transmit module, as shown in the Figure 23.

5.2 LiteFast Receiver Section

The count checker in the receiver section can be replaced with the data receiver in the user design. The data receiver takes input from the LiteFast receiver module, as shown in the Figure 23.

Figure 23 • **Custom LiteFast Demo Diagram**



5.3 Guidelines for Libero Design Flow

Following are the guidelines for Libero design flow:

1. Create the design using smart design in the Libero v11.7 SP1.
2. Add the LiteFast IP from the IP catalogue.
3. Configure the transmitter and receiver sections, as per system requirements.
4. Go through the synthesis and check for any warnings.
5. Adjust the DELAY value of the delay line module in EPCS RX module to avoid any hold violations.
6. Give proper LiteFast TX and RX clock constraints.
7. Proper care for clock crossing needs to be taken for local and remote token handling.
8. Complete the implementation and generate the bit stream.
9. Program the device.
10. Execute the design and check the functionality.

5.4 System Resource Utilization for Demo Design

Table 3 • **System Resource Utilization for Demo Design**

Resource Type	Used	Available	Percentage Utilization
4LUT	2111	86184	2.45
DFF	1710	86184	1.98
I/O Register	0	795	0.00
User I/O	5	265	1.89
-- Single-ended I/O	3	265	1.13
-- Differential I/O Pairs	1	132	0.76
RAM64x18	2	112	1.79
RAM1K18	0	109	0.00
MACC	0	84	0.00
Chip Globals	15	16	93.75
Row Global	2	1408	0.14
CCC	1	6	16.67
RCOSC_25_50MHZ	1	1	100.00
RCOSC_1MHZ	0	1	0.00
XTLOSC	0	1	0.00
SERDESIF Blocks	1	1	100.00
-- SERDESIF Lanes	1	4	25.00
MSS	1	1	100.00

6 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

6.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

6.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

6.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

6.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

6.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

6.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

6.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

6.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

6.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.