

LX7730 Datasheet List of Changes

Rev0.98 - Rev0.97

1. Page 9, EC Table.

Is:

IVCC	VCC Normal Current		38	70	85	mA
IVEE	VEE Current	Using external VEE source. Positive current out of pin.	-2	-4.7	-7.0	mA

Was:

IVCC	VCC Normal Current		55	70	85	mA
IVEE	VEE Current	Using external VEE source. Positive current out of pin.	-3.5	-4.7	-6.0	mA

2. Page 9, EC Table.

Is:

V _{VEE}	VEE UVLO	Voltage falling; 200mV Hysteresis	-8.2	-8.0	-7.5	V
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Was:

V _{VEE}	VEE UVLO	Voltage falling; 200mV Hysteresis	-8.2	-8.0	-7.8	V
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3. Page 9, EC Table

Is:

V _{VEE}	VEE voltage	VCC - VEE	1.5	2.6	3	V
V _{+5V_NOM}	+5V voltage		4.75	5.00	5.25	V

Was:

V _{VEE}	VEE voltage	VCC - VEE	2.0	2.6	2.9	V
V _{+5V_NOM}	+5V voltage		4.8	5.00	5.20	V

4. Page 9, EC Table

Is:

V _{CH#}	Voltage Clamp (power applied)	Clamp Current = 1mA (into pin) ⁽¹⁾	VCC	16	17	V
		Clamp Current = 1mA (out of pin)	-23	-20	-16	
V _{CH#}	Voltage Clamp (VCC=VEE=0)	Clamp Current = 1mA (into pin)	16	20	23	V
		Clamp Current = 1mA (out of pin)	-23	-20	-16	

Was:

V _{CH#}	Voltage Clamp (power applied)	Clamp Current = 1mA (into pin) ⁽¹⁾	15	16	17	V
		Clamp Current = 1mA (out of pin)	-23	-20	-17	
V _{CH#}	Voltage Clamp (VCC=VEE=0)	Clamp Current = 1mA (into pin)	17	20	23	V
		Clamp Current = 1mA (out of pin)	-23	-20	-17	

5. Delete EC spec :

I _{CH#}	Settling Time	To within 5% tolerance			10	μs
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6. Page 1 & 8, the LX7730 offers 1 kV ESD pin protection on FPGA interface pins and power pins, 500V ESD protection to all CH#, BLI# and the other pins.

It was “1 kV ESD pin protection on all CH# pins and 2kV on the other pins.”

7. Page 1, 3% Precision Adjustable Current Source. Update it to match the EC table spec, it is not a spec change.

It was “2% Precision Adjustable Current Source”

8. Page 4 & 9, add 0.1% resistor tolerance to ADC_BIAS_IN and ADC_DAC_OUT pins description, add 1% resistor tolerance to IREF1 pin description.

9. Page 5, add “Connect it to ground when not used.” to BL-TH pin description.

10. Page 17, delete “but will not change during the process of a data read which starts by reading the upper byte and ends by reading the lower byte” from 12 bit ADC theory of operation description.



Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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