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Microsemi FPGA TechBytes

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New Imaging and Video Solution

Microsemi now has recently announced a new imaging/video solution available for the development of low-power, reliable video processing applications. The solution is ideal for a variety of applications including drones, machine vision, robotics, infrared cameras, head-up display, target acquisition systems, medical imaging, surveillance, and automotive imaging.

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Unique Debug Capabilities Reduce FPGA Debug Time

Microsemi and Synopsys provide logic analyzer and built-in oscilloscope visibility software tools for the fastest FPGA debug. IGLOO2, SmartFusion2, and RTG4 are the only devices with unique Active Probe and Live Probe capabilities.

Learn More Watch Webinar Now

New Motor Control Reference Designs Available

Our deterministic multi-axis motor control solution now supports applications using encoder, Hall sensor, CAN bus, and induction motors. New design examples and IP are available online.

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Highest Junction Temperature Automotive FPGAs

IGLOO2 FPGAs offer the highest junction temperature (Tj=135 °C) in the industry. IGLOO2 FPGAs support AECQ-100 grade 1 temperature ranges, and both IGLOO2 and SmartFusion2 support grade 2.

Learn More

Prevent Overbuilding and Cloning for FPGA Designs

Microsemi's Secure Production Programming Solution (SPPS) automatically prevents overbuilding using hardware security modules (HSM), custom firmware, and the state-of-the-art security protocols built into every SmartFusion2 SoC FPGA and IGLOO2 FPGA.

Learn More Watch Video

Powerful, Easy-to-Use Constraints Manager

Libero SoC v11.7 introduced the Enhanced Constraint Flow to simplify the management of constraints, and provides a single entry point for editing and applying all user constraints for I/O, timing, floor planning, and synthesis.

View Short Constraints Overview

In The News

Microsemi and Arrow Electronics Team Up for Growth in Key Verticals

Microsemi Collaborates With Solectrix to Introduce SmartFusion2 SoC FPGA-Based System-on-Module for Low Power and Secure Digital Signal Processing

Recent Articles

FPGAs and audio processors enable unique industrial applications – Ted Marena

Preventing Overbuilding & Cloning in the Global Electronics Supply Chain – Tim Morin

Smart FPGA Debugging Tools Reduce Validation Times – Ted Marena

The Biggest Security Threats Facing Embedded Designers – Richard Newell

FPGA-Based Design for Low System Power Consumption – Prem Arora

Center of Excellence

Signal Integrity / Power Integrity Expert – Deepali Gupta

Q) How did you become extremely knowledgeable on SIPI (Signal Integrity / Power Integrity)?
A) I started in 1999 working as a Product Engineer at Quicklogic. We were bringing up the first OC12 Serdes Transceivers for an internal test chip which was running at a very high speed of 622Mbps. It was during this bring-up where I got introduced to the intricacies of SIPI and how it can influence the SerDes Eye characteristics. Spent months of debug with designers to bring down the jitter, build a clean power delivery network (PDN) for the system. This basically involved learning from the works of Howard Johnson and Lee Ritchey. Grew a lot of interest and appreciation for this domain and started using these methodologies into hardware design. This domain is extremely complex and we still have ways to go to reach the full expertise.

Q) What is the most common mistake you see in designs and what is the best practice that you recommend?
A) There is a higher level of awareness now on designing High Speed systems for SerDes but still see that PDN is not given due diligence at times. In my experience debugging issues caused due to a compromised PDN is extremely time consuming and almost always results in a new revision of the hardware which is an expensive ordeal. Once the PDN gets comprised the system loses credibility. As the core voltages go lower designers need to take care of designing a robust PDN across the full system.

Q) How can SIPI play a role with customers who are designing for high speed Serdes applications?
A) In next generation devices with higher performance Serdes transceivers it is critical to have a robust SI ecosystem surrounding the designing of the Serdes links at a full system level by customers. This includes providing customers a robust simulation environment with high quality IBIS-AMI models/Package S-Parameter models. The simulation environment needs to be correlated at a system level with actual silicon/Boards. This should also include providing easy to use SIPI configurator tools which align to the simulation flow so customers can configure the actual silicon seamlessly. Having a reliable and correlated system provides confidence to customers.

Q) Tell us something about yourself that we would be surprised to know
A) I have had the unique opportunity to travel the globe at a very young age. I did most of my elementary/middle schooling between Liverpool, UK and State College, Pennsylvania including a few month stint in a small town in Nigeria. I was the only Indian math geek in the entire school so life was interesting to say the least. This opportunity definitely allowed me to absorb and appreciate the pros and cons of different cultures. But no matter how much I travel I always gravitate back to my home and family in India so that's my current haunt for now.

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