Timberwolf Digital Signal Processor family, powered by *AcuEdge*™ Technology

Designed for USB Audio Accessories

ZL38090

Product Brief

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Description

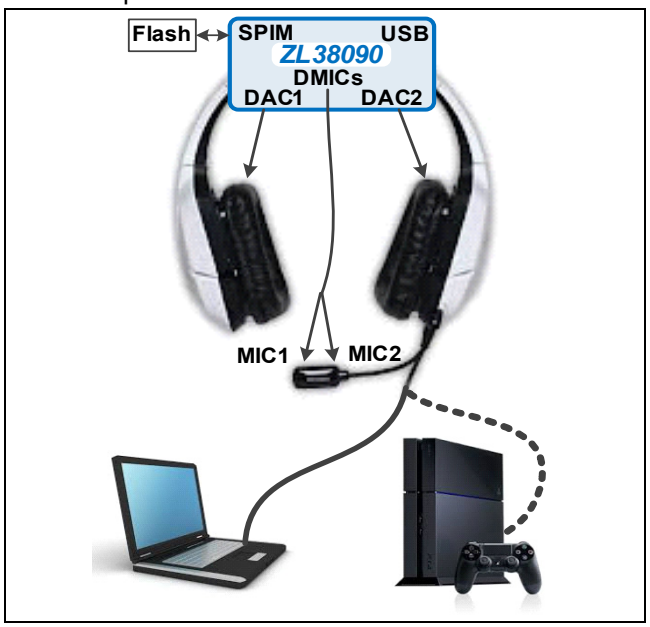
The ZL38090 is part of Microsemi's Timberwolf audio processor family of products that feature the company's innovative *AcuEdge* acoustic technology, which is a set of highly-complex and integrated algorithms. These algorithms are incorporated into a powerful DSP platform that allow the user to extract intelligible information from the audio environment.

The Microsemi *AcuEdge* Technology ZL38090 device is ideal for Universal Serial Bus (USB) Audio Accessories. The device is available in a 64 pin QFN or 56 ball WLCSP package. Its license-free, royalty-free intelligent audio Firmware (ZLS38090) provides Beamforming and a variety of other voice enhancements to improve both the intelligibility and subjective quality of audio.

Microsemi offers the *MiTuner*™ ZLS38508LITE GUI software package allowing a user to interactively configure the ZL38090 device.

Applications

- Unified Communication Devices
- USB Boom and Boomless Headsets
- USB Beamforming Microphones
- USB Speakerphone
- USB Speakers



Typical USB Headset Application

Ordering Information

Device OPN	Package	Packing
ZL38090LDF1	64-pin QFN (9x9)	Tape & Reel
ZL38090LDG1	64-pin QFN (9x9)	Tray
ZL38090UGB2	56-ball WLCSP(3.05x3.05)	Tape & Reel

These packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Microsemi *AcuEdge* Technology ZLS38090 Firmware Audio Features

- Supports 1 stereo headset pair with play and record or just playback functions
- Microphone Beamforming (2 microphones)
- Standard Dynamic Range Compressor
- Limiter
- Expander
- Send and receive path 8-band parametric equalizers
- 8 kHz/16 kHz/48 kHz audio streaming
- 14 General Purpose Input/Outputs (11 in the WLCSP package) with fixed function capability for:
  - Volume Up/Down, Mute Mic, and Hook-Switch On/Off
  - PWM outputs for LED control

Common USB Features

- USB Audio Class Device v1.0 compliant
- Adaptive mode for playback, Asynchronous mode for record
  - USB Audio Class clock modes
- Remote wake-up via fixed function GPIO
- Common HID controls for volume, mute, equalizer, and audio source and destinations
- A USB port enumerates with:
  - EP0 (Control)
  - 2 endpoints for Microphones and Speakers (both stereo)
  - 1 interrupt endpoint (for Status Reporting)
- Skype/Lync Compatible

- Stand alone USB device (additional host processor not required for headphone applications)

ZL38090 Common Hardware Features

- DSP with Voice Hardware Accelerators
- Dual ΔΣ 16-bit digital-to-analog converters (DAC)
  - Sampling up to 48 kHz and internal output drivers
  - Headphone amplifiers capable of 32 mW output drive power into 16 ohms
  - Impulse pop/click protection
- 2 Digital Microphone inputs
- TDM port shared between PCM and Inter-IC Sound (I^2S)
- General purpose UART port for debug
- Boots from SPI or Flash
  - Master SPI port for serial Flash interface
  - Can run unattended (controllerless), self-booting into a configured operational state

For ease of mounting, the ZL38090 is available in two packages.

QFN Hardware Features

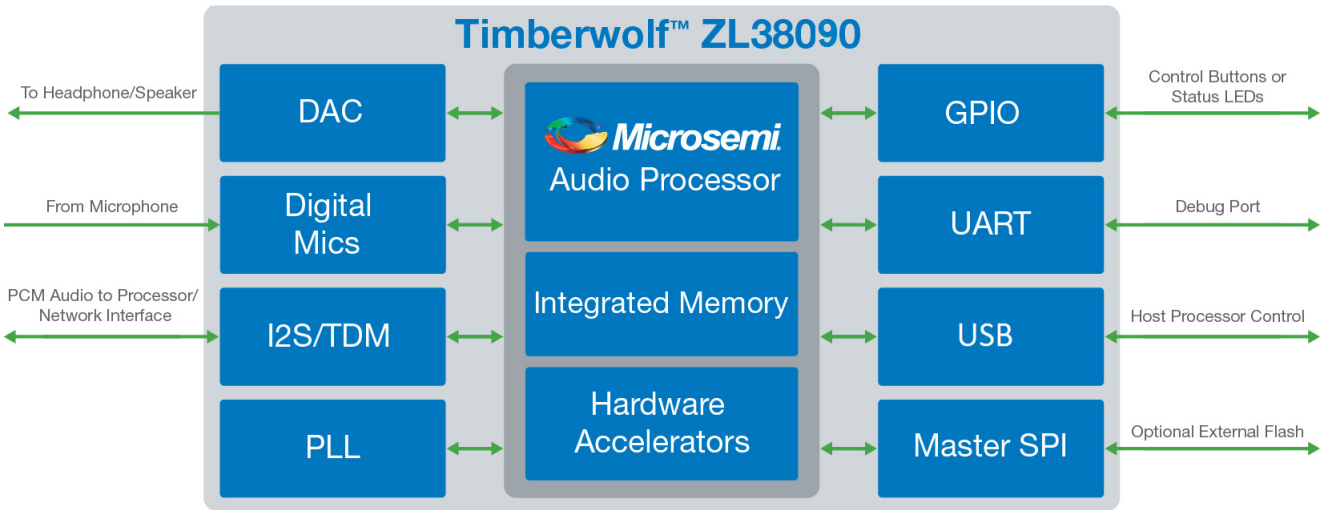
- 64-pin QFN
  - 9 mm by 9 mm package size
- Headphone amplifiers can be configured as 2 differential or 4 single-ended outputs
- 4 Fixed Function PWM pins for Vol Up, Vol Down, Mute, and Hook Switch control and status
- 14 General Purpose Input/Output (GPIO) pins
- Internal +1.2 V voltage regulator

WLCSP Hardware Features

- 56-ball Wafer Level Chip Scale Package
  - 3.05 mm by 3.05 mm package size
- Headphone amplifiers can be configured as 2 single-ended outputs
- 4 Fixed Function PWM pins for Vol Up, Vol Down, Mute, and Hook Switch control and status
- 11 General Purpose Input/Output (GPIO) pins

Tools

- ZLK38000 Evaluation Kit
- *MiTuner*™ ZLS38508LITE GUI software



ZL38090 Audio Processor for USB Headsets

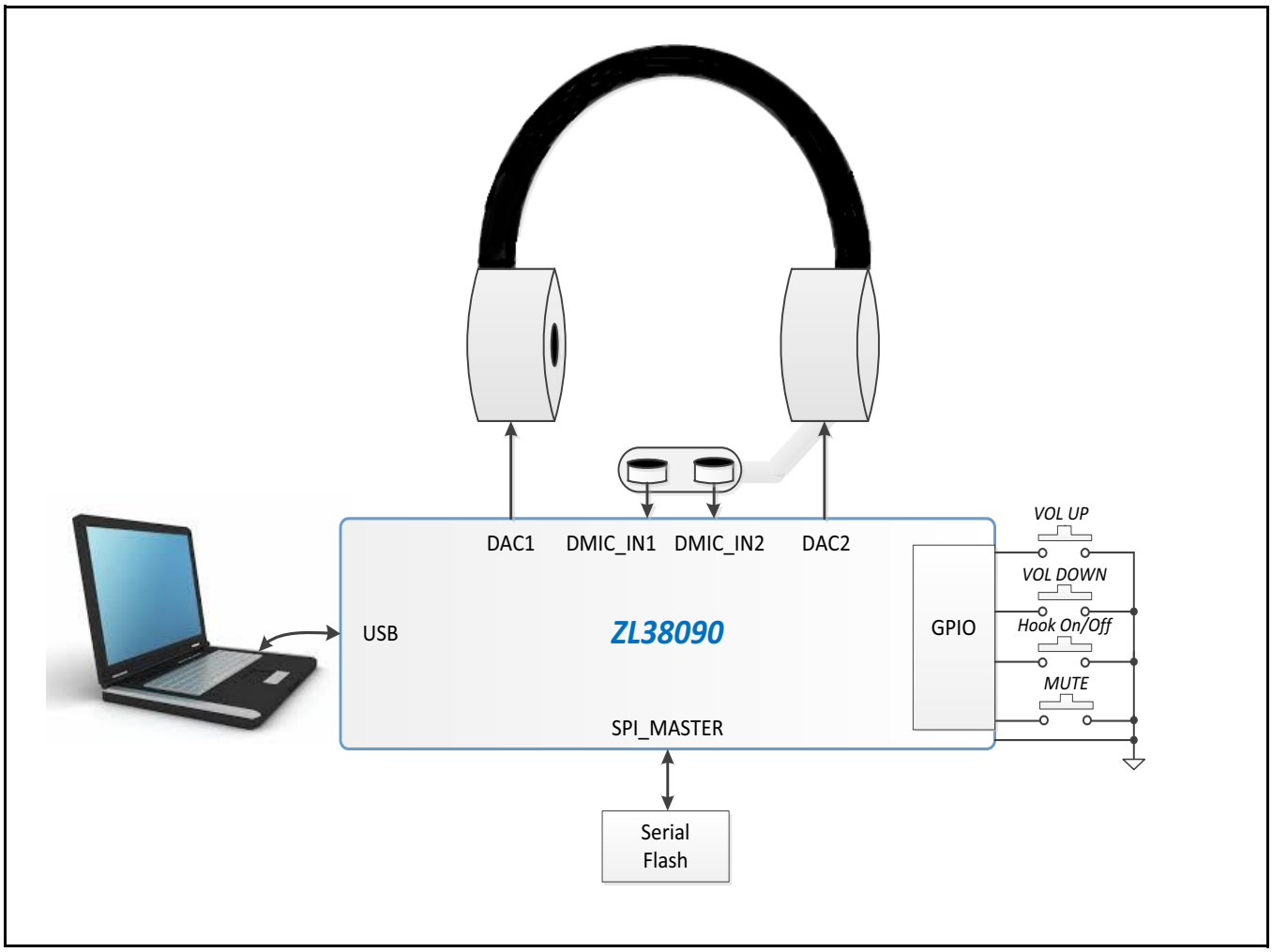
Typical Headset Application

The ZL38090 functions as a complete USB Audio device. The ZL38090 does not require a separate host processor to operate. It it is designed to meet the Skype Certification/Lync Logo specification for a headset. The USB port can be connected to any computer or gaming system. All device controls can be accessed through the USB port, including a subset of basic functions (preset modes) that can be wired to the GPIO pins to provide volume up/down, mute, or special programmable commands.

The ZL38090 has two internal differential headphone speaker amplifiers that can drive stereo signals directly into 16/32 ohm headphones.

Digital microphones can be connected to the ZL38090 DMIC interface, providing a low noise audio pick-up. The ZL38090 can perform beamforming when two microphones are used. Analog microphones can be used with the addition of an electret microphone pre-amplifier device.

The ZL38090 has a TDM port that can be used to route audio, or audio can be routed through the USB port.



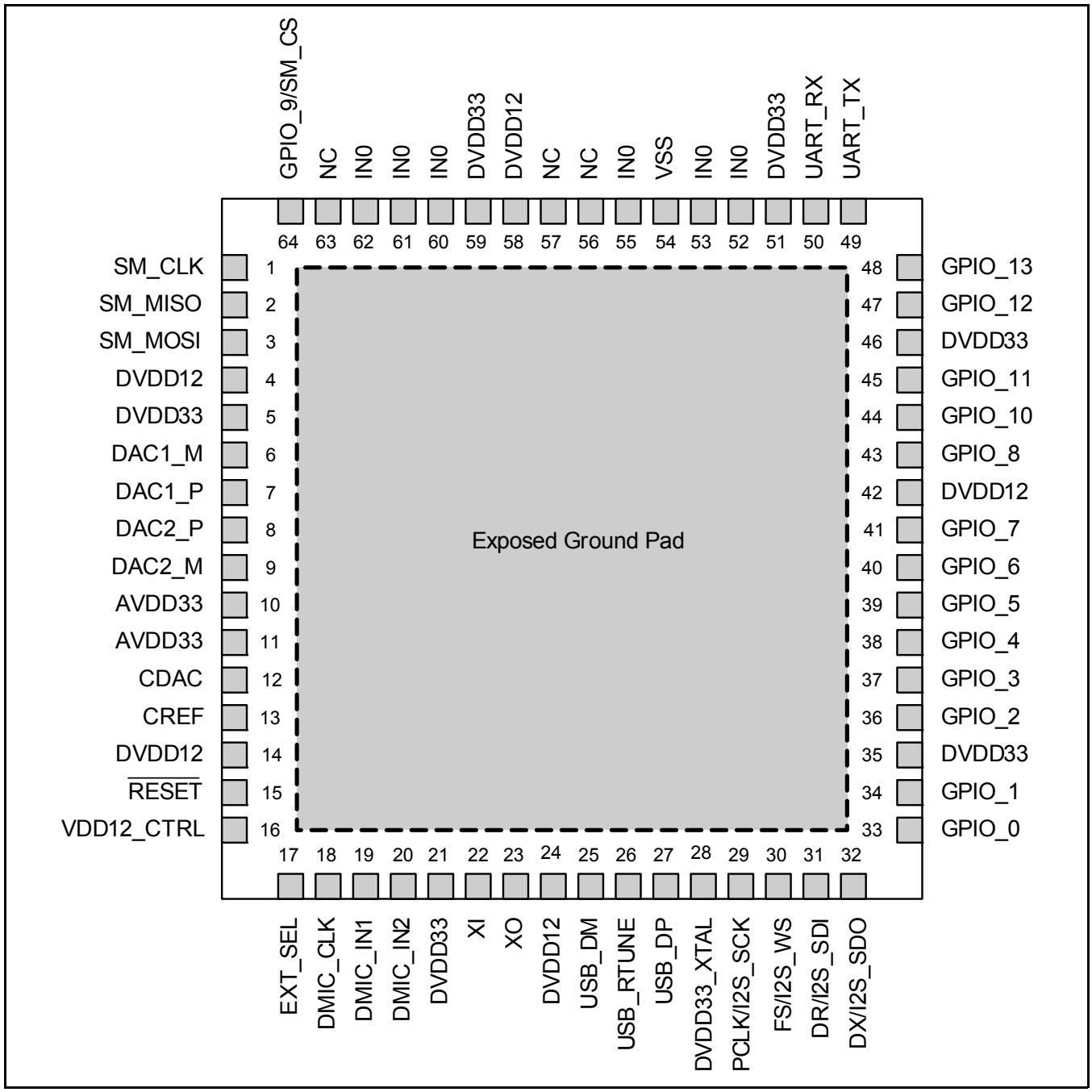
USB Headset Block Diagram

Note: When using the WLCSP package option, the headphone speaker amplifiers (DAC1 and DAC2) have single-ended stereo drive.

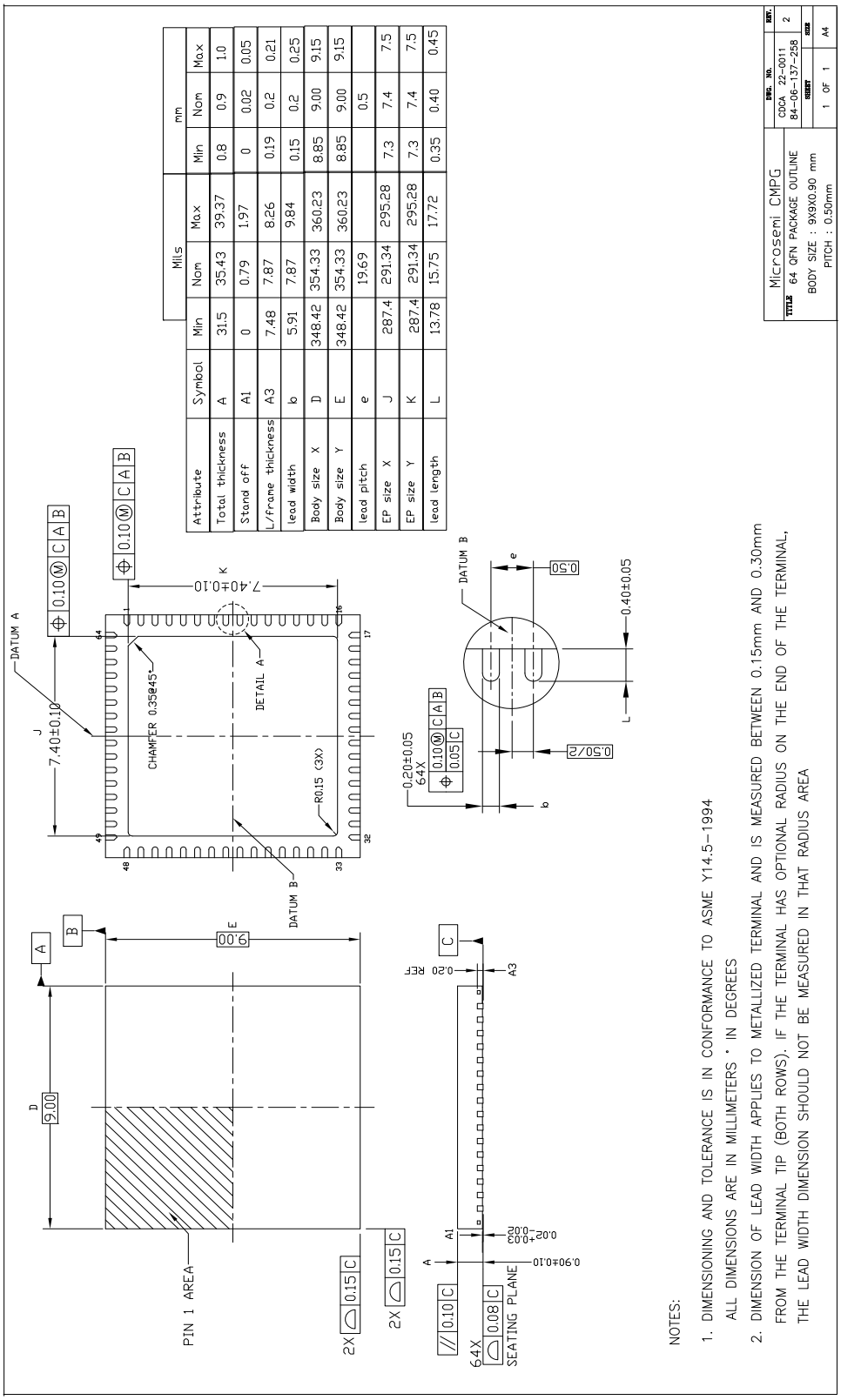
ZLK38090 Evaluation Kit

The ZLK38090 Evaluation Kit includes all the hardware necessary to operate the ZLE38090 Evaluation Board. The Evaluation Board provides a flexible platform to evaluate a ZL38090 Timberwolf Audio Processor device with *AcuEdge*™ Technology Firmware. Firmware Code for the ZL38090 can be downloaded into the Evaluation Board using the ZLS38000 Firmware Loader software. The ZLE38090 Evaluation Board can then be controlled using the *MiTuner*™ GUI Lite Software (ZLS38508LITE).

Device Pinout (64-Pin QFN) – Top View

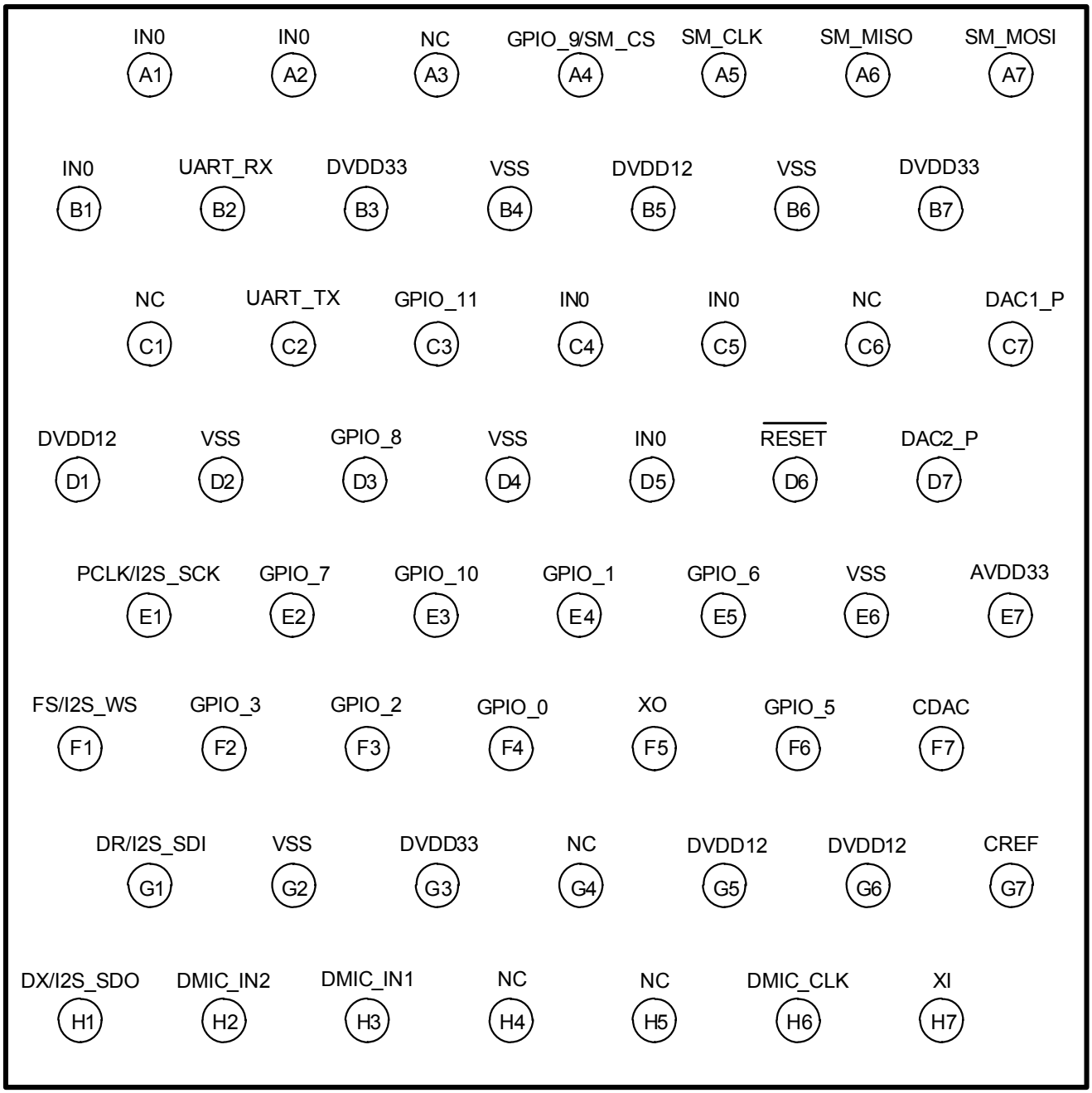


Package Outline (64-Pin QFN)

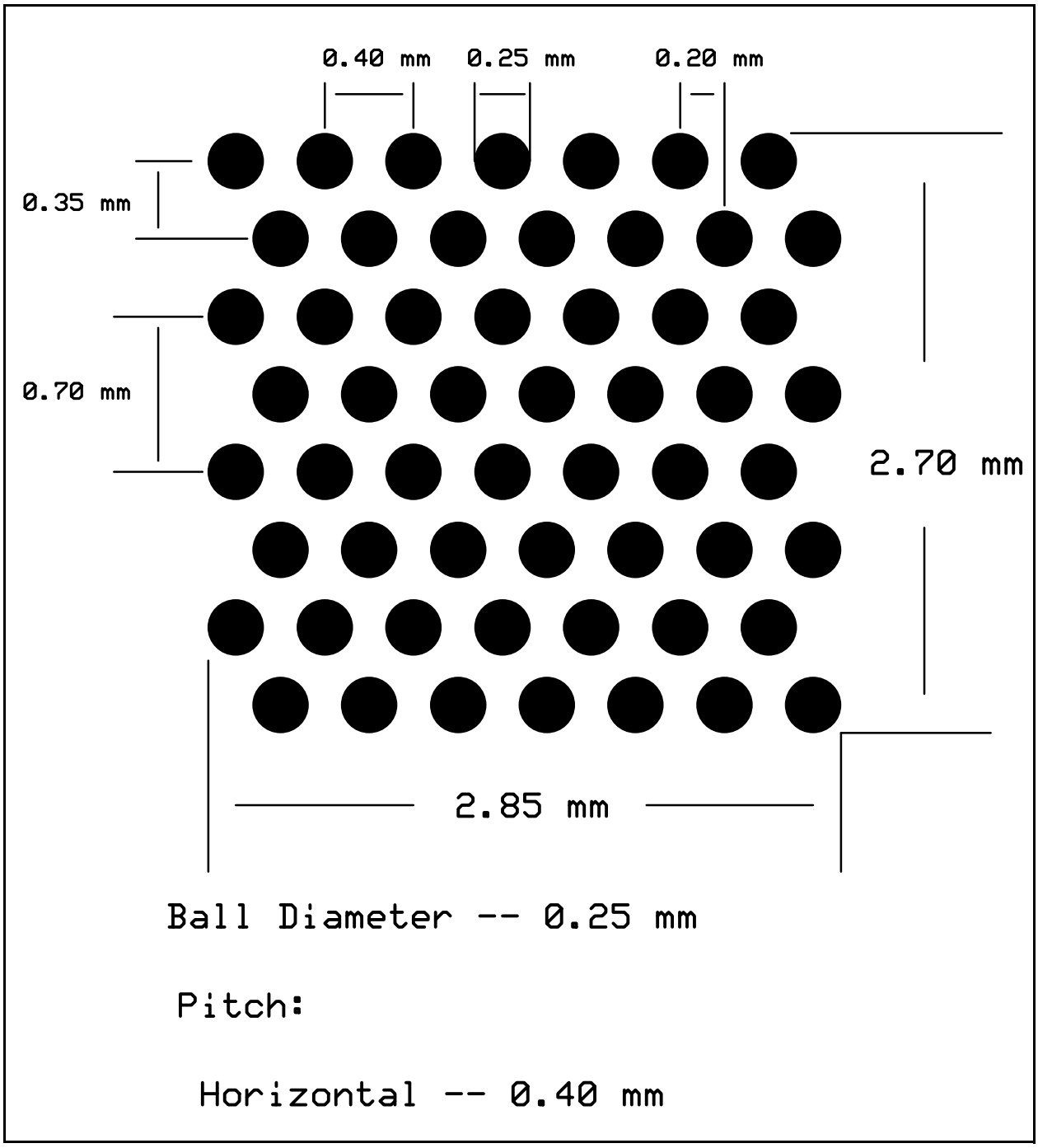


Attribute	Symbol	Mils Min	Mils Nom	Mils Max	mm Min	mm Nom	mm Max
Total thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/frame thickness	A3	7.48	7.87	8.26	0.19	0.2	0.21
lead width	b	5.91	7.87	9.84	0.15	0.2	0.25
Body size X	D	348.42	354.33	360.23	8.85	9.00	9.15
Body size Y	E	348.42	354.33	360.23	8.85	9.00	9.15
lead pitch	e		19.69			0.5	
EP size X	J	287.4	291.34	295.28	7.3	7.4	7.5
EP size Y	K	287.4	291.34	295.28	7.3	7.4	7.5
lead length	L	13.78	15.75	17.72	0.35	0.40	0.45

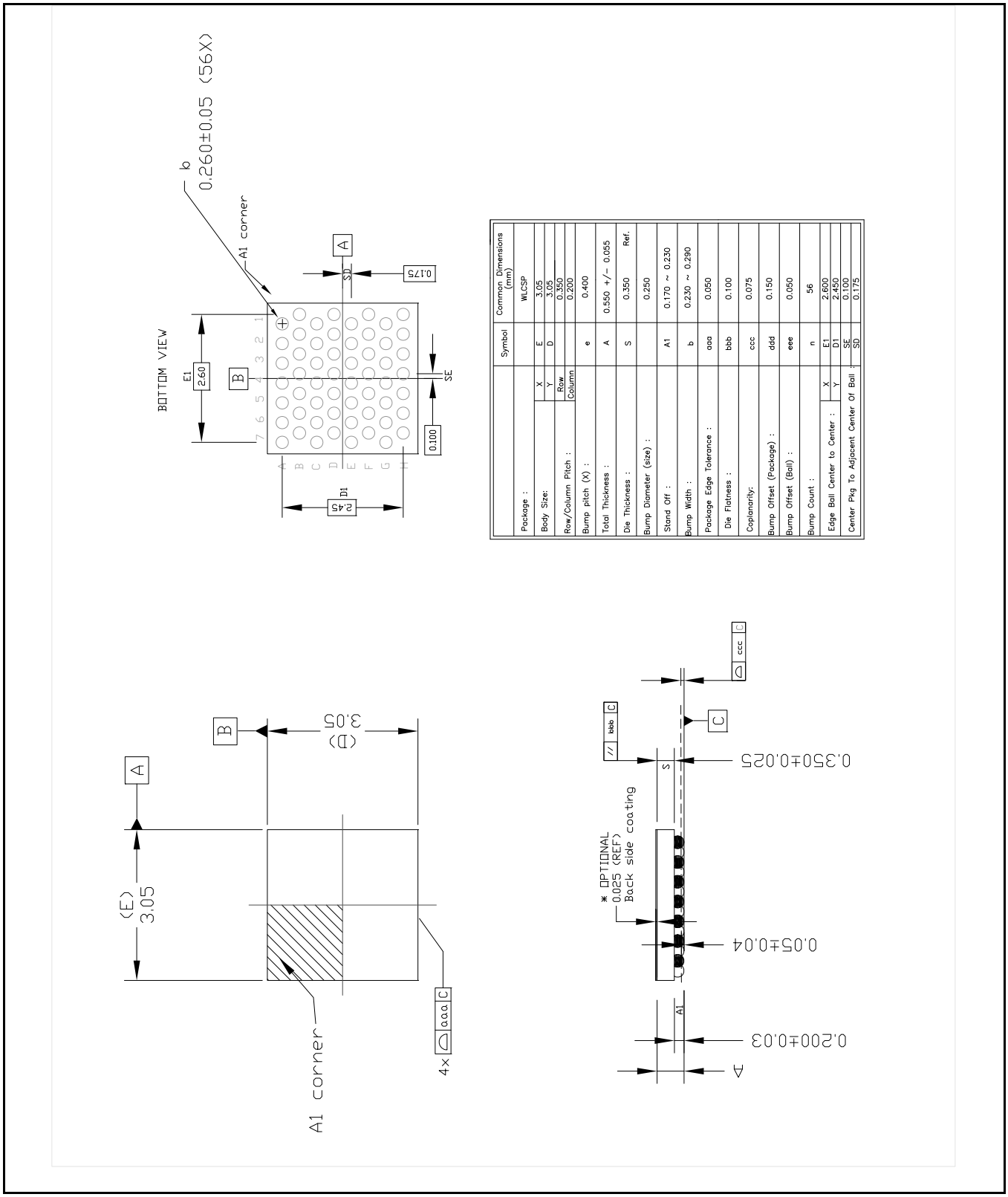
Device Pinout (56-Ball WLCSP) – Top View



Staggered Balls (56-Ball WLCSP) – Bottom View



Package Outline (56-Ball WLCSP)



	Symbol		Common Dimensions (mm)
Package :			WLCSP
Body Size:	X	E	3.05
	Y	D	3.05
Row/Column Pitch :	Row		0.350
	Column		0.200
Bump pitch (X) :		e	0.400
Total Thickness :		A	0.550 +/- 0.055
Die Thickness :		S	0.350 Ref.
Bump Diameter (size) :			0.250
Stand Off :		A1	0.170 ~ 0.230
Bump Width :		b	0.230 ~ 0.290
Package Edge Tolerance :		aaa	0.050
Die Flatness :		bbb	0.100
Coplanarity:		ccc	0.075
Bump Offset (Package) :		ddd	0.150
Bump Offset (Ball) :		eee	0.050
Bump Count :		n	56
Edge Ball Center to Center :	X	E1	2.600
	Y	D1	2.450
Center Pkg To Adjacent Center Of Ball :		SE	0.100
		SD	0.175

Device Pinout

QFN Pin #	WLCSP Ball	Name	Type	Description
15	D6	$\overline{\text{RESET}}$	Input	**Reset.** When low the device is in its reset state and all tristate outputs will be in a high impedance state. This input must be high for normal device operation. *A 10 KΩ pull-up resistor is required on this node to DVDD33 if this pin is not continuously driven.*

Table 1 - Reset Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
6	–	DAC1_M	Output	**DAC 1 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 1. *Not available on the WLCSP package.*
7	C7	DAC1_P		**DAC 1 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 1.
9	–	DAC2_M		**DAC 2 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 2. *Not available on the WLCSP package.*
8	D7	DAC2_P		**DAC 2 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 2.
12	F7	CDAC		**DAC Reference.** This node requires capacitive decoupling.
13	G7	CREF		**Common Mode Reference.** This node requires capacitive decoupling.

Table 2 - DAC Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
18	H6	DMIC_CLK	Output	**Digital Microphone Clock Output.** Clock output for digital microphones and digital electret microphone pre-amplifier devices.
19	H3	DMIC_IN1	Input	**Digital Microphone Input 1.** Stereo or mono digital microphone input. *Tie to VSS if unused.*
20	H2	DMIC_IN2	Input	**Digital Microphone Input 2.** Stereo or mono digital microphone input. *Tie to VSS if unused.*

Table 3 - Microphone Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
29	E1	PCLK/ I2S_SCK	Input/ Output	**PCM Clock (Input/Tristate Output).** PCLK is equal to the bit rate of signals DR/DX. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I^2S Serial Clock (Input/Tristate Output).** This is the I^2S bit clock. In I^2S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I^2S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *A 100 KΩ pull-down resistor is required on this pin to VSS. If this pin is unused, tie the pin to VSS.* *When driving PCLK/I2S_SCK from a host, one of the following conditions must be satisfied:* *1. Host drives PCLK low during reset, or* *2. Host tri-states PCLK during reset (the 100 KΩ resistor will keep PCLK low), or* *3. Host drives PCLK at its normal frequency*
30	F1	FS/ I2S_WS	Input/ Output	**PCM Frame Pulse (Input/Tristate Output).** This is the TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I^2S Word Select (Left/Right) (Input/Tristate Output**). This is the I^2S left or right word select. In I^2S master mode word select is an output which drives the left/right input of the external slave device's peripheral converters. In I^2S slave mode this pin is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *Tie this pin to VSS if unused.*
31	G1	DR/ I2S_SDI	Input	**PCM Serial Data Stream Input.** This serial data stream operates at PCLK data rates. **I^2S Serial Data Input.** This is the I^2S port serial data input. *Tie this pin to VSS if unused.*
32	H1	DX/ I2S_SDO	Output	**PCM Serial Data Stream Output.** This serial data stream operates at PCLK data rates. **I^2S Serial Data Output.** This is the I^2S port serial data output.

Table 4 - TDM and I2S Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
1	A5	SM_CLK	Output	**Master SPI Port Clock (Tristate Output).** Clock output for the Master SPI port. Maximum frequency = 8 MHz.
2	A6	SM_MISO	Input	**Master SPI Port Data Input.** Data input signal for the Master SPI port.
3	A7	SM_MOSI	Output	**Master SPI Port Data Output (Tristate Output).** Data output signal for the Master SPI port.
64	A4	GPIO_9/ SM_CS	Input/ Output	**Master SPI Port Chip Select (Input Internal Pull-Up/Tristate Output).** Chip select output for the Master SPI port. Shared with GPIO_9.

Table 5 - Master SPI Port Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
50	B2	UART_RX	Input	**UART (Input).** Receive serial data in. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.
49	C2	UART_TX	Output	**UART (Tristate Output).** Transmit serial data out. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.

Table 6 - UART Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
33, 34, 36	F4, E4, F3	GPIO_[0:2]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling.
37, 38, 39	F2, –, F6	GPIO_[3:5]		**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signaling. *GPIO_4 is not available on the WLCSP package.*
64	A4	GPIO_9/ SM_CS		**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** This pin can be configured as an input or output and is intended for low-frequency signalling. Alternate functionality with SM_CS.

Table 7 - GPIO Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
41	E2	GPIO_7	Input/ Output	**Hook Switch/Volume Down.** Fixed function used to control the hook state and volume down with GPIO[10:13].
43	D3	GPIO_8		**Microphone/Volume Up.** Fixed function used to control the hook state and volume down with GPIO[10:13].
44	E3	GPIO_10		**Volume Control/Call State.** Fixed function used to control the volume and indicate the call state with GPIO[7:8].
45	C3	GPIO_11		**Call Control/Volume State 1.** Fixed function used to control the hook switch (on/off) and control multicolor LEDs for volume indication with GPIO[7:8].
47	-	GPIO_12		**Volume State 2.** Fixed function used to control multicolor LEDs for volume indication with GPIO[7:8]. *GPIO_12 is not available on the WLCSP package.*
48	-	GPIO_13		**Volume State 3.** Fixed function used to control multicolor LEDs for volume indication with GPIO[7:8]. *GPIO_13 is not available on the WLCSP package.*

Table 8 - Headset Control/Indicator

QFN Pin #	WLCSP Ball	Name	Type	Description
22	H7	XI	Input	**Crystal Oscillator Input.**
23	F5	XO	Output	**Crystal Oscillator Output.**

Table 9 - Oscillator Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
25	H5	USB_DM	Input/ Output	**USB Data D- Signal.** Carries USB data to/from USB 2.0.
26	G4	USB_RTUNE		**Tx Resistor Tune.** Connect to external 43.2 Ω resistor to VSS.
27	H4	USB_DP		**USB Data D+ Signal.** Carries USB data to/from USB 2.0.
40	E5	GPIO_6		**USB Resume.** This pin is used to sense activity on USB Data D+ to resume from sleep or perform a USB reset. It can be configured as an input or output and are intended for low-frequency signaling.

Table 10 - USB Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
17	–	EXT_SEL	Input	**VDD +1.2 V Select.** Select external +1.2 V supply. Tie to DVDD33 if the +1.2 V supply is to be provided externally. Tie to VSS (0 V) if the +1.2 V supply is to be generated internally. *Not available on the WLCSP package.*
16	–	VDD12_CTRL	Output	**VDD +1.2 V Control.** Analog control line for the voltage regulator external FET when EXT_SEL is tied to VSS. When EXT_SEL is tied to DVDD33, the VDD12_CTRL pin becomes a CMOS output which can drive the shutdown input of an external LDO. *Not available on the WLCSP package.*
4, 14, 24, 42, 58	B5, D1, G5, G6	DVDD12	Power	**Core Supply.** Connect to a +1.2 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
5, 21, 35, 46, 51, 59	B3, B7, G3	DVDD33	Power	**Digital Supply.** Connect to a +3.3 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
28	–	DVDD33_ XTAL	Power	**Crystal Digital Supply.** For designs using a crystal or external oscillator, this pin must be connected to a +3.3 V supply source capable of delivering 10 mA. For designs that do not use a crystal or external oscillator this pin can be tied to VSS in order to save power. *Not available on the WLCSP package.*
10, 11	E7	AVDD33	Power	**Analog Supply.** Connect to a +3.3 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
54	B4, B6, D2, D4, E6, G2	VSS	Ground	**Ground.** Connect to digital ground plane.
	–	Exposed Ground Pad	Ground	**Exposed Pad Substrate Connection.** Connect to VSS. This pad is at ground potential and must be soldered to the printed circuit board and connected via multiple vias to a heatsink area on the bottom of the board and to the internal ground plane. *Not available on the WLCSP package.*

Table 11 - Supply and Ground Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
56, 57, 63	A3, C1, C6	NC		**No Connection.** These pins are to be left unconnected, do not use as a tie point.

Table 12 - No Connect Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
52, 53, 55, 60, 61, 62	A1, A2, B1, C4, C5, D5	IN0	Input	**IN0.** Tie these pins to Ground.

Table 13 - IN0 Pin Descriptions

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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