Timberwolf Digital Signal Processor family, powered by *AcuEdge*™ Technology

Designed for IP Cameras with Sound Classification

ZL38052

Product Brief

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Description

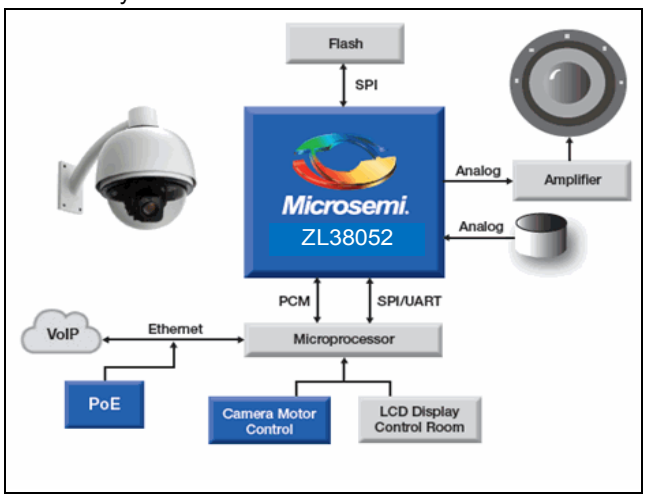
The ZL38052 is part of Microsemi's Timberwolf audio processor family of products. These devices feature Microsemi's innovative *AcuEdge* acoustic technology, which is a set of highly-complex and integrated algorithms. The Microsemi *AcuEdge* Technology ZL38052 is designed to provide leading edge far field microphone processing with advanced features targeted for IP and security cameras with high definition (HD) 2-way hands-free voice.

The Microsemi *AcuEdge* Technology license-free, royalty-free intelligent audio Firmware provides Beamforming, Sound Location Estimation, Acoustic Echo Cancellation (AEC), Noise Reduction and a variety of other voice enhancements to improve both the intelligibility and subjective quality of voice in harsh environments. The ZL38052 also incorporates a sound classification feature allowing the system to recognize smoke detector alarms (T3), carbon monoxide detector alarms (T4) and glass break detection.

Microsemi offers additional tools to speed up the product development cycle. The *MiTuner*™ ZLS38508 or ZLS38508LITE GUI software packages allow a user to interactively configure the ZL38052 device. The optional *MiTuner* ZLE38470BADA Automatic Tuning Kit provides automatic tuning and easy control for manual fine tuning adjustments.

Applications

- IP Cameras
- Security Cameras



Typical IP Security Camera Application

Ordering Information

Device OPN	Package	Packing
ZL38052LDF1	64-pin QFN (9x9)	Tape & Reel
ZL38052LDG1	64-pin QFN (9x9)	Tray
ZL38052UGB2	56-ball WLCSP (3.1x3.1)	Tape & Reel

These packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Microsemi *AcuEdge* Technology ZLS38052 Firmware

There are two Firmware images that may be selected to provide the desired operating mode. Firmware images can be swapped during normal operation to switch modes dynamically. Firmware image size varies with firmware load.

ZLS38052.0 (Full Duplex Communication)

- Far Field Microphone Processing
- Microphone Beamforming
- Sound Location Estimation
- Full Narrowband and Wideband Acoustic Echo cancellation operation
  - Supports long tail AEC (up to 256 ms)
  - Non-Linear AEC provides higher tolerance for speaker distortions
- Howling detection/cancellation
  - Prevents oscillation in AEC audio path
- Advanced noise reduction reduces background noise from the near-end speech signal using Psychoacoustic techniques
- Various encoding/decoding options:16-bit linear, G.722, G.711 A/µlaw
- Send and receive path equalizers

ZLS38052.2 (Glass Break and Energy Detectors)

- Detects T3 (Temporal smoke alarm) signals
- Detects T4 (Temporal carbon monoxide alarm) signals
- Detects the sound of breaking glass
- Programmable Energy Detector

ZL38052 Hardware Features

- DSP with Voice Hardware Accelerators

- 2 digital microphone interfaces allowing sampling of up to 4 digital Microphones
- 2 independent headphone drivers
  - Dual 16-bit digital-to-analog converters (DACs)
  - 16 ohms single-ended or differential drive capability
  - 32 mW output drive power into 16 ohms
- 2 Time-Division Multiplexing (TDM) buses
  - The ports can be configured for Inter-IC Sound (I^2S) or Pulse-Code Modulation (PCM) operation
  - PCM operation supports PCM and GCI timing, I^2S operation supports I^2S and left justified timing
  - Each port can be a clock master or a slave
  - Each port supports up to four bi-directional streams when configured in PCM mode or two bi-directional streams when configured for I^2S mode at data rates from 128 kb/s to 8 Mb/s
- 2 Serial Peripheral Interface (SPI) ports
  - The SPI Slave port is recommended as the main communication port with a host processor. The port provides the fastest means to Host Boot and configures the device's firmware and configuration record*.
  - The Master SPI port is used to Auto Boot and load the device's firmware and configuration record from external Flash memory
- Inter-Integrated Circuit (I^2C) Port (pins shared with SPI Slave Port)
  - The I^2C port can be used as the main communication port with a host processor, and can be used to Host Boot and configure the device's firmware and configuration record
- General purpose Universal Asynchronous Receiver/Transmitter (UART) port for debug
  - The UART port can be used as a debug tool and is used for tuning purposes
- 14 General Purpose Input/Output (GPIO) pins(full operation with Full Duplex Communication Firmware, limited operation with Alarm, Glass Break And Energy Detector Firmware)
  - GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices

The *MiTuner*™ Automatic Tuning Kit and ZLS38508 MiTuner GUI

Microsemi's Automatic Tuning Kit option includes:

- Audio Interface Box hardware
- Microphone and Speaker
- ZLS38508 *MiTuner* GUI software
  - Allows tuning of Microsemi's *AcuEdge* Technology Audio Processor

The ZLS38508 software features:

- Auto Tuning and Subjective Tuning support
- Allows tuning of key parameters of the system design
- Provides visual representations of the audio paths with drop-down menus to program parameters, allowing:
  - Control of the audio routing configuration
  - Programming of key blocks in the transmit (Tx) and receive (Rx) audio paths
  - Setting analog and digital gains
- Configuration parameters allow users to "fine tune" the overall performance

Tools

- ZLK38000 Evaluation Kit
- *MiTuner*™ ZLS38508 and ZLS38508LITE GUI
- *MiTuner*™ ZLE38470BADA Automatic Tuning Kit

Device Block Diagram

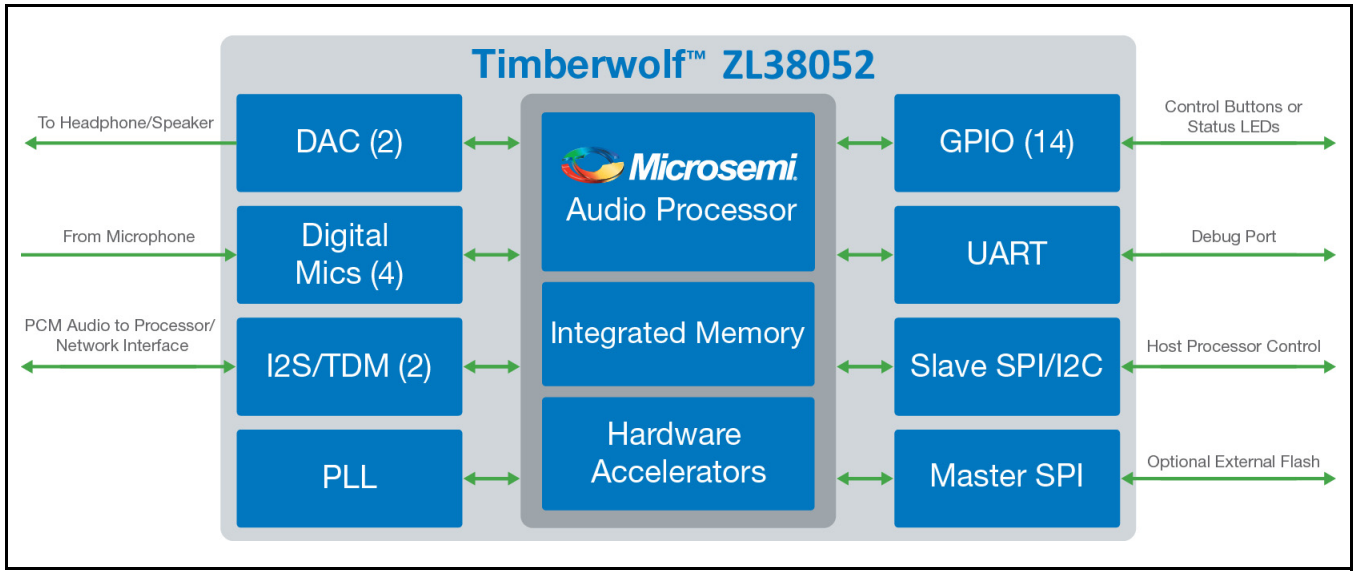
The Microsemi *AcuEdge*™ Technology ZLS38052.0 Firmware offers a sophisticated audio compressor/limiter/expander (CLE) with adjustable attack and decay time. This feature along with Beamforming and advanced Noise Reduction allows for Far Field Microphone pick-up.

Beamforming can be performed with 2 or 3 microphones. The Beamformer uses the signals from multiple microphones to determine the direction of arrival of various sound sources. The beamformer accepts those sources that it determines are in the direction of interest and attenuates those that are deemed to be coming from other directions. By attenuating anything outside of the beam, the microphone pick-up of desired audio improves and the interfering sounds are reduced. The Beamformer's beam width, steering angle, and out-of-beam attenuation are programmable.

The Microsemi *AcuEdge* Technology ZLS38052.0 Firmware Sound Location feature reports the angle at which a sound arrives at the microphones. The Sound Locator can track an audio source with a +/-10 degree accuracy.

The majority of the signal processing (AEC, Equalization, Noise Reduction, Beamforming, CLE, etc.) runs in the Audio Processor Block at 16 kHz. Each of the audio inputs (Digital Mics, I^2S/TDM) and outputs (DACs, I^2S/TDM) can be routed amongst themselves or to the Audio Processor via a highly configurable Cross Point Switch.

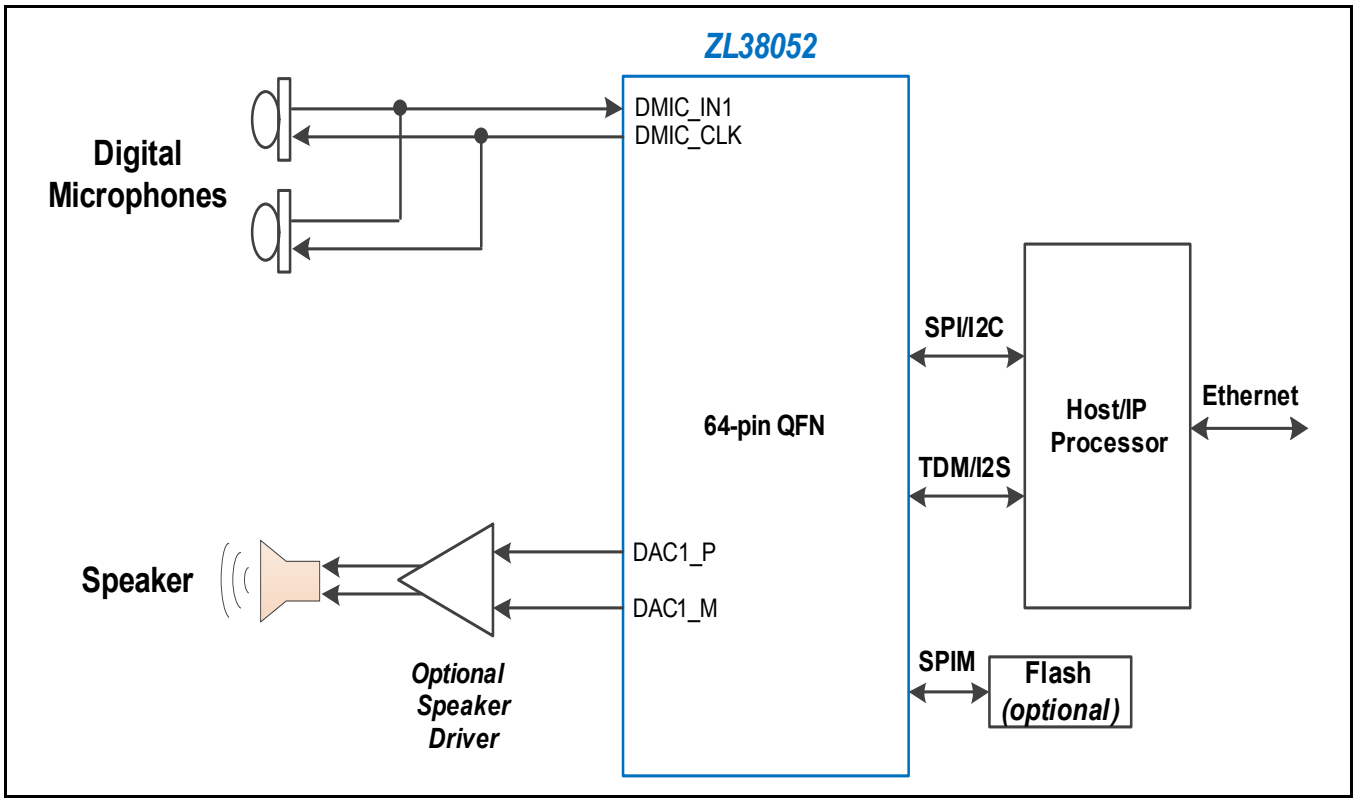
The Microsemi *AcuEdge*™ Technology ZLS38052.2 Firmware offers advanced sound classification for Glass Break and Programmable Energy Detector. The sound classification requires only one microphone. It will detect T3 (temporal smoke alarm) and T4 (temporal carbon monoxide alarm) signals.



ZL38052 IP Camera Audio Processor

Typical Application Block Diagram

The Microsemi *AcuEdge*™ Technology ZL38052 is a hardware platform designed to support advanced features such as far field microphone, sound locator, beamforming, acoustic echo canceller and noise reduction with the ZLS38052 Firmware pack for IP camera applications.

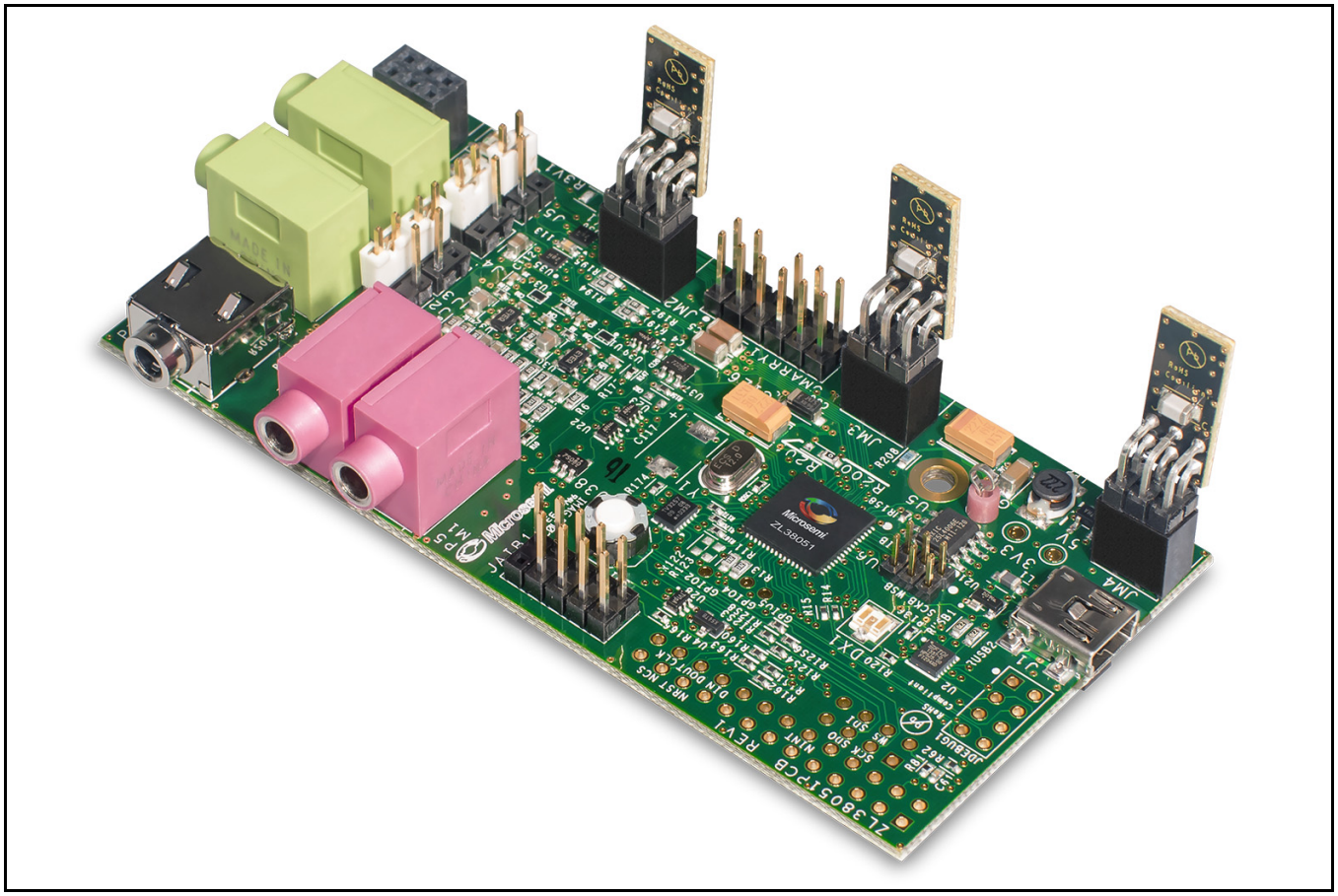


IP Camera HD Voice 2-way Audio Application

ZLK38000 Evaluation Kit

The ZLK38000 Evaluation Kit includes all the hardware necessary to operate the ZLE38000 Evaluation Board. The Evaluation Board provides a flexible platform to evaluate a ZL38052 Timberwolf Audio Processor device with *AcuEdge*™ Technology Firmware.

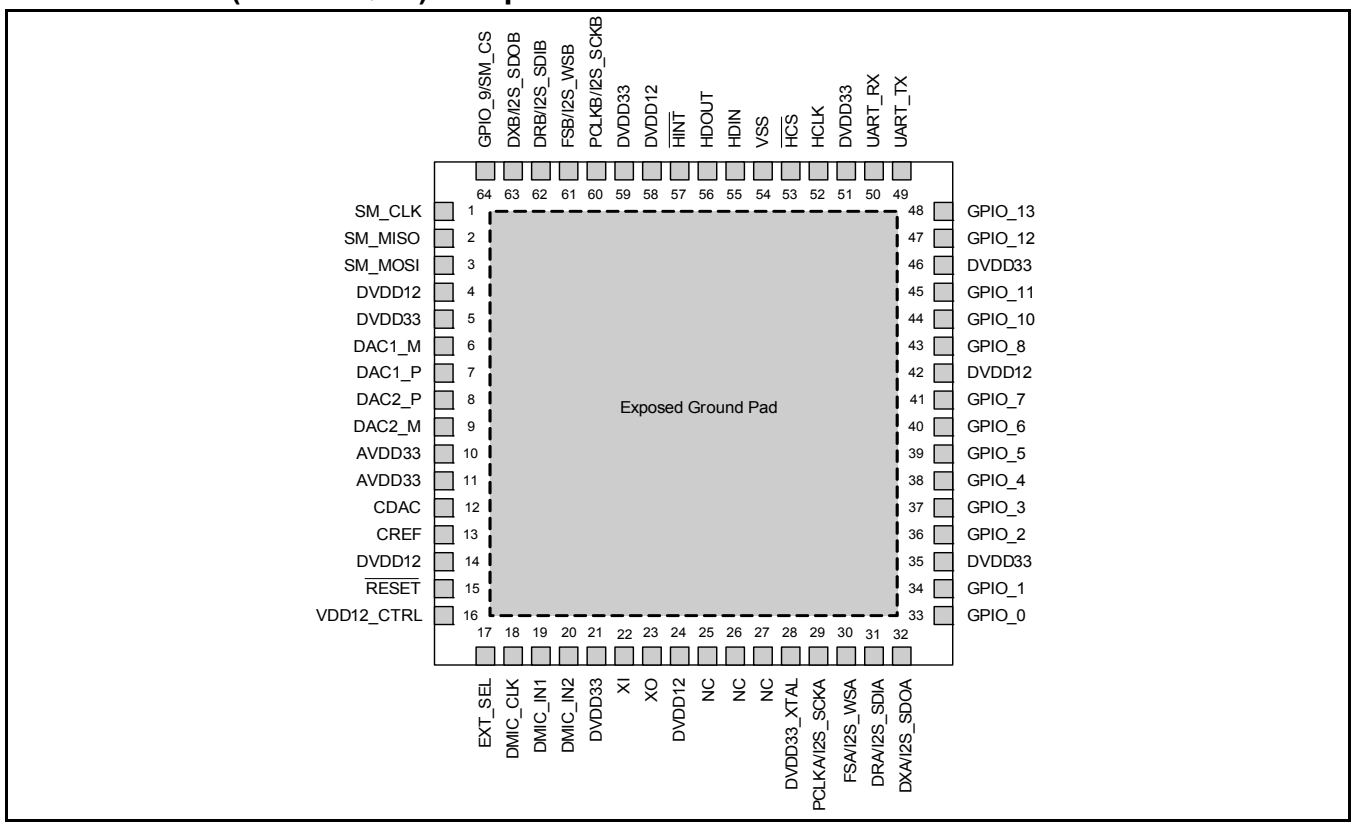
The ZLE38000 Evaluation Board provides a simple analog interface that can be connected to microphones and speakers to allow for subjective testing. The miniature size allows for easy mounting in an existing plastic enclosure.



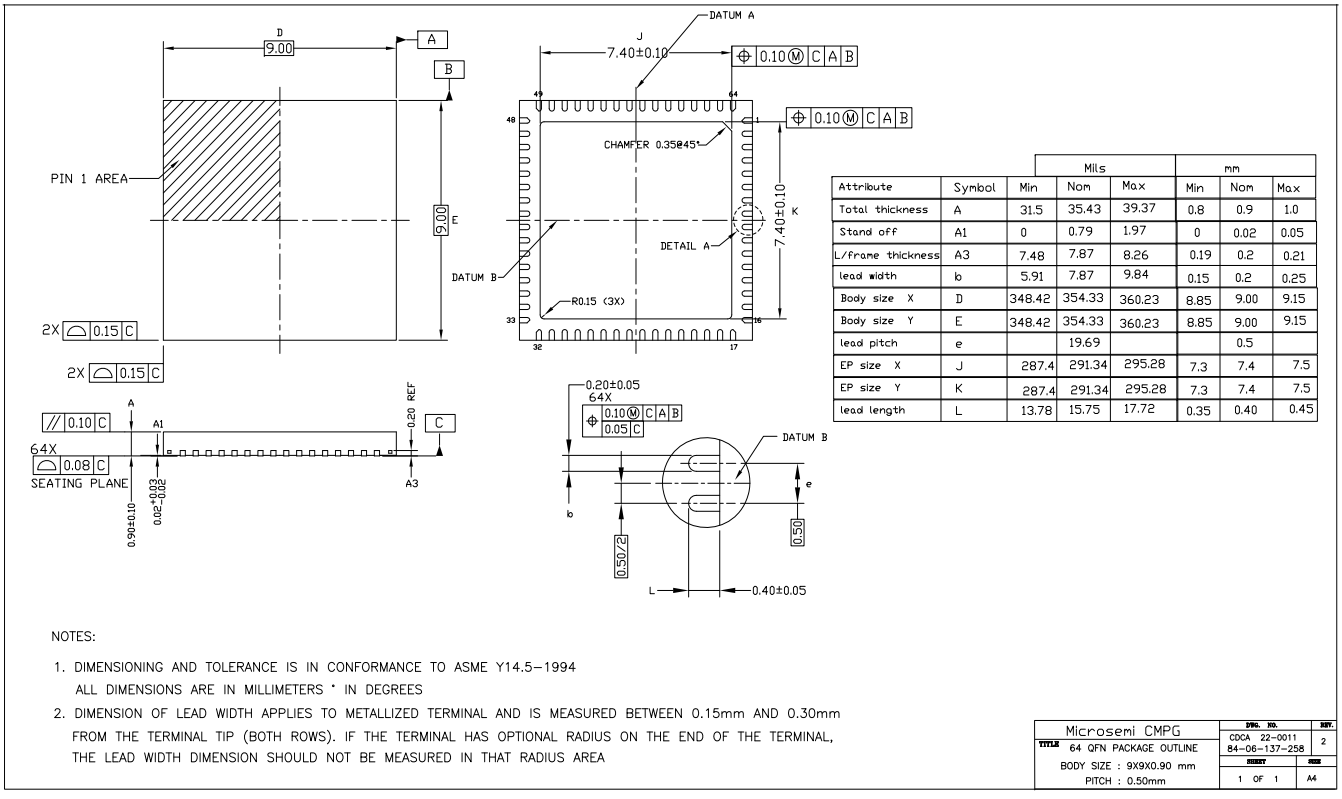
ZLE38000 Evaluation Board

Firmware Code for the ZL38052 can be downloaded into the Evaluation Board using the ZLS38000 Firmware Loader software. The ZLE38000 Evaluation Board can then be controlled using the *MiTuner*™ GUI Lite Software (ZLS38508LITE) or the full *MiTuner* GUI Software package (ZLS38508). Microsemi has developed automatic tuning capability into the full *MiTuner* GUI Software to further facilitate and shorten the design process. The ZLS38508 Software package consists of the *MiTuner* GUI Software and the Audio Interface Box (AIB) Evaluation Kit (ZLE38470BADA) hardware, together performing automatic tuning of the Timberwolf Audio Processor on the Evaluation Board or in a system design.

Device Pinout (64-Pin QFN) – Top View



Package Outline (64-Pin QFN)



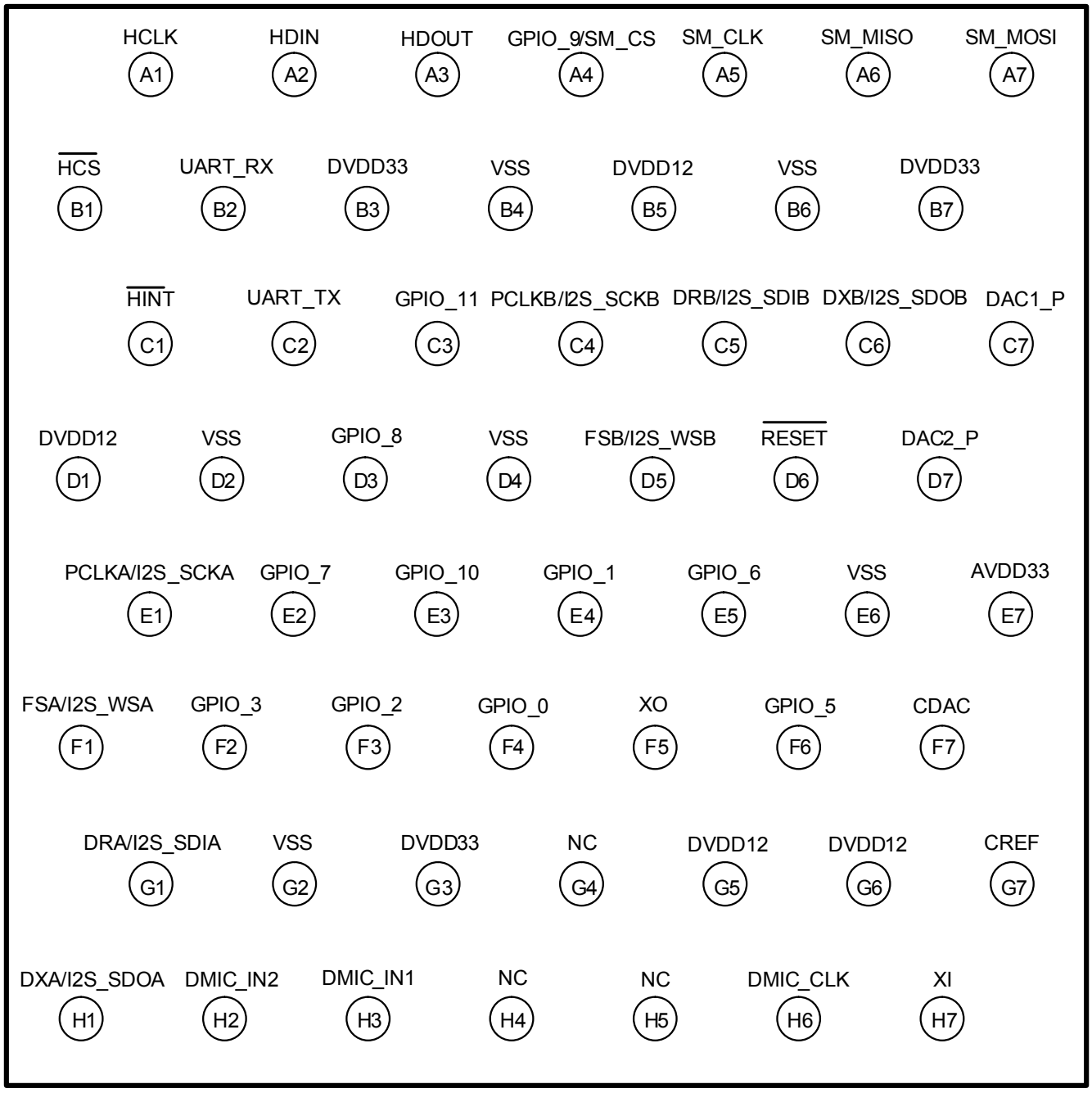
		Mils			mm		
Attribute	Symbol	Min	Nom	Max	Min	Nom	Max
Total thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/frame thickness	A3	7.48	7.87	8.26	0.19	0.2	0.21
lead width	b	5.91	7.87	9.84	0.15	0.2	0.25
Body size X	D	348.42	354.33	360.23	8.85	9.00	9.15
Body size Y	E	348.42	354.33	360.23	8.85	9.00	9.15
lead pitch	e		19.69			0.5	
EP size X	J	287.4	291.34	295.28	7.3	7.4	7.5
EP size Y	K	287.4	291.34	295.28	7.3	7.4	7.5
lead length	L	13.78	15.75	17.72	0.35	0.40	0.45

NOTES:

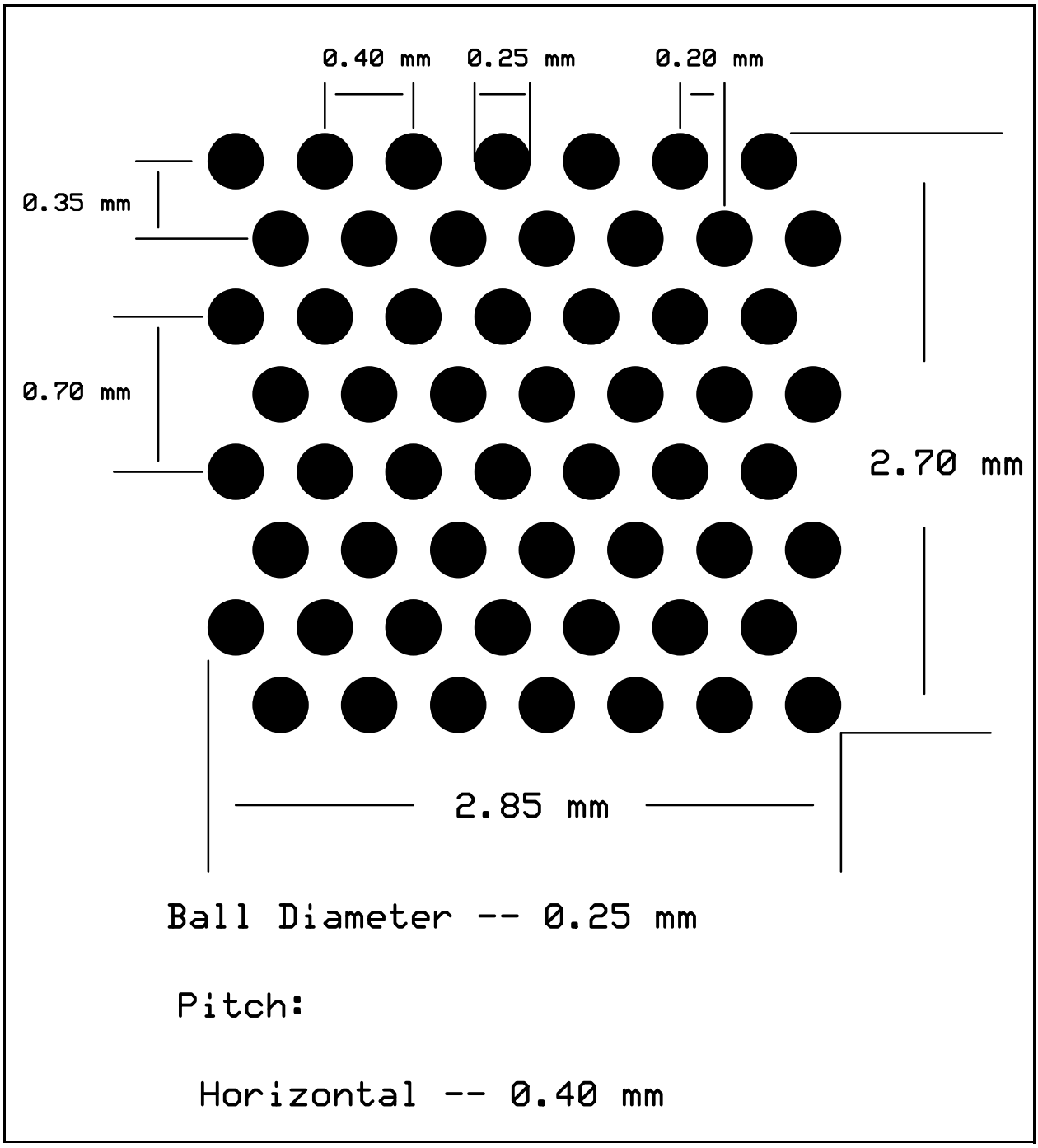
1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG	DWG. NO.	REV.
TITLE: 64 QFN PACKAGE OUTLINE BODY SIZE : 9X9X0.90 mm PITCH : 0.50mm	CDCA 22-0011 84-06-137-258	2
	SHEET 1 OF 1	SIZE A4

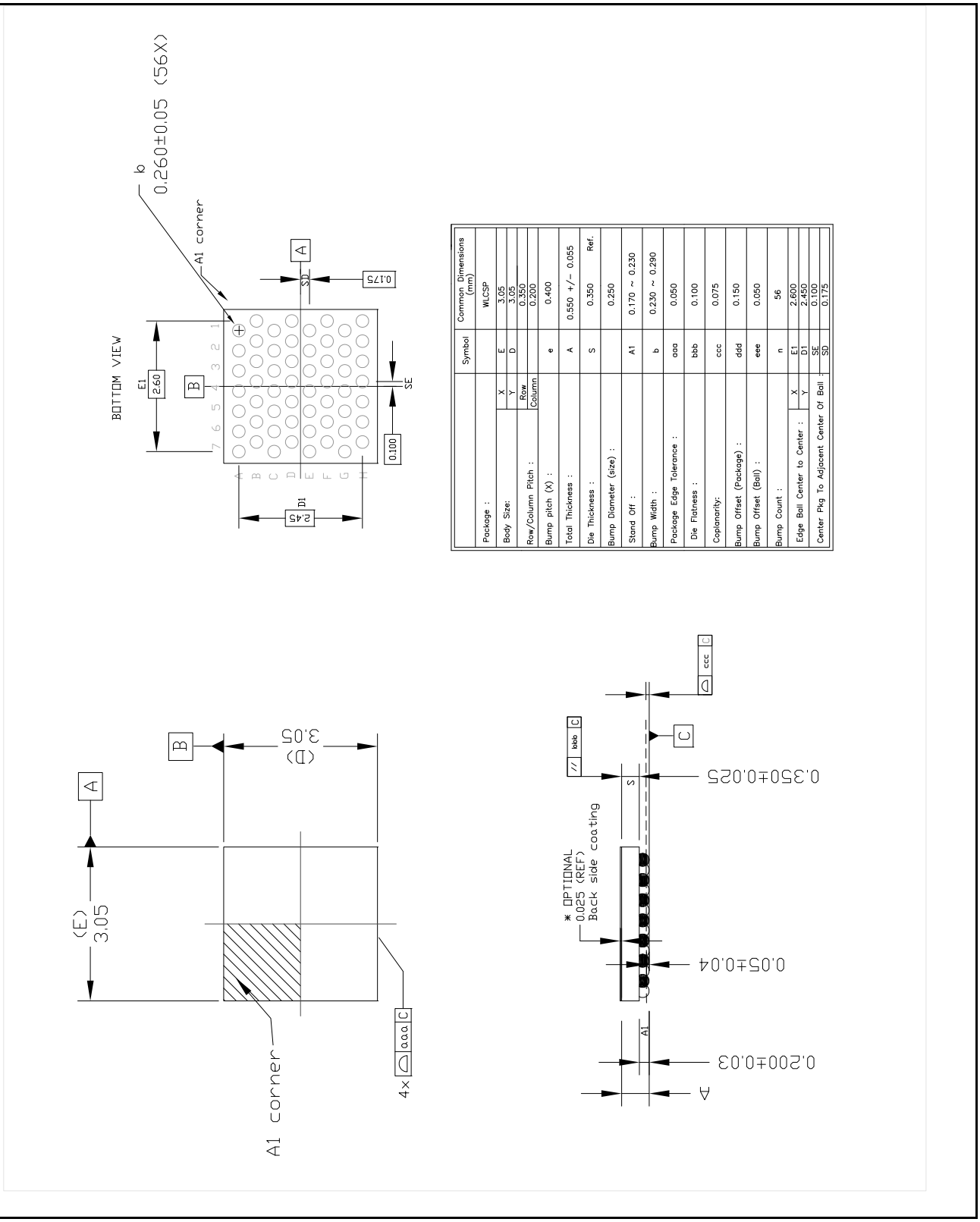
Device Pinout (56-Ball WLCSP) – Top View



Staggered Balls (56-Ball WLCSP) – Bottom View



Package Outline (56-Ball WLCSP)



Pin Descriptions

Table 1 - Reset Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
15	D6	$\overline{\text{RESET}}$	Input	**Reset.** When low the device is in its reset state and all tristate outputs will be in a high impedance state. This input must be high for normal device operation. A 10 KΩ pull-up resistor is required on this node to DVDD33 if this pin is not continuously driven.

Table 2 - DAC Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
6	–	DAC1_M	Output	**DAC 1 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 1. *Not available on the WLCSP package.*
7	C7	DAC1_P	Output	**DAC 1 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 1.
9	–	DAC2_M	Output	**DAC 2 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 2. *Not available on the WLCSP package.*
8	D7	DAC2_P	Output	**DAC 2 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 2.
12	F7	CDAC	Output	**DAC Reference.** This pin requires capacitive decoupling.
13	G7	CREF	Output	**Common Mode Reference.** This pin requires capacitive decoupling.

Table 3 - Microphone Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
18	H6	DMIC_CLK	Output	**Digital Microphone Clock Output.** Clock output for digital microphones and digital electret microphone pre-amplifier devices.
19	H3	DMIC_IN1	Input	**Digital Microphone Input 1.** Stereo or mono digital microphone input. *Tie to VSS if unused.*
20	H2	DMIC_IN2	Input	**Digital Microphone Input 2.** Stereo or mono digital microphone input. *Tie to VSS if unused.*

Table 4 - TDM and I²S Ports Pin Descriptions

The ZL38052 device has two TDM interfaces, TDM-A and TDM-B. Each TDM block is capable of being a master or a slave. The ports can be configured for Pulse-Code Modulation (PCM) or Inter-IC Sound (I²S) operation. The ports conform to PCM, GCI, and I²S timing protocols.

QFN Pin #	WLCSP Ball	Name	Type	Description
29	E1	PCLKA/ I2S_SCKA	Input/ Output	**PCM Port A Clock (Input/Tristate Output).** PCLKA is equal to the bit rate of signals DRA/DXA. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I²S Port A Serial Clock (Input/Tristate Output).** This is the I²S port A bit clock. In I²S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I²S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I²S slave mode. *A 100 KΩ pull-down resistor is required on this pin to VSS. If this pin is unused, tie the pin to VSS.* *When driving PCLKA/I2S_SCKA from a host, one of the following conditions must be satisfied:* *1. Host drives PCLKA low during reset, or* *2. Host tri-states PCLKA during reset (the 100 KΩ resistor will keep PCLKA low), or* *3. Host drives PCLKA at its normal frequency*
30	F1	FSA/ I2S_WSA	Input/ Output	**CM Port A Frame Sync (Input/Tristate Output).** This is the TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I²S Port A Word Select (Left/Right) (Input/Tristate Output**). This is the I²S port A left or right word select. In I²S master mode word select is an output which drives the left/right input of the external slave device's peripheral converters. In I²S slave mode this pin is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I²S slave mode. *Tie this pin to VSS if unused.*
31	G1	DRA/ I2S_SDIA	Input	**PCM Port A Serial Data Stream Input.** This serial data stream operates at PCLK data rates. **I²S Port A Serial Data Input.** This is the I²S port serial data input. *Tie this pin to VSS if unused.*
32	H1	DXA/ I2S_SDOA	Output	**PCM Port A Serial Data Stream Output.** This serial data stream operates at PCLK data rates. **I²S Port A Serial Data Output.** This is the I²S port serial data output.

QFN Pin #	WLCSP Ball	Name	Type	Description
60	C4	PCLKB/ I2S_SCKB	Input/ Output	**PCM Port B Clock (Input/Tristate Output).** PCLKB is equal to the bit rate of signals DRB/DXB. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I^2S Port B Serial Clock (Input/Tristate Output).** This is the I^2S port B bit clock. In I^2S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I^2S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal is an input in I^2S slave mode. *Tie this pin to VSS if unused.*
61	D5	FSB/ I2S_WSB	Input/ Output	**PCM Port B Frame Sync (Input/Tristate Output).** This is the TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I^2S Port B Word Select (Left/Right) (Input/Tristate Output**). This is the I^2S port B left or right word select. In I^2S master mode word select is an output which drives the left/right input of the external slave device's peripheral converters. In I^2S slave mode this pin is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *Tie this pin to VSS if unused.*
62	C5	DRB/ I2S_SDIB	Input	**PCM Port B Serial Data Stream Input.** This serial data stream operates at PCLK data rates. **I^2S Port B Serial Data Input.** This is the I^2S port serial data input. *Tie this pin to VSS if unused.*
63	C6	DXB/ I2S_SDOB	Output	**PCM Port B Serial Data Stream Output.** This serial data stream operates at PCLK data rates. **I^2S Port B Serial Data Output.** This is the I^2S port serial data output.

Table 5 - HBI – SPI Slave Port Pin Descriptions

This port functions as a peripheral interface for an external controller, and supports access to the internal registers and memory of the device.

QFN Pin #	WLCSP Ball	Name	Type	Description
52	A1	HCLK	Input	**HBI SPI Slave Port Clock Input.** Clock input for the SPI Slave port. Maximum frequency = 25 MHz. This input should be tied to VSS in I^2C mode. *Tie this pin to VSS if unused.*
53	B1	$\overline{HCS}$	Input	**HBI SPI Slave Chip Select Input.** This active low chip select signal activates the SPI Slave port. **HBI I^2C Serial Clock Input.** This pin functions as the I2C_SCLK input in I^2C mode. *A pull-up resistor is required on this node for I^2C operation.* *Tie this pin to VSS if unused.*
55	A2	HDIN	Input	**HBI SPI Slave Port Data Input.** Data input signal for the SPI Slave port. This input selects the slave address in I^2C mode. *Tie this pin to VSS if unused.*
56	A3	HDOUT	Input/ Output	**HBI SPI Slave Port Data Output (Tristate Output).** Data output signal for the SPI Slave port. **HBI I^2C Serial Data (Input/Output).** This pin functions as the I2C_SDA I/O in I^2C mode. *A pull-up resistor is required on this node for I^2C operation.*
57	C1	$\overline{HINT}$	Output	**HBI Interrupt Output.** This output can be configured as either CMOS or open drain by the host.

Table 6 - Master SPI Port Pin Descriptions

This port functions as the interface to an external Flash device used to optionally Auto Boot and load the device's firmware and configuration record from external Flash memory.

QFN Pin #	WLCSP Ball	Name	Type	Description
1	A5	SM_CLK	Output	**Master SPI Port Clock (Tristate Output).** Clock output for the Master SPI port. Maximum frequency = 8 MHz.
2	A6	SM_MISO	Input	**Master SPI Port Data Input.** Data input signal for the Master SPI port.
3	A7	SM_MOSI	Output	**Master SPI Port Data Output (Tristate Output).** Data output signal for the Master SPI port.
64	A4	GPIO_9/ $\overline{SM\_CS}$	Input/ Output	**Master SPI Port Chip Select (Input Internal Pull-Up/Tristate Output).** Chip select output for the Master SPI port. Shared with GPIO_9.

Table 7 - UART Pin Descriptions

The ZL38052 device incorporates a two-wire UART (Universal Asynchronous Receiver Transmitter) interface with a fixed 115.2K baud transfer rate, 8 data bits, 1 stop and no parity. The UART port can be used as a debug tool and is used for tuning purposes.

QFN Pin #	WLCSP Ball	Name	Type	Description
50	B2	UART_RX	Input	**UART (Input).** Receive serial data in. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.
49	C2	UART_TX	Output	**UART (Tristate Output).** Transmit serial data out. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.

Table 8 - GPIO Pin Descriptions

GPIO ports can be used for interrupt and event reporting, fixed function control, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices.

QFN Pin #	WLCSP Ball	Name	Type	Description
33, 34, 36	F4, E4, F3	GPIO_[0:2]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling.
37, 38, 39, 40, 41, 43	F2, –, F6, E5, E2, D3	GPIO_[3:8]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling. *GPIO_4 is not available on the WLCSP package.*
64	A4	GPIO_9/ SM_CS	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** This pin can be configured as an input or output and is intended for low-frequency signalling. Alternate functionality with SM_CS.
44, 45, 47, 48	E3, C3, –, –	GPIO_ [10:13]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling. *GPIO_12 and GPIO_13 are not available on the WLCSP package.*

Table 9 - Oscillator Pin Descriptions

These pins are connected to a 12.000 MHz crystal or clock oscillator which drives the device's internal PLL. Alternatively, PCLKA can be used as the internal clock source.

QFN Pin #	WLCSP Ball	Name	Type	Description
22	H7	XI	Input	**Crystal Oscillator Input.**
23	F5	XO	Output	**Crystal Oscillator Output.**

Table 10 - Supply and Ground Pin Descriptions

QFN Pin #	WLCSP Ball	Name	Type	Description
17	–	EXT_SEL	Input	**VDD +1.2 V Select.** Select external +1.2 V supply. Tie to DVDD33 if the +1.2 V supply is to be provided externally. Tie to VSS (0 V) if the +1.2 V supply is to be generated internally. *Not available on the WLCSP package.*
16	–	VDD12_CTRL	Output	**VDD +1.2 V Control.** Analog control line for the voltage regulator external FET when EXT_SEL is tied to VSS. When EXT_SEL is tied to DVDD33, the VDD12_CTRL pin becomes a CMOS output which can drive the shutdown input of an external LDO. *Not available on the WLCSP package.*
4, 14, 24, 42, 58	B5, D1, G5, G6	DVDD12	Power	**Core Supply.** Connect to a +1.2 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
5, 21, 35, 46, 51, 59	B3, B7, G3	DVDD33	Power	**Digital Supply.** Connect to a +3.3 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
28	–	DVDD33_ XTAL	Power	**Crystal Digital Supply.** For designs using a crystal or external oscillator, this pin must be connected to a +3.3 V supply source capable of delivering 10 mA. For designs that do not use a crystal or external oscillator this pin can be tied to VSS in order to save power. *Not available on the WLCSP package.*
10, 11	E7	AVDD33	Power	**Analog Supply.** Connect to a +3.3 V ±5% supply. *Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.*
54	B4, B6, D2, D4, E6, G2	VSS	Ground	**Ground.** Connect to digital ground plane.
	–	Exposed Ground Pad	Ground	**Exposed Pad Substrate Connection.** Connect to VSS. This pad is at ground potential and must be soldered to the printed circuit board and connected via multiple vias to a heatsink area on the bottom of the board and to the internal ground plane. *Not available on the WLCSP package.*

Table 11 - No Connect Pin Description

QFN Pin #	WLCSP Ball	Name	Type	Description
25, 26, 27	G4, H4, H5	NC		**No Connection.** These pins are to be left unconnected, do not use as a tie point.

For more information about all Microsemi products visit our website at www.microsemi.com

TECHNICAL DOCUMENTATION – NOT FOR RESALE

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