Microsemi FPGA TechBytes

Microsemi
Power Matters.™

Newest FPGA Development Software Release **- Libero SoC v11.7**

This latest release of Microsemi's easy-to-adopt Libero System on Chip (SoC) design software offers a significantly improved user experience due to a new and enhanced constraints flow with a new constraints management view, a fully redesigned ChipPlanner, and a new Simultaneous Switching Noise (SSN) Analyzer. Customers will also benefit greatly from SmartDebug updates with improved navigation of the user's design, an improved remote workflow installation, and a SERDES BER calculator.

Read Release Notes and Dowlnoad Now Libero Videos Watch Now

Reliability

Single Event Effect Failures in Ground Level Apps

Modern ICs are susceptible to radiation effects at ground level due to atmospheric neutrons and terrestrial radiation. Learn how single event effects (SEE) in FPGAs can affect high-availability or high-reliability systems. Watch Now

Application – Motor Control

Microsemi's multi-axis deterministic motor control solution consists of a fully modular motor control IP suite, hardware development platform, and GUI-based motor control software. Learn more about this solution from Microsemi experts Watch Now

Intellectual Property – JESD204B

Microsemi now offers transmit and receive cores conforming to the JEDEC JESD204B standard. This specification describes a high-speed serial interface for data converters. These IP cores support two default data rates: 1.25 Gbps and 2.5 Gbps per lane.

JESD204BTX Transmitter JESD204BRX Receiver

Partner Solutions – Mikroprojekt

Mikroprojekt's SmartFusion2 HMI KIT is an intelligent display module based on Microsemi's SmartFusion2 SoC FPGA which enables easy design and deployment of touchscreen GUIs. It is designed for use with Mikroprojekt's IQ Editor and integrates Mikroprojekt's HMI solutions. - Learn More About HMI

Microsemi Training Courses

Microsemi Libero SoC training is a two-day course offered at Microsemi's facility in San Jose, CA. The course consists of lectures and hands-on labs using VHDL or Verilog. Each student will use Libero SoC to completion, targeting the Microsemi SmartFusion2 devices.

Course Schedules Course Descriptions

In The News

Microsemi's high-security, high-reliability IGLOO2 FPGAs achieve AEC-Q100 Grade 1 specification for automotive applications. These newly-evaluated products offer the highest operating temperature in their class. Read Full Release

Recent Articles

Microcontroller-based FPGAs hit the mark – Ted Marena

Q & A with Microsemi – Shakeel Peera

Biggest security threats for embedded designers – Ted Marena

Single Event Effects Webinar

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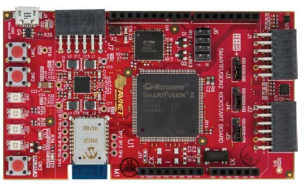
ARROW SF2+ Development Kit Video



Avnet KickStarter Kit Videos

Mikroprojekt HMI Webinar on-Demand

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Center of Excellence

Serial Protocols Expert – Jamie Freed

Q) How did you become such an expert on SERDES transceivers?

A) In 2000, I was working as an application engineer in the ORCA FPGA group of Lucent Technologies when we released the first FPGA with integrated SERDES running at a blazing 622 Mbps. The application for this new device was to provide flexible bridging interfaces for SONET STS-12 backplanes. That was how my career in SERDES began. I spent the next several years supporting five generations of SERDES devices with Lattice Semiconductor. In 2012, I joined the SoC team of Microsemi as product marketing manager for transceivers and protocols working with the SmartFusion2 and IGLOO2 generation of products.

Q) The built-in PCIe Gen2 core in the IGLOO2 and SF2 is very comprehensive. For a design needing PCIe Gen2 x1 interface, how many additional LEs will typically be required?

A) That would be zero. The SmartFusion2 and IGLOO2 embedded PCIe solution covers the entire protocol stack from the differential pins, up through the transaction layer, and is presented to the user as an AXI3 master and slave. This complete solution makes using PCIe extremely easy by isolating all of the PCIe protocol behind an AXI3 bus. The PCIe solution comes complete with several example designs and easy simulation support with BFM models for the AXI3 master and slave.

Q) Has Microsemi released any enhanced Ethernet interfaces?

A) The SmartFusion2 and IGLOO2 family supports 10/100, 1 GbE, and 10 GbE interfaces. We have a series of Ethernet IP cores around triple-speed Ethernet rates of 10, 100, 1000 M using both serial and GMII-based interfaces.

Q) Tell us something about yourself that we would be surprised to know?

A) My wife and I have thirteen children together. No twins- seven boys, six girls, from the age of eighteen down to six months. We started with our first boy when we were both twenty-two and simply kept rolling. They are a great joy in our life.