Libero® SoC v2022.3

RTG4™ DDR Memory Controller Configuration User Guide

Introduction

The RTG4™ FPGA has the following two DDR memory controller blocks located on the East and West side of the chip.

- East Fabric External Memory DDR (FDDR)
- West FDDR

The DDR controllers control off-chip DDR memories. Perform the following steps to fully configure the RTG4 DDR memory controller.

1. Using the RTG4 DDR Memory Controller Configurator to configure the DDR controller, select its datapath bus interface (AXI or AHB), and then select the DDR clock frequency and the fabric datapath clock frequency.
2. Set the register values for the DDR controller registers to match your external DDR memory characteristics.
3. Instantiate the DDR controller as part of a user application and make datapath connections.
4. Connect the DDR controller's APB configuration interface as defined by the peripheral initialization solution.

Table of Contents

Introduction....1

1. Fabric External Memory DDR Controller Configurator....3
   - 1.1. Memory Settings....3
   - 1.2. Fabric Interface Settings....3

2. FDDR Controller Configuration....6
   - 2.1. Fabric DDR Control Registers....6
   - 2.2. Importing DDR Configuration Files....8
   - 2.3. Exporting DDR Configuration Files....9
   - 2.4. Fabric DDR Initialization....10

3. Port Description....18
   - 3.1. FDDR Core Ports....18
   - 3.2. Interrupt Ports....18
   - 3.3. APB3 Configuration Interface....18
   - 3.4. DDR PHY Interface....19
   - 3.5. AXI Bus Interface....20
   - 3.6. AHB0 Bus Interface....21
   - 3.7. AHB1 Bus Interface....22

4. Revision History....24

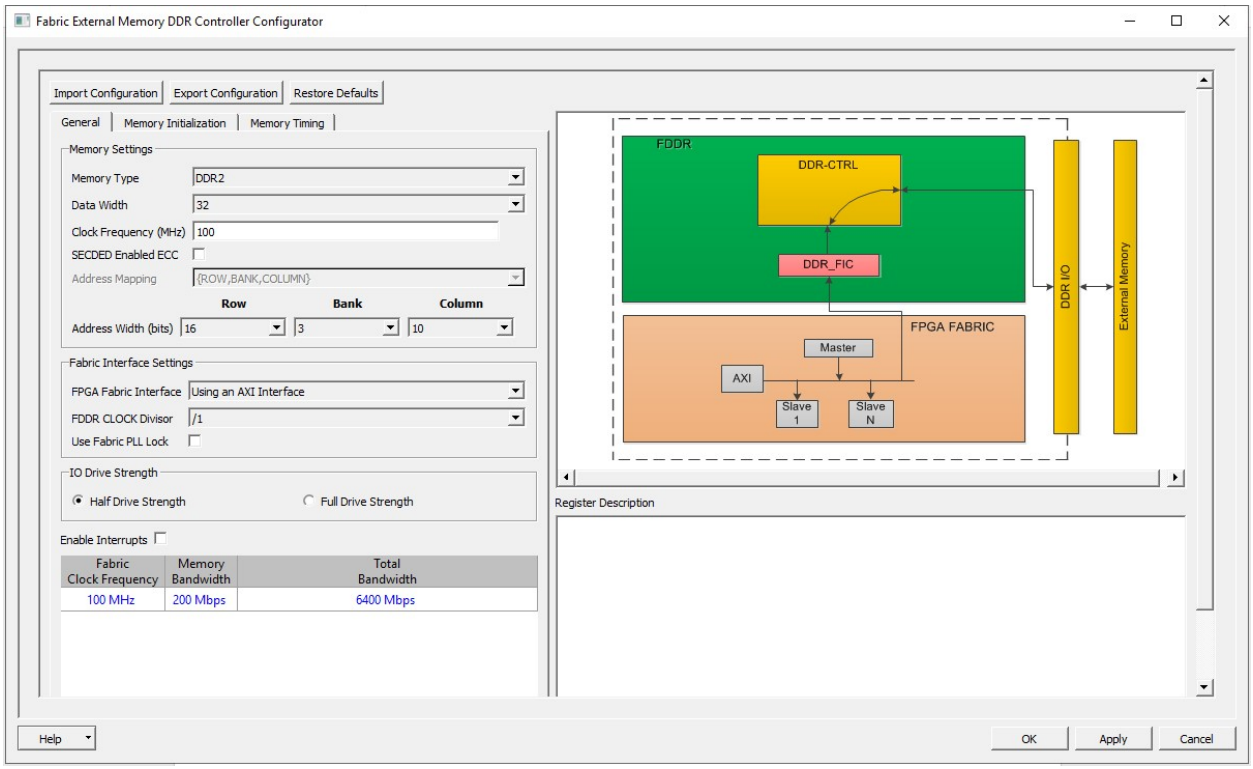
Microchip FPGA Support....25

Microchip Information....25
- The Microchip Website....25
- Product Change Notification Service....25
- Customer Support....25
- Microchip Devices Code Protection Feature....25
- Legal Notice....26
- Trademarks....26
- Quality Management System....27
- Worldwide Sales and Service....28

1. Fabric External Memory DDR Controller Configurator

The FDDR configurator is used to configure the overall datapath and the external DDR memory parameters for the Fabric DDR controller.

Figure 1-1. FDDR Configurator Overview



1.1 Memory Settings

Use **Memory Settings** to configure your memory options in the MDDR.

- **Memory Type**: LPDDR, DDR2, or DDR3.
- **Data Width**: 32-bit, 16-bit, or 8-bit.
- **Clock Frequency**: Any value (decimal/fractional) in the range of 20 to 333 MHz.
- **SECDED Enabled ECC**: ON or OFF.
  This is Single Error Correction Double Error Detection (SECDED) ECC feature of DDR/LPDDR.

1.2 Fabric Interface Settings

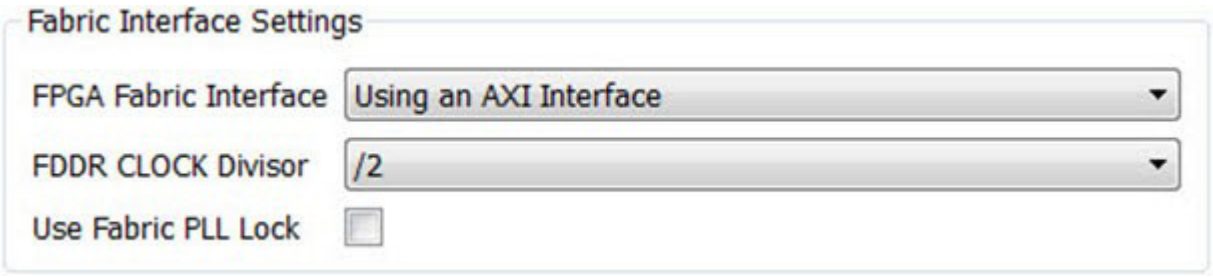
FPGA Fabric Interface

This is the data interface between the FDDR and the FPGA design. As FDDR is a memory controller, it is a target on an AXI or AHB bus. The initiator of the bus initiates bus transactions, which are in turn interpreted by FDDR as memory transactions and communicated to the off-chip DDR Memory. FDDR fabric interface options are:

- **Using an AXI-64 Interface**: One initiator accesses the FDDR through a 64-bit AXI interface.
- **Using a Single AHB-32 Interface**: One initiator accesses the FDDR through a single 32-bit AHB interface.
- **Using Two AHB-32 Interfaces**: Two initiators can access the FDDR using two 32-bit AHB interfaces.

FPGA CLOCK Divisor
Specifies the frequency ratio between the DDR controller clock (CLK_FDDR) and the clock controlling the fabric interface (CLK_FIC64). The CLK_FIC64 frequency must be equal to that of the AHB/AXI subsystem that is connected to the FDDR AHB/AXI bus interface. For example, if you have a DDR RAM running at 200 MHz and your Fabric/AXI Subsystem runs at 100 MHz, then you must select a divisor of 2. See the following figure.

Figure 1-2. Fabric Interface Settings-AXI Interface and FDDR Clock Divisor Agreement



Use Fabric PLL LOCK
If CLK_BASE is sourced from a Fabric CCC, then you can connect the fabric CCC LOCK output to the FDDR FAB_PLL_LOCK input. CLK_BASE is not stable until the Fabric CCC locks. Therefore, Microchip recommends that you hold the FDDR in reset (that is, assert the CORE_RESET_N input) until CLK_BASE is stable. The LOCK output of the Fabric CCC indicates that the Fabric CCC output clocks are stable. By checking the Use FAB_PLL_LOCK option, you can expose the FAB_PLL_LOCK input port of the FDDR. You can then connect the LOCK output of the Fabric CCC to the FAB_PLL_LOCK input of the FDDR.

1.2.1 I/O Drive Strength (DDR2 and DDR3 only)

Select one of the following drive strengths for your DDR I/Os:

- Half Drive Strength
- Full Drive Strength

Depending on your DDR Memory type and the I/O Strength you select, Libero® SoC sets the DDR I/O Standard for your FDDR system, as listed in the following table.

Table 1-1. DDR I/O Standard (For FDDR System)

DDR Memory Type	Half Drive Strength	Full Drive Strength
DDR3	SSTL15I	SSTL15II
DDR2	SSTL18I	SSTL18II

1.2.2 I/O Standard (LPDDR Only)

Select one of the following options:

- LVCMOS18 (lowest power) for LVCMOS 1.8V IO standard.
- LPDDRI

Important: Before you choose this standard, ensure that your board supports this standard.

1.2.3 I/O Calibration

Choose one of the following options:

- ON
- OFF

Calibration ON and OFF provide different values for PCODE and NCODE registers. The I/O calibration block calibrates the I/O drivers to an external resistor. The impedance control is used to identify the digital values PCODE<5:0> and NCODE<5:0>. These values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor. Once it matches the PCODE and NCODE registers, they are latched and sent to the drivers. Users turn on or turn off this feature as per their board requirements.

1.2.4 Enable Interrupts

The FDDR is capable of raising interrupts when certain predefined conditions are satisfied. Check **Enable Interrupts** in the FDDR configurator if you use these interrupts in your application. This exposes the interrupt signals on the FDDR instance. You can connect these interrupt signals as your design requires. The following Interrupt signals and their preconditions are available:

- **FIC_INT**: Generated when there is an error in the transaction between the Initiator and the FDDR.
- **IO_CAL_INT**: Enables you to recalibrate DDR I/Os by writing to DDR controller registers via the APB configuration interface. When calibration is complete, this interrupt is raised. For details about I/O recalibration, see the *RTG4™ User Guide*.
- **PLL_LOCK_INT**: Indicates that the FDDR FPLL has locked.
- **PLL_LOCKLOST_INT**: Indicates that the FDDR FPLL has lost lock.
- **FDDR_ECC_INT**: Indicates that a single-bit or two-bit error has been detected.

1.2.5 Fabric Clock Frequency

Clock frequency (CLK_BASE) calculation based on your current DDR Controller Clock (CLK_FDDR) frequency and the FDDR CLOCK divisor, displayed in MHz.

Fabric Clock (CLK_BASE) Frequency (in MHz) = CLK_FDDR Clock Frequency/FDDR CLOCK divisor.

1.2.6 Memory Bandwidth

Memory bandwidth calculation based on your current Clock Frequency value in Mbps.
Memory Bandwidth (in Mbps) = 2 * Clock Frequency

1.2.7 Total Bandwidth

Total bandwidth calculation is based on your current Fabric Clock Frequency (CLK_BASE), DDR, Data Width, and FDDR CLOCK divisor, in Mbps.

Total Bandwidth (in Mbps) = (2 * Fabric Clock Frequency * DDR Data Width)/FDDR CLOCK divisor.

2. FDDR Controller Configuration

When you use the Fabric DDR Controller to access an external DDR Memory, the DDR Controller must be configured at run time. This is done by writing configuration data to dedicated DDR controller configuration registers. This configuration data is dependent on the characteristics of the external DDR memory and your application. This section describes how to enter these configuration parameters in the FDDR controller configurator and how to build the initialization circuitry for the FDDR Controller after the FDDR controller is configured.

2.1 Fabric DDR Control Registers

The Fabric DDR Controller has a set of registers that must be configured at run time. The configuration values for these registers represent different parameters (for example, DDR mode, PHY width, burst mode, ECC, and so on). For details about the DDR controller configuration registers, see the UG0741: RTG4 FPGA I/O User Guide.

2.1.1 Fabric DDR Registers Configuration

Use the **Memory Initialization** for Figure 2-1 and **Memory Timing** for Figure 2-2 tabs to enter parameters that correspond to your DDR memory and application. Consult your DDR memory vendor's datasheet for values to enter in these two tabs.

Values you enter in these tabs are automatically translated to the appropriate register values. When you click a specific parameter, its corresponding register is described in the **Register Description** window (Figure 1-1).

Figure 2-1. FDDR Configuration-Memory Initialization Tab

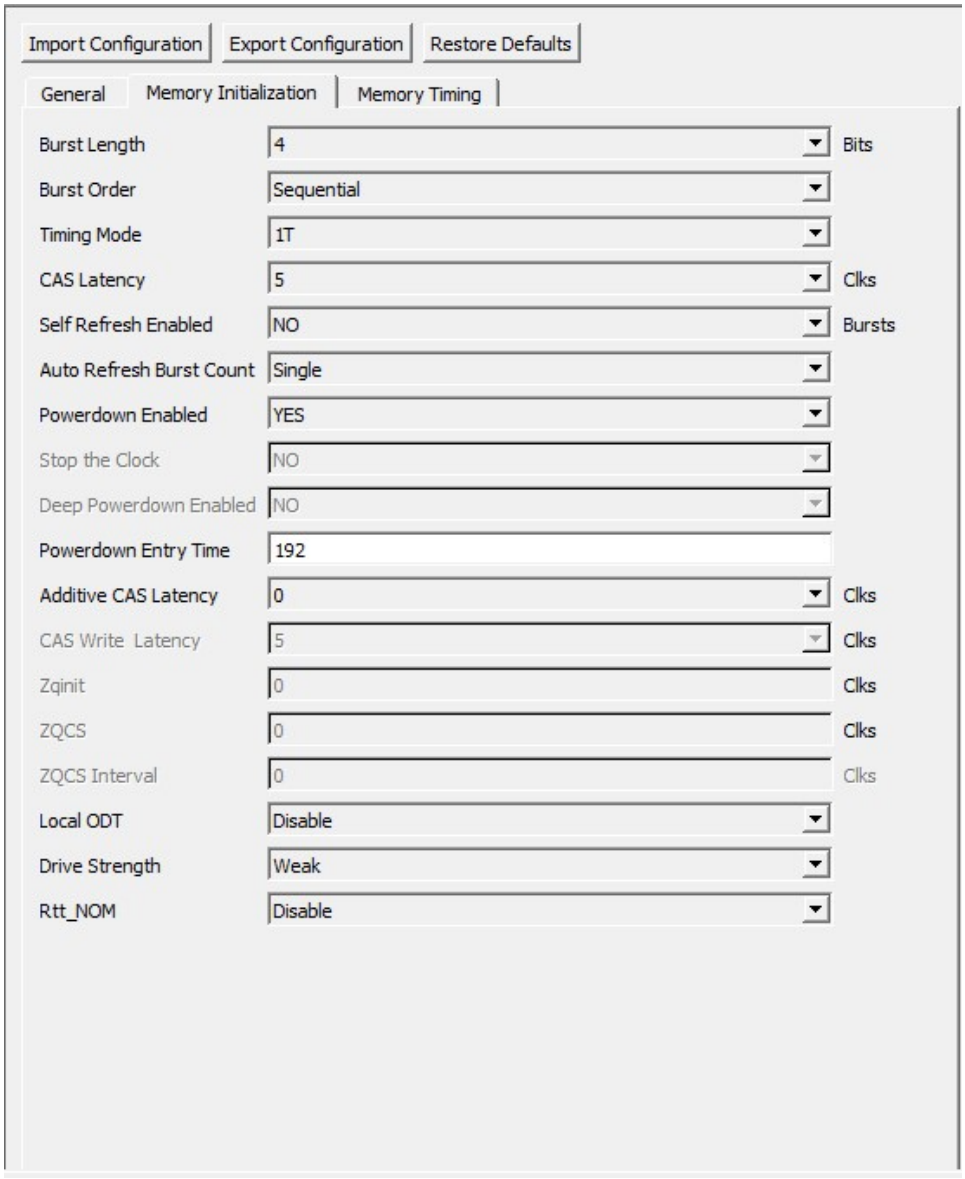
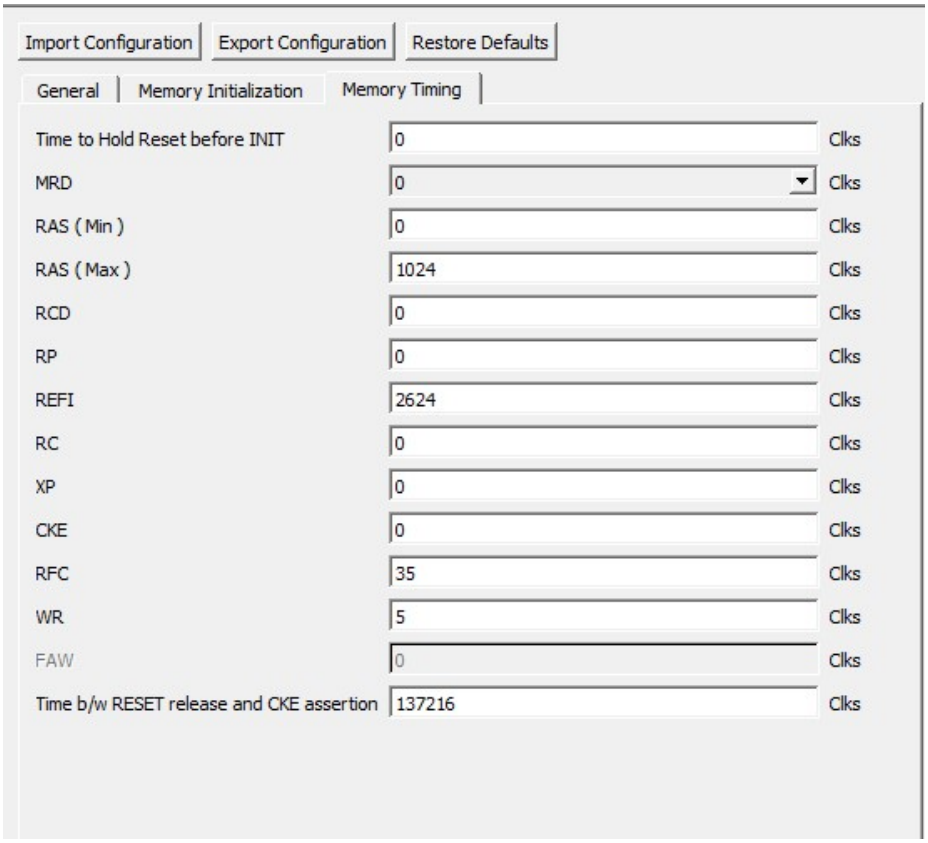


Figure 2-2. FDDR Configuration-Memory Timing Tab



2.2 Importing DDR Configuration Files

In addition to entering DDR Memory parameters using the Memory Initialization and Timing tabs, you can import DDR register values from a file. To do so, click the **Import Configuration** button and navigate to the text file containing DDR register names and values. The following figure shows the import configuration syntax.

Figure 2-3. DDR Register Configuration File Syntax

```
ddrc_dyn_soft_reset_CR          0x00 ;
ddrc_dyn_refresh_1_CR           0x27DE ;
ddrc_dyn_refresh_2_CR           0x030F ;
ddrc_dyn_powerdown_CR           0x02 ;
ddrc_dyn_debug_CR               0x00 ;
ddrc_ecc_data_mask_CR           0x0000 ;
ddrc_addr_map_col_1_CR          0x3333 ;
ddrc_addr_map_col_3_CR          0x3300 ;
ddrc_init_1_CR                  0x0001 ;
ddrc_cke_rstn_cycles_CR1        0x0100 ;
ddrc_cke_rstn_cycles_CR2        0x0008 ;
ddrc_init_emr2_CR               0x0000 ;
ddrc_init_emr3_CR               0x0000 ;
ddrc_dram_bank_act_timing_CR    0x1947;
```

Important: If you choose to import register values rather than entering them using the GUI, you must specify all necessary register values. See the SmartFusion2 SoC FPGA Documentation for details.

2.3 Exporting DDR Configuration Files

You can also export the current register configuration data into a text file. This file contains register values that you imported (if any) and those that were computed from GUI parameters you entered in this dialog.

If you want to undo changes you have made to the DDR register configuration, you can do so with Restore Default. This deletes all register configuration data and you must either re-import or reenter this data. The data is reset to the hardware reset values.

2.3.1 Generated Data

Click **OK** to generate the configuration. Based on your input in the **General**, **Memory Timing and Memory Initialization** tabs, the FDDR Configurator computes values for all DDR configuration registers and exports these values into your firmware project and simulation files. The exported file syntax is shown in the following figure.

Figure 2-4. Exported DDR Register Configuration File Syntax

```
# Exported: 2022-Sep-08 22:45:53
# Libero DDR Configurator GUI Version = 2.0
# DDR Controller Type = LPDDR
# Bus Width = 32-bits
# Memory Bandwidth = 200 Mbps
# Total Bandwidth = 6400 Mbps
#
# Validation Status:
# Target Device Manufacturer:
# Target Device: M2GL150TS
#
DDRC_ADDR_MAP_BANK_CR.REG_DDRC_ADDRMAP_BANK_B2                                0xf
DDRC_ADDR_MAP_BANK_CR.REG_DDRC_ADDRMAP_BANK_B1                                0xa
DDRC_ADDR_MAP_BANK_CR.REG_DDRC_ADDRMAP_BANK_B0                                0xa
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B7                                0x3
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B4                                0x3
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B3                                0x3
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B2                                0x3
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B11                               0xf
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B10                               0xf
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B9                                0xf
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B8                                0x3
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_DIS_SCRUB                                     0x0
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_DIS_COLLISION_PAGE_OPT                        0x0
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_DIS_PRE_BYPASS                                0x0
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_DIS_RD_BYPASS                                 0x0
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_DIS_ACT_BYPASS                                0x0
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_DIS_WC                                        0x0
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_ADDRMAP_COL_B6                                0x3
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_ADDRMAP_COL_B5                                0x3
DDRC_ADDR_MAP_ROW_1_CR.REG_DDRC_ADDRMAP_ROW_B12                               0x8
DDRC_ADDR_MAP_ROW_1_CR.REG_DDRC_ADDRMAP_ROW_B2_11                             0x8
DDRC_ADDR_MAP_ROW_1_CR.REG_DDRC_ADDRMAP_ROW_B1                                0x8
DDRC_ADDR_MAP_ROW_1_CR.REG_DDRC_ADDRMAP_ROW_B0                                0x8
DDRC_ADDR_MAP_ROW_2_CR.REG_DDRC_ADDRMAP_ROW_B15                               0x8
DDRC_ADDR_MAP_ROW_2_CR.REG_DDRC_ADDRMAP_ROW_B14                               0x8
DDRC_ADDR_MAP_ROW_2_CR.REG_DDRC_ADDRMAP_ROW_B13                               0x8
DDRC_AXI_FABRIC_PRI_ID_CR.PRIORITY_ID                                         0x0
DDRC_AXI_FABRIC_PRI_ID_CR.PRIORITY_ENABLE_BIT                                 0x0
DDRC_CKE_RSTN_CYCLES_1_CR.REG_DDRC_DRAM_RSTN_X1024                            0x0
DDRC_CKE_RSTN_CYCLES_1_CR.REG_DDRC_PRE_CKE_X1024                              0x42
DDRC_CKE_RSTN_CYCLES_2_CR.REG_DDRC_PRE_CKE_X1024                              0x0
DDRC_CKE_RSTN_CYCLES_2_CR.REG_DDRC_POST_CKE_X1024                             0x2
DDRC_DFI_CTRLUPD_TIME_INTERVAL_CR.REG_DDRC_DFI_T_CTRLUPD_INTERVAL_MAX_X1024   0x9
DDRC_DFI_CTRLUPD_TIME_INTERVAL_CR.REG_DDRC_DFI_T_CTRLUPD_INTERVAL_MIN_X1024   0x3
DDRC_DFI_MAX_CTRLUPD_TIMING_CR.REG_DDRC_DFI_T_CTRLUP_MAX                      0x40
DDRC_DFI_MIN_CTRLUPD_TIMING_CR.REG_DDRC_DFI_T_CTRLUP_MIN                      0x3
DDRC_DFI_RDDATA_EN_CR.REG_DDRC_DFI_T_RDDATA_EN                                0x3
DDRC_DFI_RD_LVL_CONTROL_1_CR.REG_DDRC_RDLVL_RR                                0x0
DDRC_DFI_RD_LVL_CONTROL_1_CR.REG_DDRC_DFI_RDLVL_MAX_X1024                     0x0
DDRC_DFI_RD_LVL_CONTROL_2_CR.REG_DDRC_DFI_RDLVL_MAX_X1024                     0x0
DDRC_DFI_RD_LVL_CONTROL_2_CR.REG_DDRC_DFI_RD_DQS_GATE_LEVEL                   0x0
DDRC_DFI_RD_LVL_CONTROL_2_CR.REG_DDRC_DFI_RD_DATA_EYE_TRAIN                   0x0
```

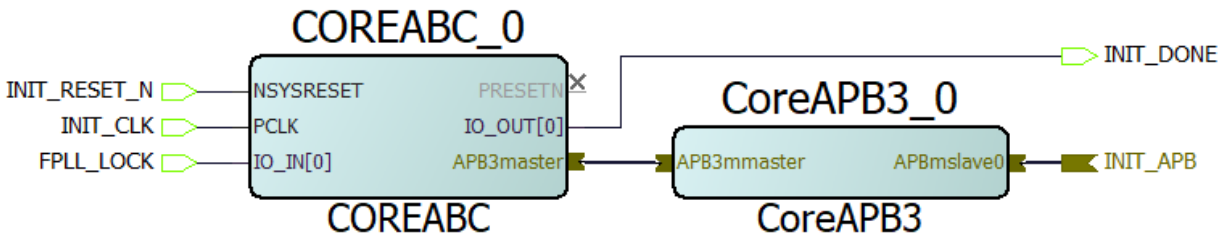
2.4 Fabric DDR Initialization

The Fabric DDR Initialization solution requires that, in addition to specifying Fabric DDR configuration register values, you must build the configuration and initialization circuitry in SmartDesign for your Fabric DDR controller. The following section describes how to build the initialization circuitry in a SmartDesign component FDDR_INIT.

The FDDR_INIT component consists of:

- CoreABC soft IP core
- CoreAPB3 bus Soft IP Core

Figure 2-5. FDDR_INIT SmartDesign Component



2.4.1 Configuring and generating the FDDR component

1. From the Catalog, right click RTG4 DDR Memory controller and choose **Configure Core**.
2. Click **OK** to exit the Configurator when done. Your FDDR component is generated. Libero generates the CoreABC program in the `<project_location>/component/work/<FDDR_component_name>/<FDDR_component_name>_0/fddr_init_abc.txt` file.
3. Some of the functions performed by CoreABC are as follows:
   - Perform the FPLL calibration/workaround, which includes polling for the FPLL_LOCK output from FDDR.
   - Configure the DDR registers.
   - Wait for controller ready and memory settling time, and then assert INIT_DONE.

2.4.2 Building the FDDR Initialization Circuitry with FDDR_INIT Component

After you have configured the RTG4 DDR memory controller, you need to build the initialization circuitry for the FDDR.

1. Create a SmartDesign component with name FDDR_INIT.
2. From the Catalog, drag and drop CoreABC (v3.6.100 or later) to the SmartDesign component FDDR_INIT.
3. Specify a name to the CoreABC component and click **OK** to open its configurator.
4. Configure the CoreABC component as shown in the following figure. Ensure that it has the following selections in the **Parameters** tab:
   - The data bus width is 32.
   - The maximum number of instructions is at least 256.
   - Number of I/O inputs is 1.
   - Number of I/O flags is 1.
   - Number of I/O outputs is 1.
   - Instruction store is hard (FPGA logic elements).
   - Use AND and IOWRT operations as optional instructions.
5. Copy the CoreABC program generated for your FDDR from the `fddr_init_abc.txt` file created under the `<project_location>/component/work/../ <user_FDDR_name>_0/` folder and paste to the **CoreABC Program** tab. The program code loads the DDR controller registers with the values you have configured for your DDR controller and starts the initialization sequence. Depending on the number of instructions generated in the `fddr_init_abc.txt` file, you may have to increase the maximum number of instructions.
6. Click **OK** to exit the configurator when done and generate the CoreABC component.
7. From the **Catalog**, drag and drop CoreAPB3 (v4.1.100 or later) to the SmartDesign component FDDR_INIT.
8. Specify a name to the CoreAPB3 component and click **OK** to open its configurator.
9. Configure the CoreAPB3 component as shown in Figure 2-8. Make sure it has the following selections:
   - APB initiator data bus width is 32.
   - Number of address bits driven by initiator is 20.
   - Enabled APB target slots is slot 0. All other save slots are disabled.
10. Click **OK** to exit the configurator when done and generate the CoreAB3 component.

11. The following table lists the necessary port tie-offs, promotions, and connections between the CoreABC and CoreAPB3 components in the FDDR_INIT SmartDesign canvas. See the Figure 2-5 for the connections and port tie-offs.
12. When completed, click the **Generate** button in the SmartDesign canvas to generate FDDR_INIT component.

Table 2-1. Port tie-offs, Promotions and Connections in FDDR_INIT

Port/Bus Interface (BIF) Name/Block	Action
NSYSRESET/CoreABC	Promote to top and rename to INIT_RESET_N
PCLK/CoreABC	Promote to top and rename to INIT_CLK
IO_IN[0]/CoreABC	Promote IO_IN[0] to top and rename to FPLL_LOCK. This is used to poll for FPLL_LOCK output of the FDDR block.
PRESETN/CoreABC	Mark as unused
IO_OUT[0]/CoreABC	Promote to top and rename to INIT_DONE
APB3master BIF/CoreABC	Connect to APB3mmaster BIF of CoreAPB3
APBmslave0/CoreAPB3	Promote to top and rename to INIT_APB

Figure 2-6. CoreABC Configurator

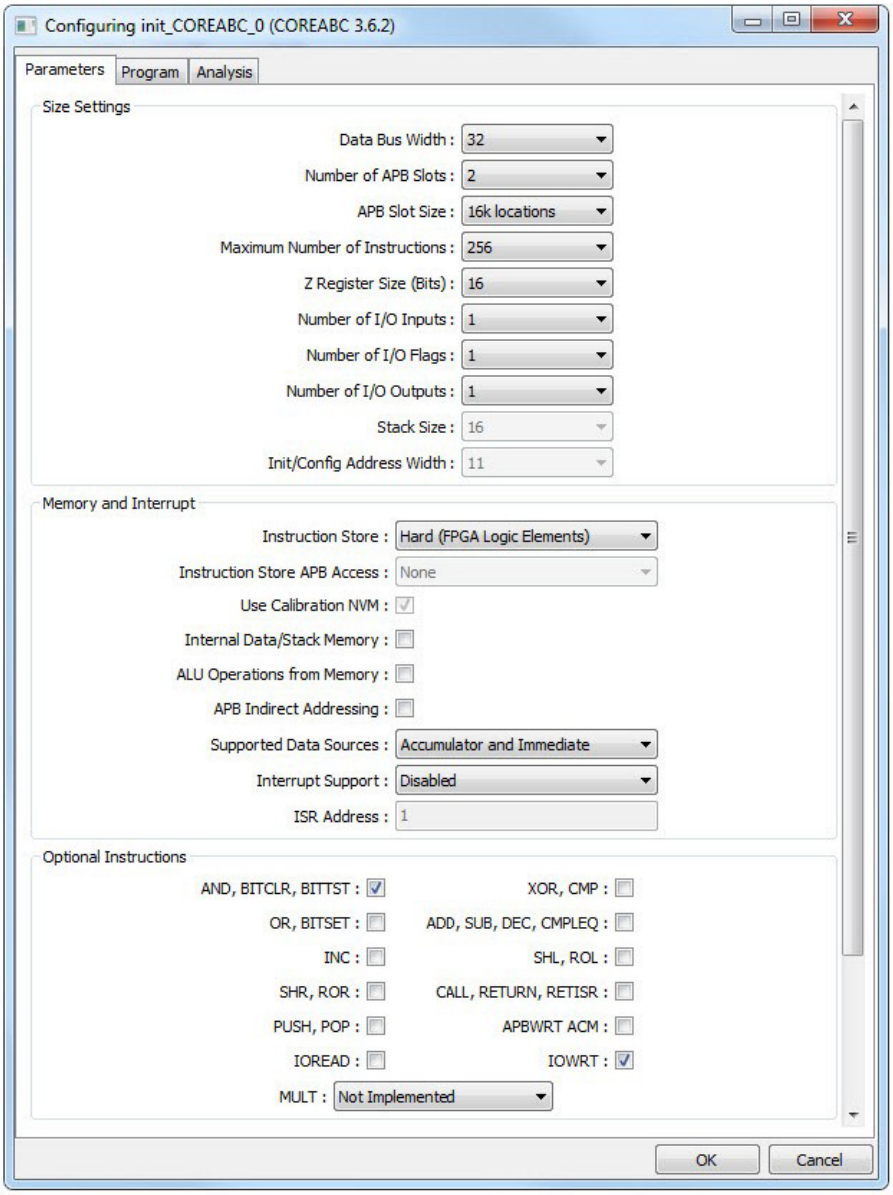


Figure 2-7. CoreABC Program Code for FDDR

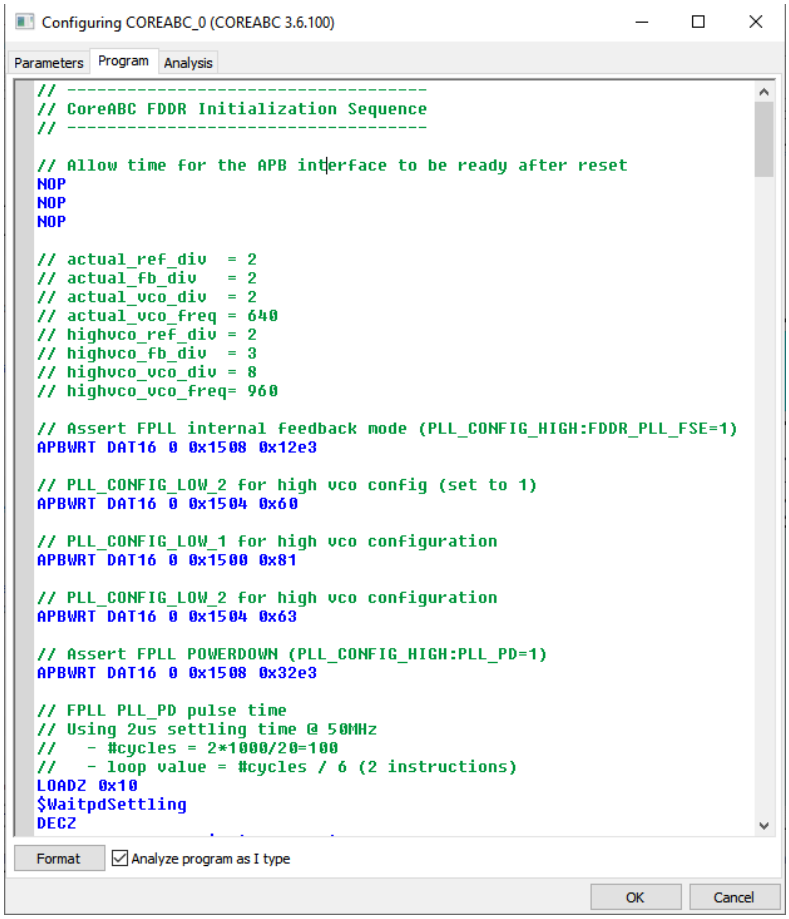
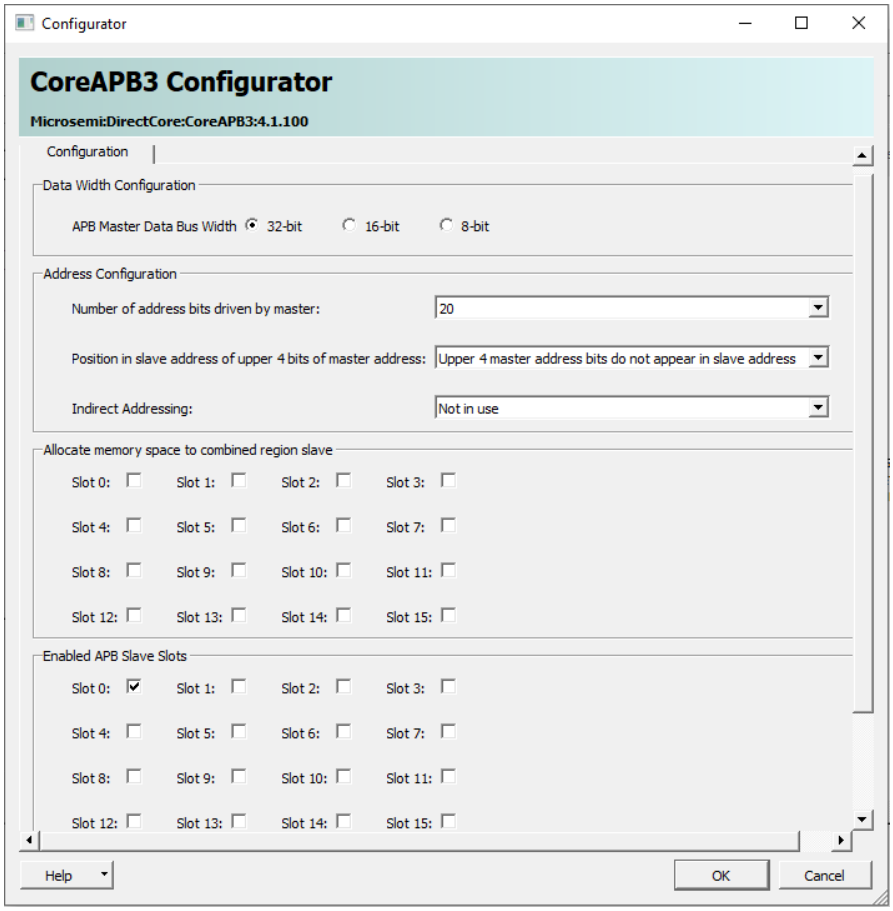


Figure 2-8. CoreAPB3 Configurator



2.4.3 DDR Memory Settling Time

The RTG4 DDR memory controller block is hard-coded with a DDR memory settling time of 200 µs, considering that the clock period of INIT_CLK is 20 ns (frequency 50 MHz). Microchip recommends that the initialization frequency be kept at 50 MHz.

The following figure shows the DDR Memory Settling Time at 200 µs.

Figure 2-9. DDR Memory Settling Time-200 µs

```
// Memory Settling time
// Using 200us settling time @ 50MHz
//    - #cycles = 200*1000/20=10000
//    - loop value = #cycles / 6 (2 instructions)
//    - loop value = 10000/6 = 0x682
LOADZ 0x682
$WaitSettling
```

Consult your DDR Memory vendor's datasheet for the correct memory settling time to use. An incorrect memory settling time may result in the failure of the DDR memory to initialize during operation.

If a different memory settling time is required for your DDR memory or you choose to use a different INIT_CLK frequency than the recommended 50 MHz, you must edit the program code in the Program tab of CoreABC to change the load value of the register used to compute the settling time. The following figure shows an example of the modified code to support DDR Memory settling time of 400 µs.

Figure 2-10. DDR Memory Settling Time-400 µs

```
// Memory Settling time
// Using 400us settling time @ 50MHz
//    - #cycles = 400*1000/20=20000
//    - loop value = #cycles / 6 (2 instructions)
//    - loop value = 20000/6 = 0xd05
LOADZ 0xd05
$WaitSettling
```

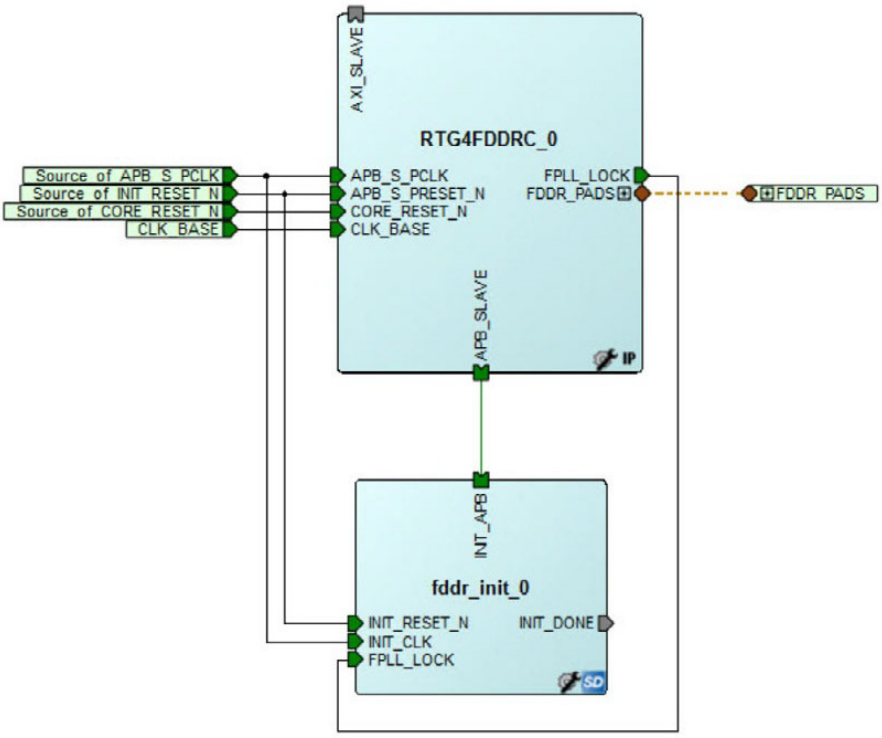
2.4.4 Interfacing FDDR with the Initialization Logic

1. Drag and drop the generated **FDDR** component from the **Design Hierarchy** window into the top level SmartDesign Canvas.
2. Drag and drop the **SmartDesign** component FDDR_INIT from the **Design Hierarchy** window into the same SmartDesign canvas where you have instantiated the FDDR core.
3. To interface the FDDR to the initialization logic block FDDR_INIT, make the necessary interconnections as shown in the following table.

Table 2-2. FDDR to FDDR_INIT Interconnections

From Port/BIF name/Block Name	To Port/BIF Name/Block Name
APB_SLAVE/FDDR	INIT_APB/FDDR_INIT
APB_S_PCLK/FDDR	INIT_CLK/FDDR_INIT
APB_S_PRESET_N/FDDR	INIT_RESET_N/FDDR_INIT
FPLL_LOCK/FDDR	FPLL_LOCK/FDDR_INIT
AXI_SLAVE/FDDR	Target (mirrored) BIF of AXI bus when the FDDR is configured as an AXI target
Connected to user Fabric Logic	INIT_DONE

Figure 2-11. FDDR Subsystem Initialization Circuitry



4. When completed, click the **Generate** button in SmartDesign to generate the FDDR subsystem. Configuration and initialization of your FDDR subsystem is complete.

3. Port Description

This section describes the ports of RTG4 DDR Memory Controller Configurator.

3.1 FDDR Core Ports

The following table lists the ports of FDDR Core.

Table 3-1. FDDR Core Ports

Port Name	Direction	Description
CORE_RESET_N	IN	FDDR Controller Reset
CLK_BASE	IN	FDDR Fabric Interface Clock
FPLL_LOCK	OUT	FDDR PLL Lock output High when FDDR PLL is locked.
CLK_BASE_PLL_LOCK	IN	Fabric PLL Lock Input This input is exposed only when the Use FAB_PLL_LOCK option is selected.

3.2 Interrupt Ports

The following table lists the group of ports that is exposed when you select the Enable interrupts option.

Table 3-2. Interrupt Ports

Port Name	Direction	Description
PLL_LOCK_INT	OUT	Asserts when FDDR PLL locks
PLL_LOCKLOST_INT	OUT	Asserts when FDDR PLL lock is lost
ECC_INT	OUT	Asserts when an ECC Event occurs
IO_CALIB_INT	OUT	Asserts when I/O calibration is complete
FIC_INT	OUT	Asserts when there is an error in the AHB/AXI protocol on the Fabric interface.

3.3 APB3 Configuration Interface

The following table lists the APB3 configuration interface ports signals.

Table 3-3. APB3 Configuration Interface

Port Name	Direction	Description
APB_S_PENABLE	IN	Target Enable
APB_S_PSEL	IN	Target Select
APB_S_PWRITE	IN	Write Enable
APB_S_PADDR[10:2]	IN	Address
APB_S_PWDATA[15:0]	IN	Write Data
APB_S_PREADY	OUT	Target Ready

.....continued		
Port Name	**Direction**	**Description**
APB_S_PSLVERR	OUT	Target Error
APB_S_PRDATA[15:0]	OUT	Read Data
APB_S_PRESET_N	IN	Target Reset
APB_S_PCLK	IN	Clock

3.4 DDR PHY Interface

These ports are exposed at the top level of the System Builder generated block.

Table 3-4. DDR PHY Interface

Port Name	Direction	Description
FDDR_CAS_N	OUT	Dram CASN
FDDR_CKE	OUT	Dram CKE
FDDR_CLK	OUT	Clock, P side
FDDR_CLK_N	OUT	Clock, N side
FDDR_CS_N	OUT	Dram CSN
FDDR_ODT	OUT	Dram ODT
FDDR_RAS_N	OUT	Dram RASN
FDDR_RESET_N	OUT	Dram reset for DDR3
FDDR_WE_N	OUT	Dram WEN
FDDR_ADDR[15:0]	OUT	Dram address bits
FDDR_BA[2:0]	OUT	Dram bank address
FDDR_DM_RDQS[4:0]	INOUT	Dram data mask
FDDR_DQS[4:0]	INOUT	Dram data strobe Input/Output-P side
FDDR_DQS_N[4:0]	INOUT	Dram data strobe Input/Output-N side
FDDR_DQ[35:0]	INOUT	Dram data Input/Output
FDDR_FIFO_WE_IN[2:0]	IN	FIFO in signal
FDDR_FIFO_WE_OUT[2:0]	OUT	FIFO out signal
FDDR_DM_RDQS ([3:0]/[1:0]/[0])	INOUT	Dram data mask
FDDR_DQS ([3:0]/[1:0]/[0])	INOUT	Dram data strobe Input/Output-P Side
FDDR_DQS_N ([3:0]/[1:0]/[0])	INOUT	Dram data strobe Input/Output-N Side
FDDR_DQ ([31:0]/[15:0]/[7:0])	INOUT	Dram data Input/Output
FDDR_DQS_TMATCH_0_IN	IN	FIFO in signal
FDDR_DQS_TMATCH_0_OUT	OUT	FIFO out signal

.....continued		
Port Name	**Direction**	**Description**
FDDR_DQS_TMATCH_1_IN	IN	FIFO in signal (32-bit only)
FDDR_DQS_TMATCH_1_OUT	OUT	FIFO out signal (32-bit only)
FDDR_DM_RDQS_ECC	INOUT	Dram ECC data mask
FDDR_DQS_ECC	INOUT	Dram ECC data strobe Input/Output-P side
FDDR_DQS_ECC_N	INOUT	Dram ECC Data Strobe Input/Output-N side
FDDR_DQ_ECC ([3:0]/[1:0]/[0])	INOUT	Dram ECC data Input/Output
FDDR_DQS_TMATCH_ECC_IN	IN	ECC FIFO in signal
FDDR_DQS_TMATCH_ECC_OUT	OUT	ECC FIFO out signal (32-bit only)

Important: Port widths for some ports change, depending on the selection of the PHY width. The notation **[a:0]/ [b:0]/[c:0]** is used to denote such ports, where:

- **[a:0]** refers to the port width when a 32-bit PHY width is selected
- **[b:0]** corresponds to a 16-bit PHY width, and
- **[c:0]** corresponds to an 8-bit PHY width.

3.5 AXI Bus Interface

The following table lists the ports of the AXI Bus interface.

Table 3-5. AXI Bus Interface

Port Name	Direction	Description
AXI_S_AWREADY	OUT	Write address ready
AXI_S_WREADY	OUT	Write address ready
AXI_S_BID[3:0]	OUT	Response ID
AXI_S_BRESP[1:0]	OUT	Write response
AXI_S_BVALID	OUT	Write response valid
AXI_S_ARREADY	OUT	Read address ready
AXI_S_RID[3:0]	OUT	Read ID Tag
AXI_S_RRESP[1:0]	OUT	Read response
AXI_S_RDATA[63:0]	OUT	Read data
AXI_S_RLAST	OUT	Read last This signal indicates the last transfer in a read burst.
AXI_S_RVALID	OUT	Read address valid
AXI_S_AWID[3:0]	IN	Write address ID
AXI_S_AWADDR[31:0]	IN	Write address
AXI_S_AWLEN[3:0]	IN	Burst length

.....continued		
Port Name	**Direction**	**Description**
AXI_S_AWSIZE[1:0]	IN	Burst size
AXI_S_AWBURST[1:0]	IN	Burst type
AXI_S_AWLOCK[1:0]	IN	Lock type This signal provides additional information about the atomic characteristics of the transfer.
AXI_S_AWVALID	IN	Write address valid
AXI_S_WID[3:0]	IN	Write data ID tag
AXI_S_WDATA[63:0]	IN	Write data
AXI_S_WSTRB[7:0]	IN	Write strobes
AXI_S_WLAST	IN	Write last
AXI_S_WVALID	IN	Write valid
AXI_S_BREADY	IN	Write ready
AXI_S_ARID[3:0]	IN	Read address ID
AXI_S_ARADDR[31:0]	IN	Read address
AXI_S_ARLEN[3:0]	IN	Burst length
AXI_S_ARSIZE[1:0]	IN	Burst size
AXI_S_ARBURST[1:0]	IN	Burst type
AXI_S_ARLOCK[1:0]	IN	Lock type
AXI_S_ARVALID	IN	Read address valid
AXI_S_RREADY	IN	Read address ready
AXI_S_CORE_RESET_N	IN	FDDR global reset

3.6 AHB0 Bus Interface

The following table lists the AHB0 Bus interface ports signals.

Table 3-6. AHB0 Bus Interface

Port Name	Direction	Description
AHB0_S_HREADYOUT	OUT	AHBL target ready When high for a write indicates that the target is ready to accept data, and high for a read indicates that data is valid.
AHB0_S_HRESP	OUT	AHBL response status When driven high at the end of a transaction indicates that the transaction has completed with errors. Low at the end of a transaction indicates that the transaction has completed successfully.
AHB0_S_HRDATA[31:0]	OUT	AHBL read data Read data from the target to the initiator.

.....continued		
Port Name	**Direction**	**Description**
AHB0_S_HSEL	IN	AHBL target select When asserted, the target is the currently selected AHBL target on the AHB bus.
AHB0_S_HADDR[31:0]	IN	AHBL address Byte address on the AHBL interface.
AHB0_S_HBURST[2:0]	IN	AHBL burst length
AHB0_S_HSIZE[1:0]	IN	AHBL transfer size Indicates the size of the current transfer (8/16/32 byte transactions only).
AHB0_S_HTRANS[1:0]	IN	AHBL transfer type Indicates the transfer type of the current transaction.
AHB0_S_HMASTLOCK	IN	AHBL lock When asserted the current transfer is part of a locked transaction.
AHB0_S_HWRITE	IN	AHBL write When high indicates that the current transaction is a write and low indicates that the current transaction is a read.
AHB0_S_HREADY	IN	AHBL ready When high, indicates that the target is ready to accept a new transaction.
AHB0_S_HWDATA[31:0]	IN	AHBL write data Write data from the initiator to the target.

3.7 AHB1 Bus Interface

The following table lists the AHB1 Bus interface port signals.

Table 3-7. AHB1 Bus Interface

Port Name	Direction	Description
AHB1_S_HREADYOUT	OUT	AHBL target ready When high for a write indicates the target is ready to accept data and when high for a read indicates that data is valid.
AHB1_S_HRESP	OUT	AHBL response status When driven high at the end of a transaction indicates that the transaction has completed with errors. When driven low at the end of a transaction indicates that the transaction has completed successfully.
AHB1_S_HRDATA[31:0]	OUT	AHBL read data Read data from the target to the initiator.
AHB1_S_HSEL	IN	AHBL target select When asserted, the target is the currently selected AHBL target on the AHB bus.
AHB1_S_HADDR[31:0]	IN	AHBL address Byte address on the AHBL interface.

.....continued

Port Name	Direction	Description
AHB1_S_HBURST[2:0]	IN	AHBL burst length
AHB1_S_HSIZE[1:0]	IN	AHBL transfer size Indicates the size of the current transfer (8/16/32 byte transactions only).
AHB1_S_HTRANS[1:0]	IN	AHBL transfer type Indicates the transfer type of the current transaction.
AHB1_S_HMASTLOCK	IN	AHBL lock When asserted the current transfer is part of a locked transaction.
AHB1_S_HWRITE	IN	AHBL write When high indicates that the current transaction is a write. When low indicates that the current transaction is a read.
AHB1_S_HREADY	IN	AHBL ready When high, indicates that the target is ready to accept a new transaction.
AHB1_S_HWDATA[31:0]	IN	AHBL write data Write data from the initiator to the target.

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	12/2022	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template. • The document number was updated to DS50003453 from 50200589. • Updated the following screenshots: Figure 2-1 and Figure 2-2 in section 2.1.1. Fabric DDR Registers Configuration.

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