Improving the Performance of your DC-DC Forward Converter using I^2MOS™ MOSFET Technology

Microsemi Space Forum 2015

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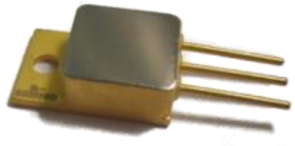
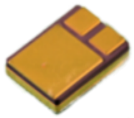
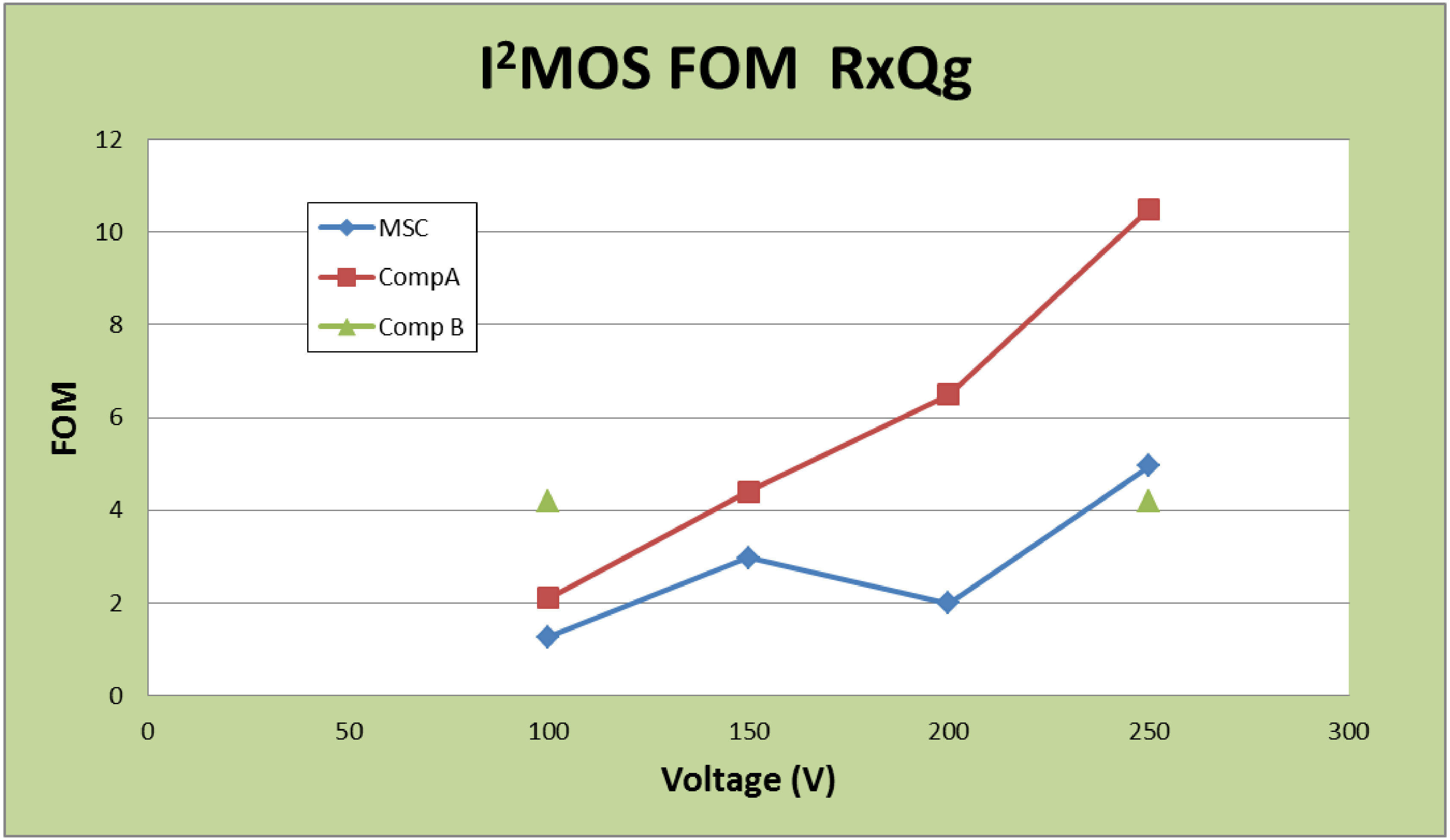
I^2MOS advantages

- Highest available SEE performance, 85- 90 MeV at full rated BVDss
- Highest Avalanche capability: 5X greater than competition
- TID (Total Ionizing Dose) Rating: 100Krad- 500Krad (depending on specific device)
- Commerce Rating: 9A515.e
  - Most Euro countries will not need a license!
- Competitive pricing on new designs

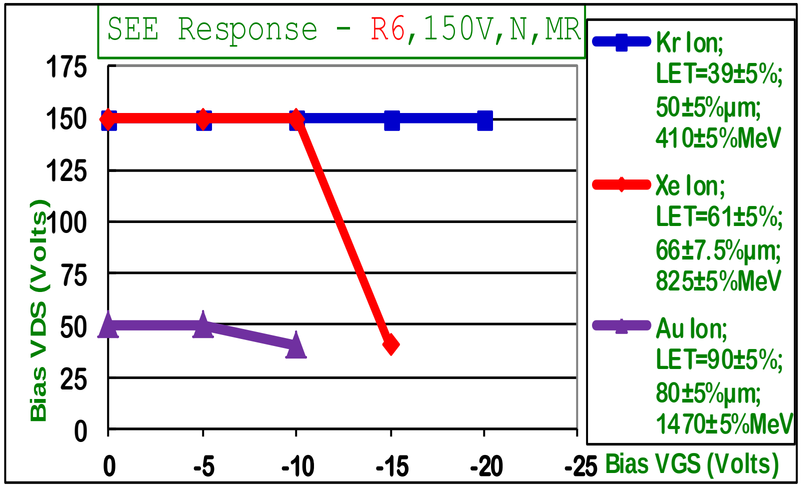


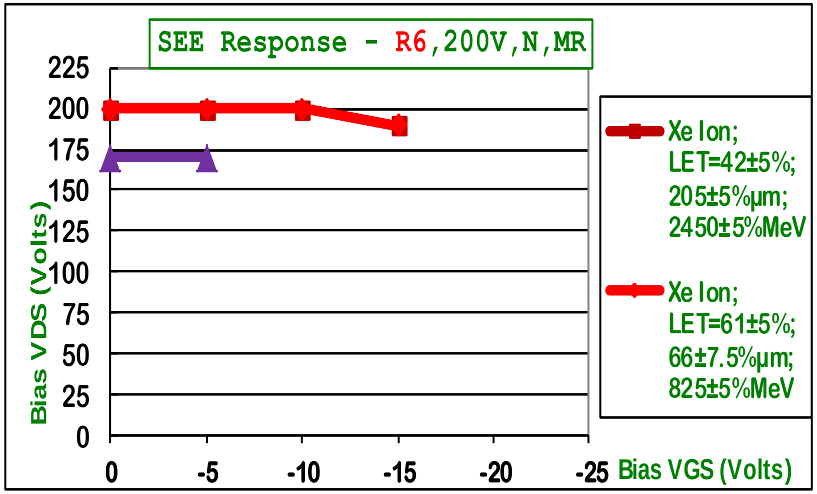


I²MOS FOM versus Competition

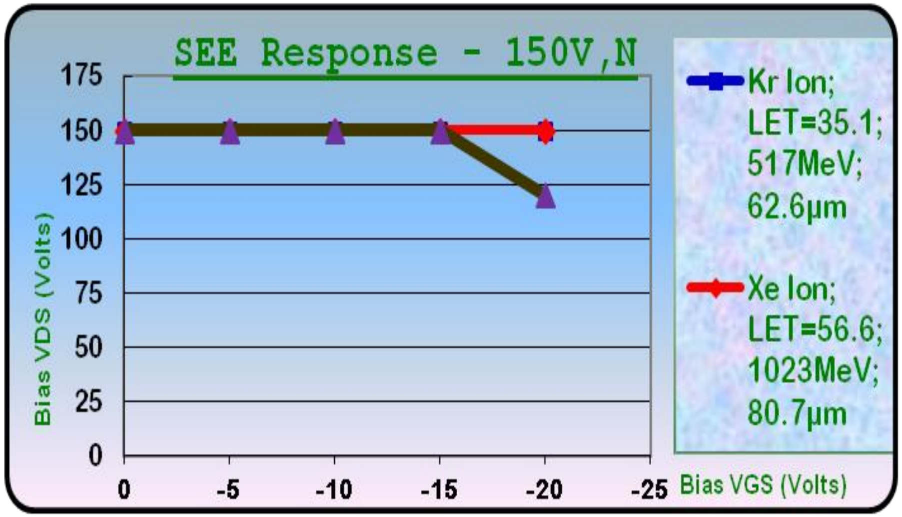


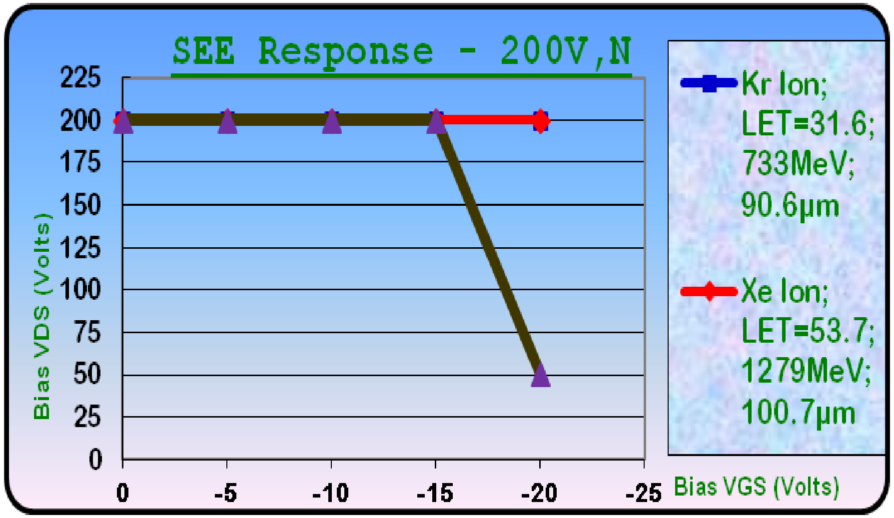
SEE results- Microsemi vs. Competitor





IR (R6)





Microsemi (I^2MOS)

I²MOS™ MOS P/N Structure

MRH	BVDSS/10 (V)	Channel	ID @ 25C (A)	Package	Screening	RAD LEVEL
MRH	20	N	22	U3	S	R
Microsemi	20= 200V	N		U3= SMD0.5	S= JANS	R= 100K F= 300K
Rad- Hard	10= 100V	P		T2= TO- 39	V= JANTXV	G= 500K
MOSFET	13= 130V			T3= TO- 257	C= EDU	
	06= 60V			U5= LCC-18		
	03= 30V			C= die		

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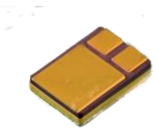
I²MOS™ Planned Products

Phase 1: I²MOS™ portfolio, N- Ch, Sz 3

Bvdss (V)	Similar JEDEC Number	Industry Equivalent	MSC p/n
150	2N7589U3	IRHNJ67134	MRH15N19U3
200	2N7591U3	IRHNJ67230	MRH20N16U3
250	2N7593U3	IRHNJ67234	MRH25N15U3

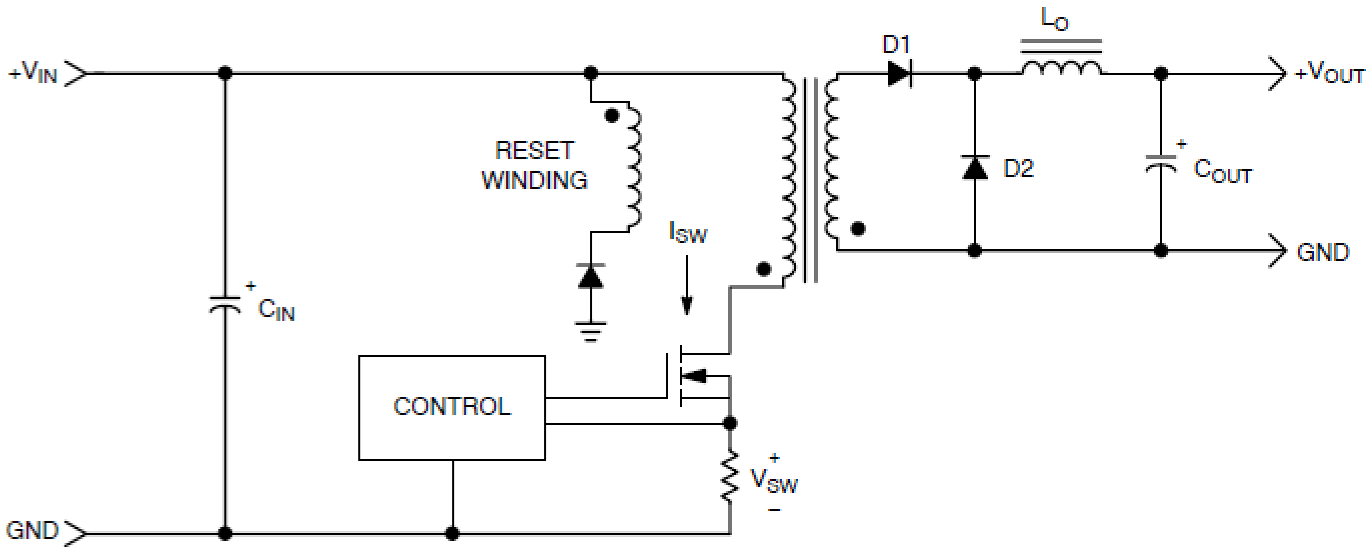


SMD0.5

Phase 2: I²MOS™ portfolio, N- Ch, Sz 5.5

Bvdss (V)	Similar JEDEC Number	Industry Equivalent	RH2 Base MSC p/n	Package
150	2N7582T1	IRHMS67164	MRH15N45T1	TO-254
150	2N7581U2	IRHNA67164	MRH15N56U1	SMD-2
200	2N7584T1	IRHMS67260	MRH20N45T1	TO-254
200	2N7583U2	IRHNA67260	MRH20N56U1	SMD-2
250	2N7586T1	IRHMS67264	MRH25N45T1	TO-254
250	2N7585U2	IRHNA67264	MRH25N56U1	SMD-2

TO-254



Efficiency Performance of I²MOS

DC-DC Forward Converter (Resonant Reset Topology)
MRH25N15U3 vs. IRHNJ67234

DC-DC Criteria

- Create a Circuit to Reveal Differences in MOSFET Power Losses
- Parallel-Inductor Isolated Forward DC-DC Converter
- Improved Efficiency
  - Resonant Transformer Reset
  - Lower DC Losses in Inductors and Schottky Rectifiers
- Use Vdd = 50Vdc
  - Peak of Resonant Reset Voltage Will Be: $V_{dd} + (I_d(pk) * L_m / C_r)$
    - L_m is Power Transformer Magnetizing Inductance (~120uH)
    - C_r is the Resonance Capacitance = $C_{oss} \,||\, C_j (N_s/N_p) *$ (~810pF)
    - Worst Case Resonance Peak at f_{sw} = 350kHz and V_{out} = 5.0Vdc (~120Vpk)

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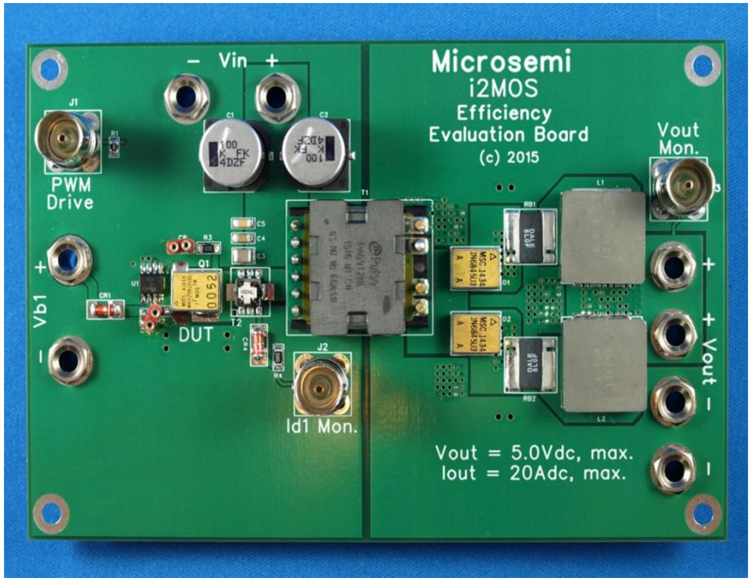
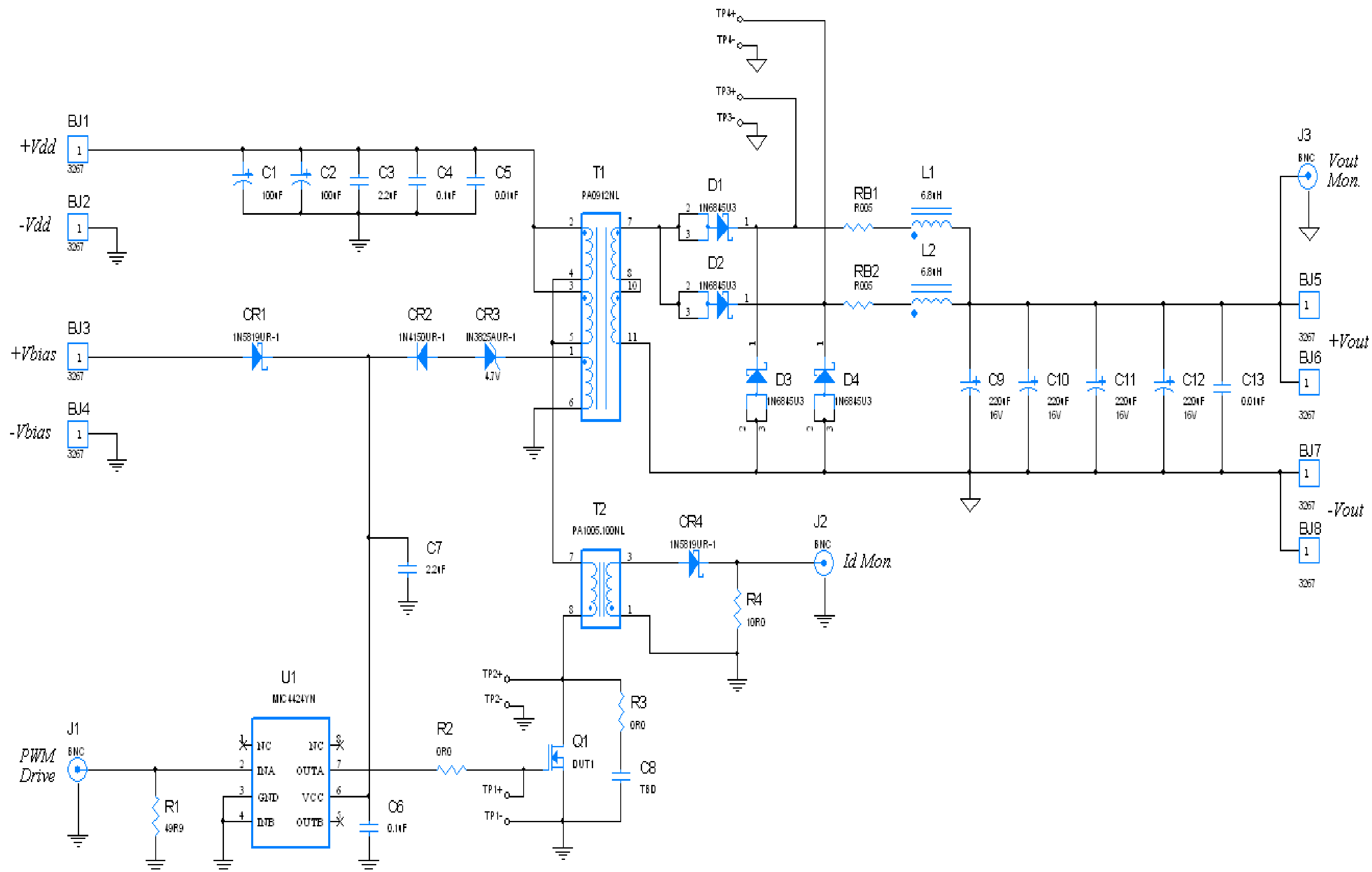
Efficiency Test Criteria

- Voltage De- Rating= 50%
  - Use Microsemi MRH25N15U3 and IR IRHNJ67234, 250V devices.

  (200V Device May Be Used For Higher Efficiency With Lower Voltage Margin.)
- 100W Maximum Output Power
  - 20A Maximum Output Current
    - 66W For Vout = 3.3Vdc
    - 100W For Vout = 5.0Vdc



Efficiency Test Circuit Schematic



Efficiency Test Circuit Features

- Circuit Used For Power Switch Efficiency Comparison:
  - Circuit Uses U3 Packages For All Power Functions
    - Small Size
    - Ease of Thermal Management
  - Output Uses Paralleled Output Stage For Increased Efficiency
    - Schottkies and Inductors Share Current ~50:50
      - DC Power Losses Reduced by ~1/4 - 1/3!
  - Optimized for 3.3Vdc < V_{out} < 5Vdc
  - Optimized For 1A < I_{out} < 20A
  - Optimized For 350kHz < f_{sw} < 500kHz
  - Uses COTS Micrel MIC4424 Gate Driver IC
    - Rad-Hard Equivalents Available from Intersil

Efficiency Test Parameters

- DC Output (V_{out}) Set By Varying Input Duty Cycle
  - Duty Cycle = Desired $V_{out} * (N_s/N_p) / V_{dd}$
- Efficiency:

$$\eta = P_{out} / (P_{in} + P_{bias}) = (V_{out} * I_{out}) / ((V_{dd} * I_{dd}) + (V_{bias} * I_{bias}))$$

I_{out} = Set, Varied from 1A to 20A

V_{dd} = Set, Constant = 50Vdc

V_{bias} = Set, Constant = 12Vdc

V_{out} is Set By Varying the Input Duty Cycle

I_{dd} and I_{bias} Are Measured at Each Operating Point

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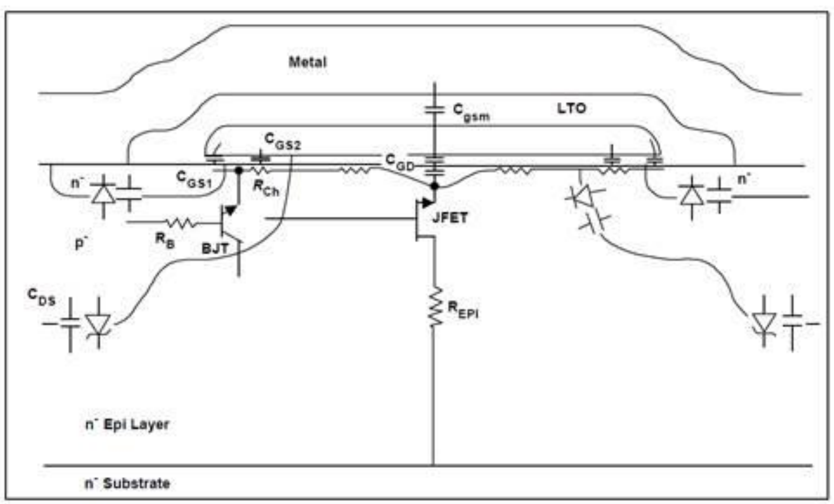
MOSFET Losses

- Key Contributors to Power MOSFET Switch Losses:
  - DC Losses: $I_d(rms)^2 * R_{ds}(on) * D$
  - AC Losses: Gate + Switching
    - Gate Input Losses: $Q_{gt} * V_{bias} * f_{sw}$
    - Drain Switching Losses: $\sim V_{dd} * I_d(rms) * (t_r + t_f) * fsw / 2) + (C_{oss} * V_{dd}^2 * f_{sw})$



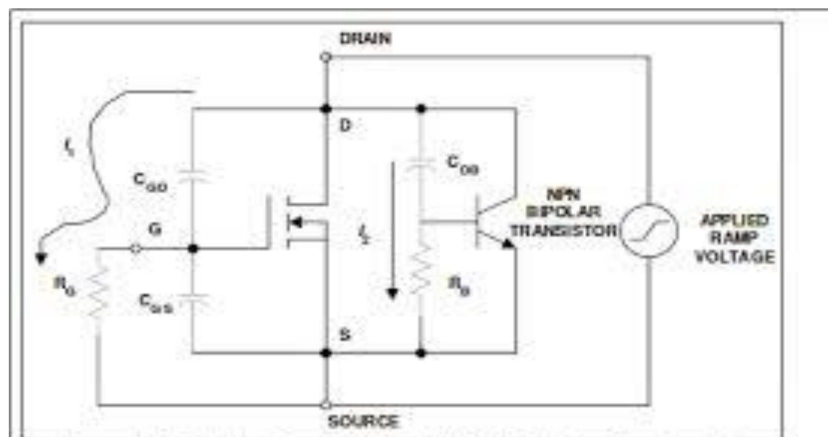
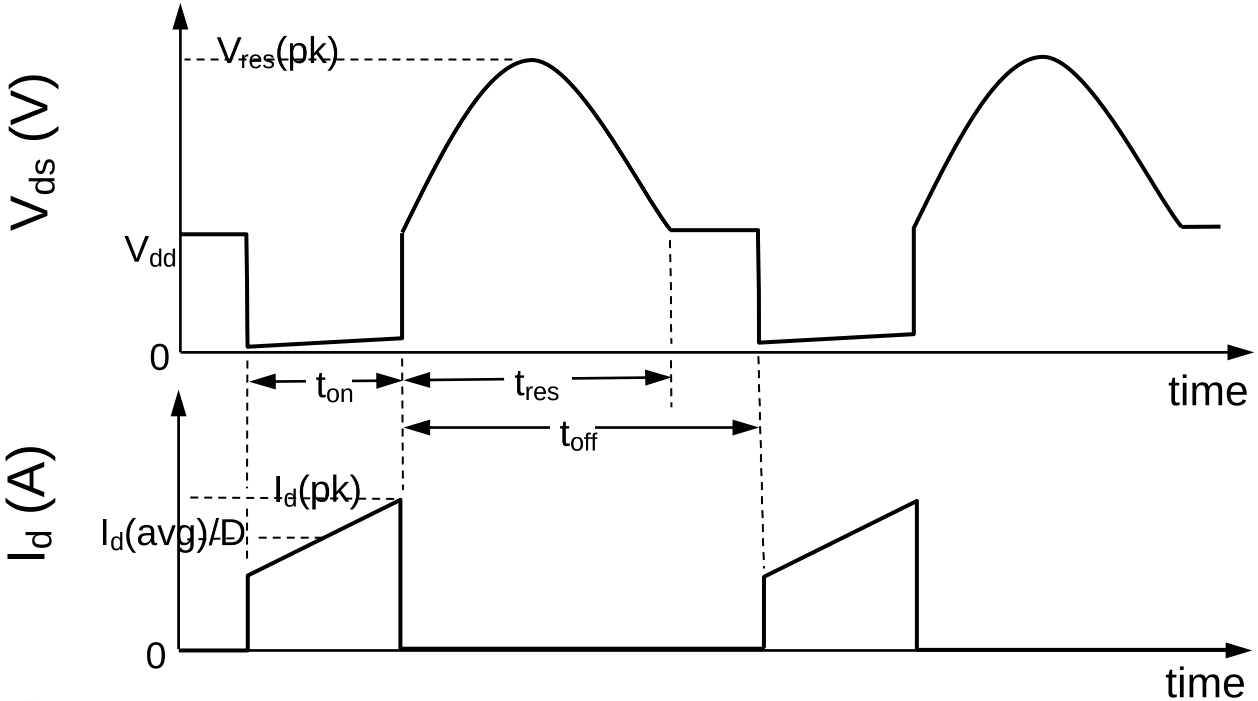


Figure 14. Equivalent Circuit of Power MOSFET Showing Two Possible Mechanisms for dv/dt Induced Turn-on.

Forward Converter Design Parameters

- Duty Cycle = D = $(V_{out} / V_{in}) * (N_s / N_p) = t_{on} / t_{off}$
- $I_d(pk) = (I_d(avg) / D) + (0.5 * (V_{dd} * t_{on}) / L_m)$
- $V_{res}(pk) = V_{dd}$ □+ $I_d(pk) * (L_m / C_r)^{0.5}$
- $t_{res} = \pi * (L_m * C_r)^{0.5}$
- $C_r = C_{oss} + (C_j / (N_p/N_s))$
  - C_j is the Output Schottky Junction Capacitance



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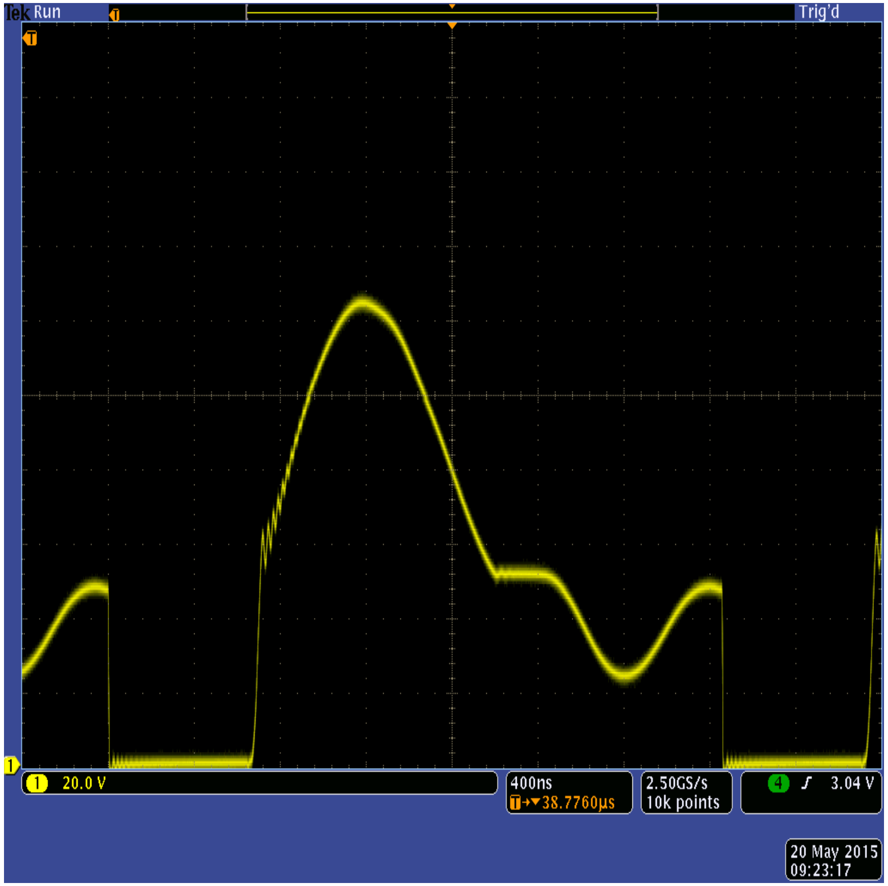
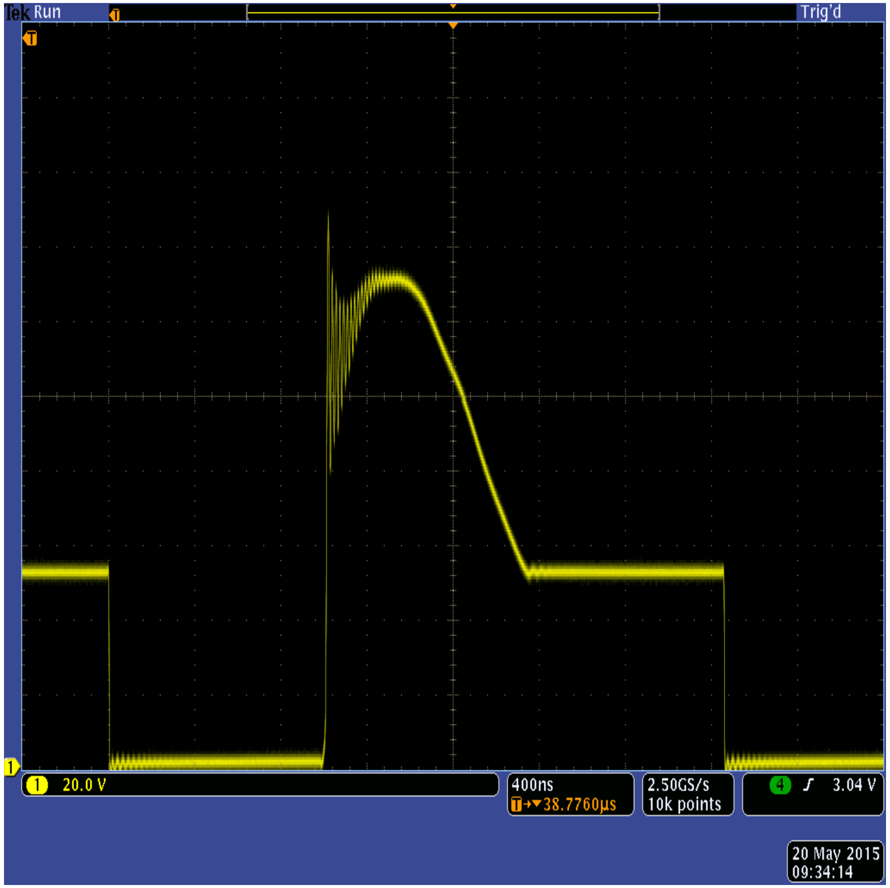
Measured Drain-Source Voltages

V_{out} = 5.0Vdc, I_{out} = 1Adc, f_{sw} = 350kHz



$V_{DS}(pk)$ = 122V

V_{out} = 5.0Vdc, I_{out} = 20Adc, f_{sw} = 350kHz



$V_{DS}(pk)$ = 148V

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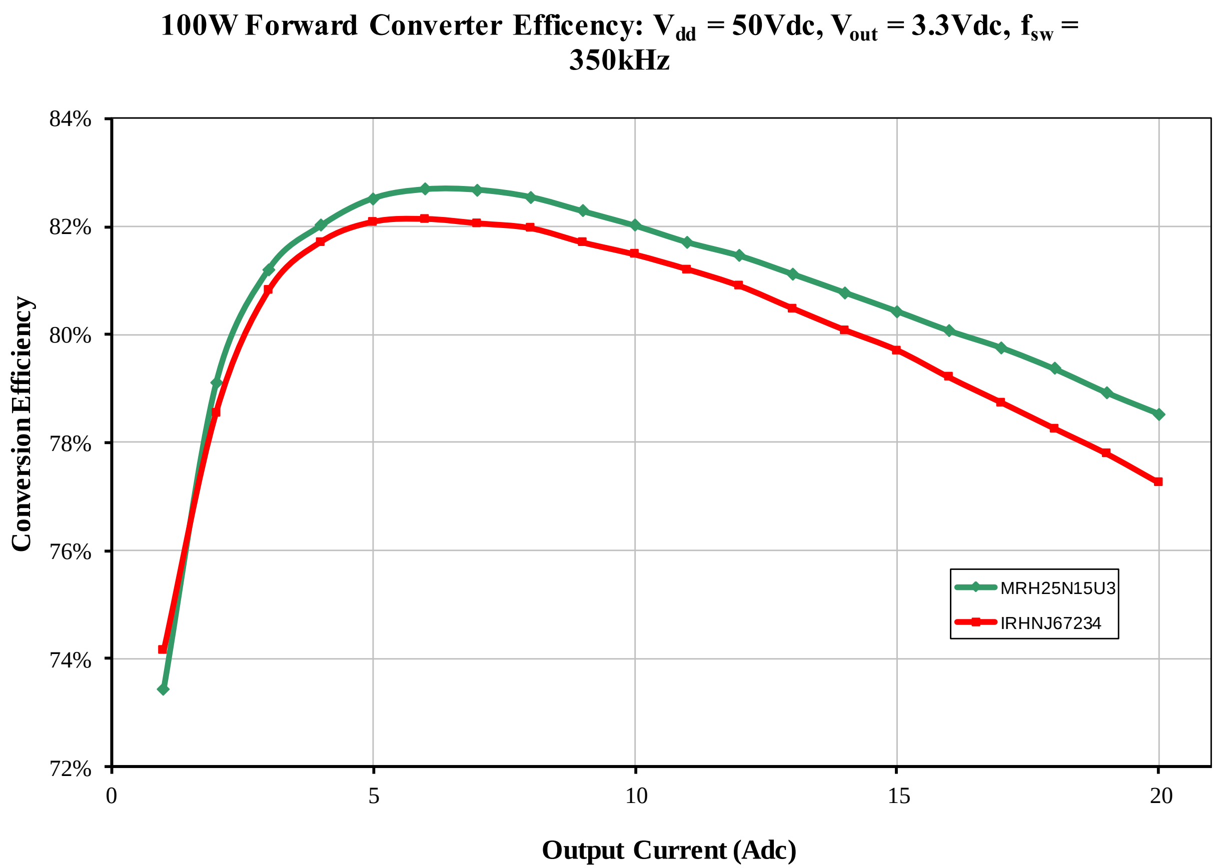
Efficiency Parameters

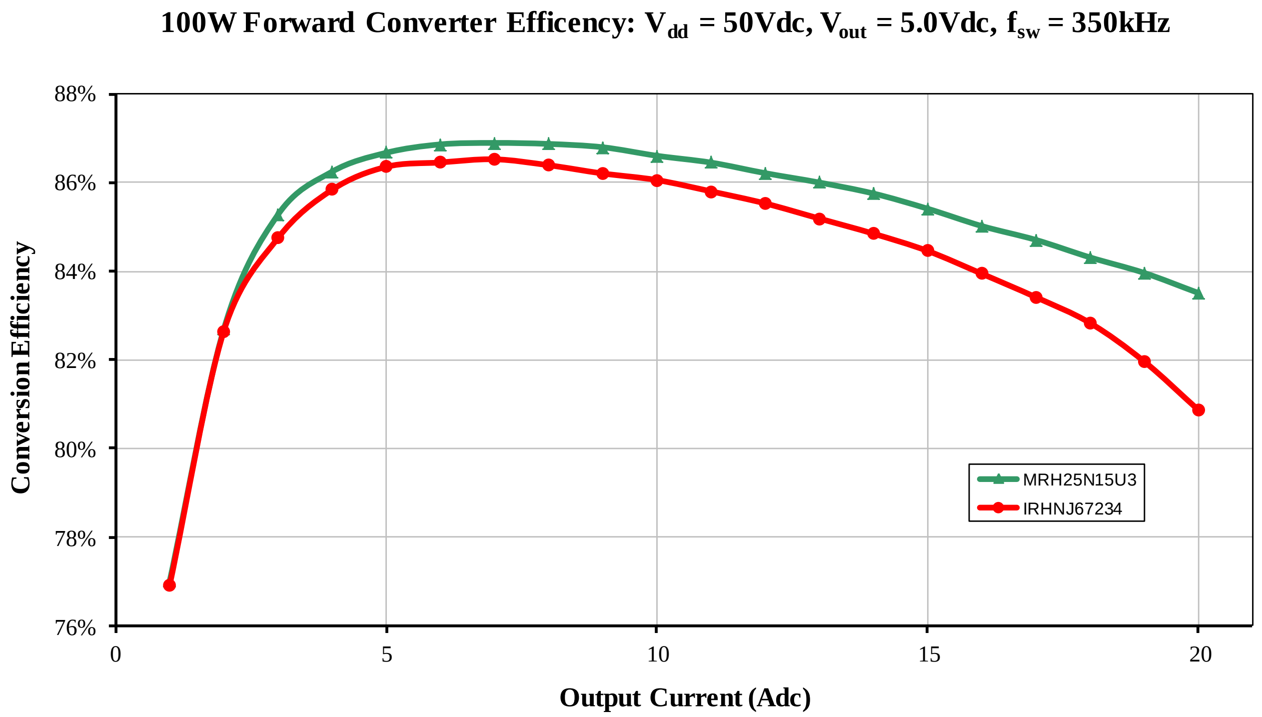
- From Data Sheet Parameters:
  - R_{ds}(ON)
    - MRH25N15U3 – 175mΩ max.
    - IRHNJ67234 – 210mΩ max.
    - IR Device **20% Higher** Than Microsemi
  - Q_{gt}
    - MRH25N15U3 – 32nC typ. (est. 40nC max.)
    - IRHNJ67234 – 50nC max. (est. 40nC typ.)
  - Coss
    - MRH25N15U3 – 275pF typ.
    - IRHNJ67234 – 187pF typ.

Efficiency Data- +3.3Vout, 350 Khz.



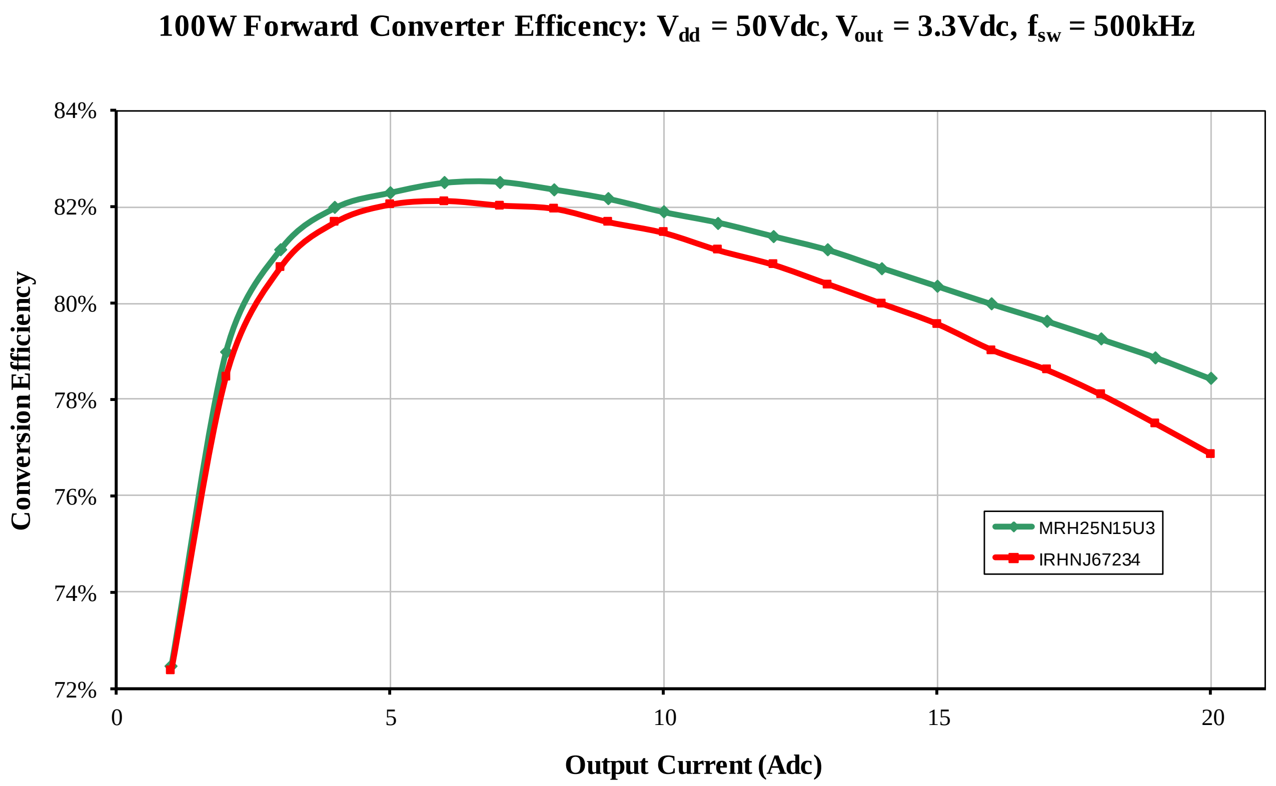
- At higher currents the improvement in conduction losses provide an advantage.

Efficiency Data, Vout = 5.0V, 350 Khz.



➢ **At higher currents the improvement in conduction losses is slightly better at 5.0Vout vs. 3.3Vout.**

Efficiency Data, +3.3Vout, 500 Khz.



- At 500 Khz. There are more switching losses in both parts but I²MOS part maintains the advantage.

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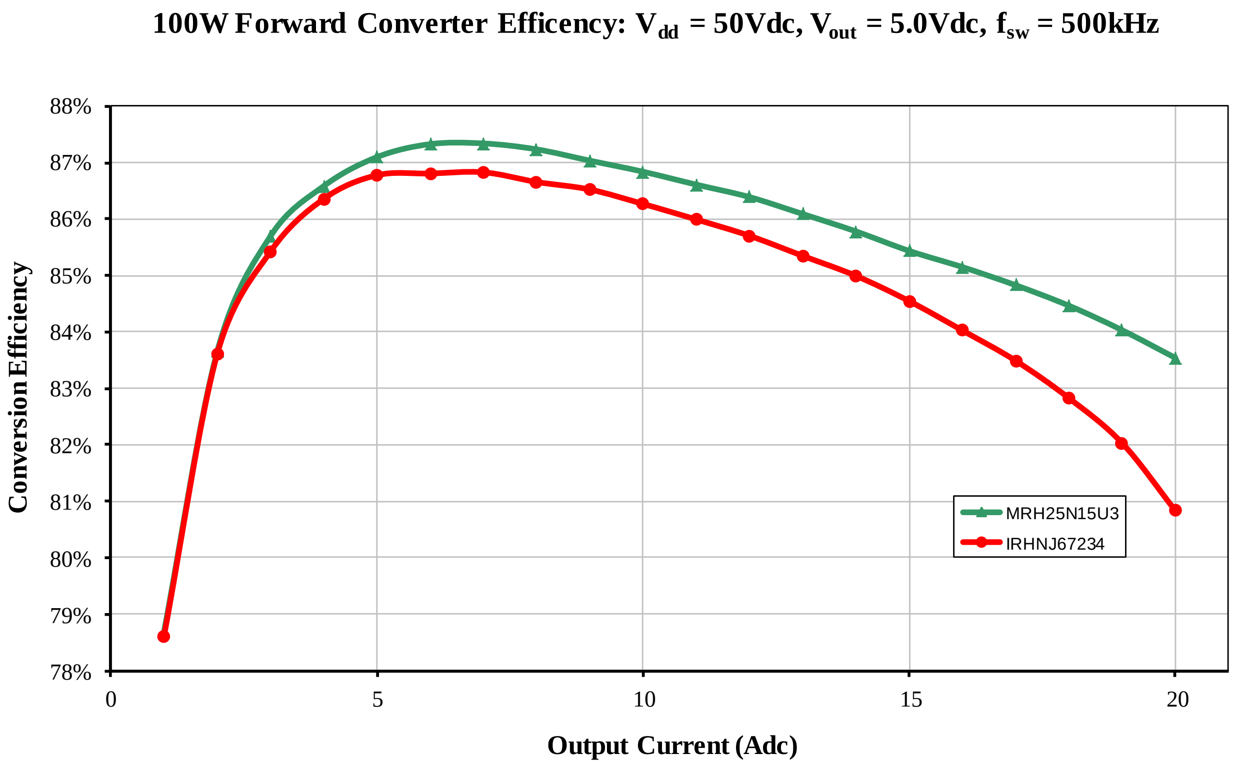
Efficiency Data, 5.0Vout, 500 Khz.



➢ **Efficiency improvements @ higher currents when Vout = 5.0V**

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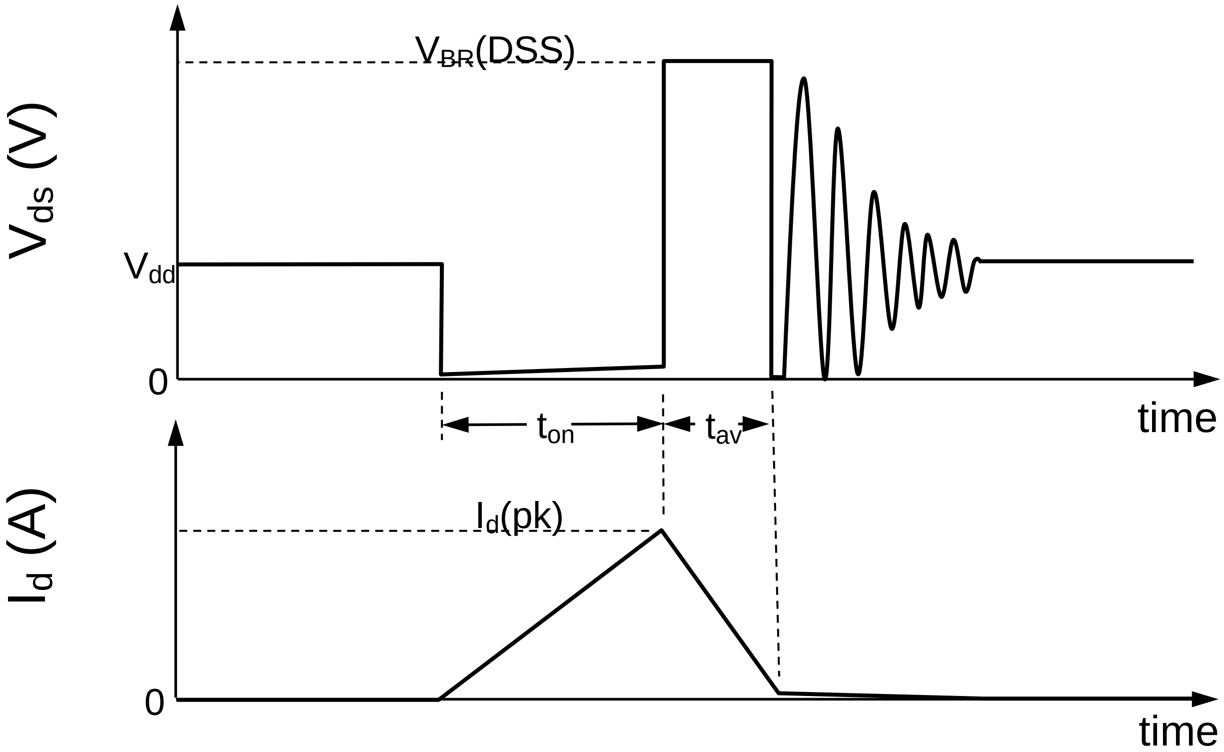


Avalanche Energy Performance

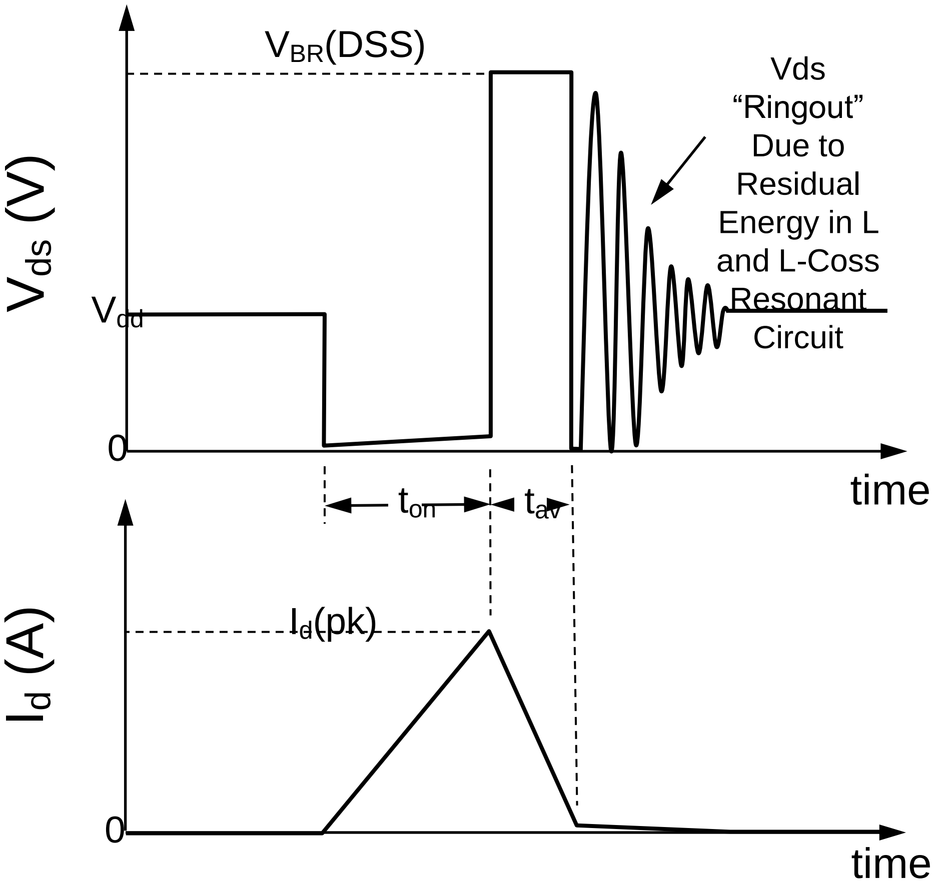
MRH25N15U3 vs. IRHNJ67234

Avalanche Basics

- Avalanche Performance Indicates Ruggedness of MOSFET
  - Energy Handling Capability
    - Repetitive
    - Single Pulse
    - Specified in Joules (V * I * t)

- "Unconstrained" Inductors Cause Excursions to $V_{BR}(DSS)$
  - Energy ~ $(L * I_d(pk)^2 / 2) * (1 – (V_{dd} / V_{BR}(DSS))$
  - Junction Dissipates Enormous Instantaneous Power
    - If $V_{BR}(DSS) = 250V$ and $I_d(pk) = 10A$, $P_{inst} = 2500W$!

- **The Greater the Avalanche Energy Rating, The Better**



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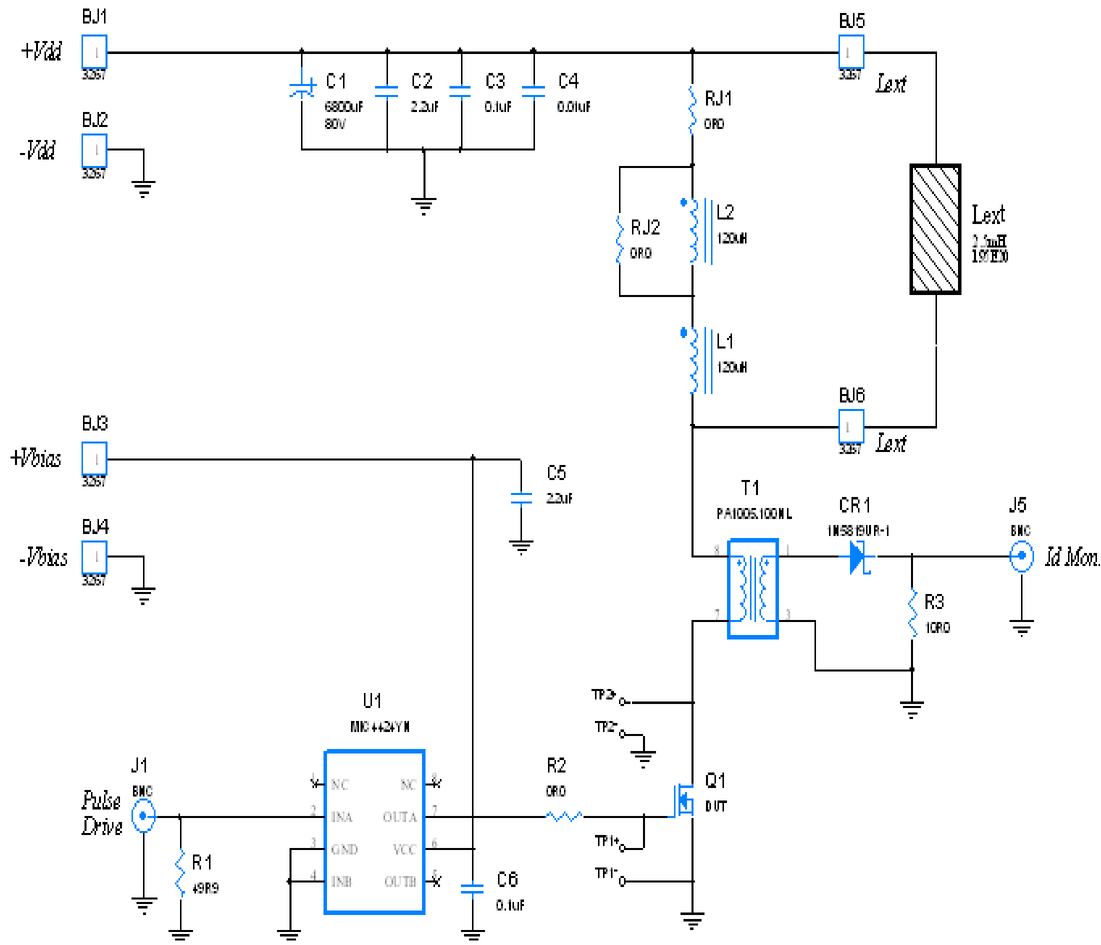
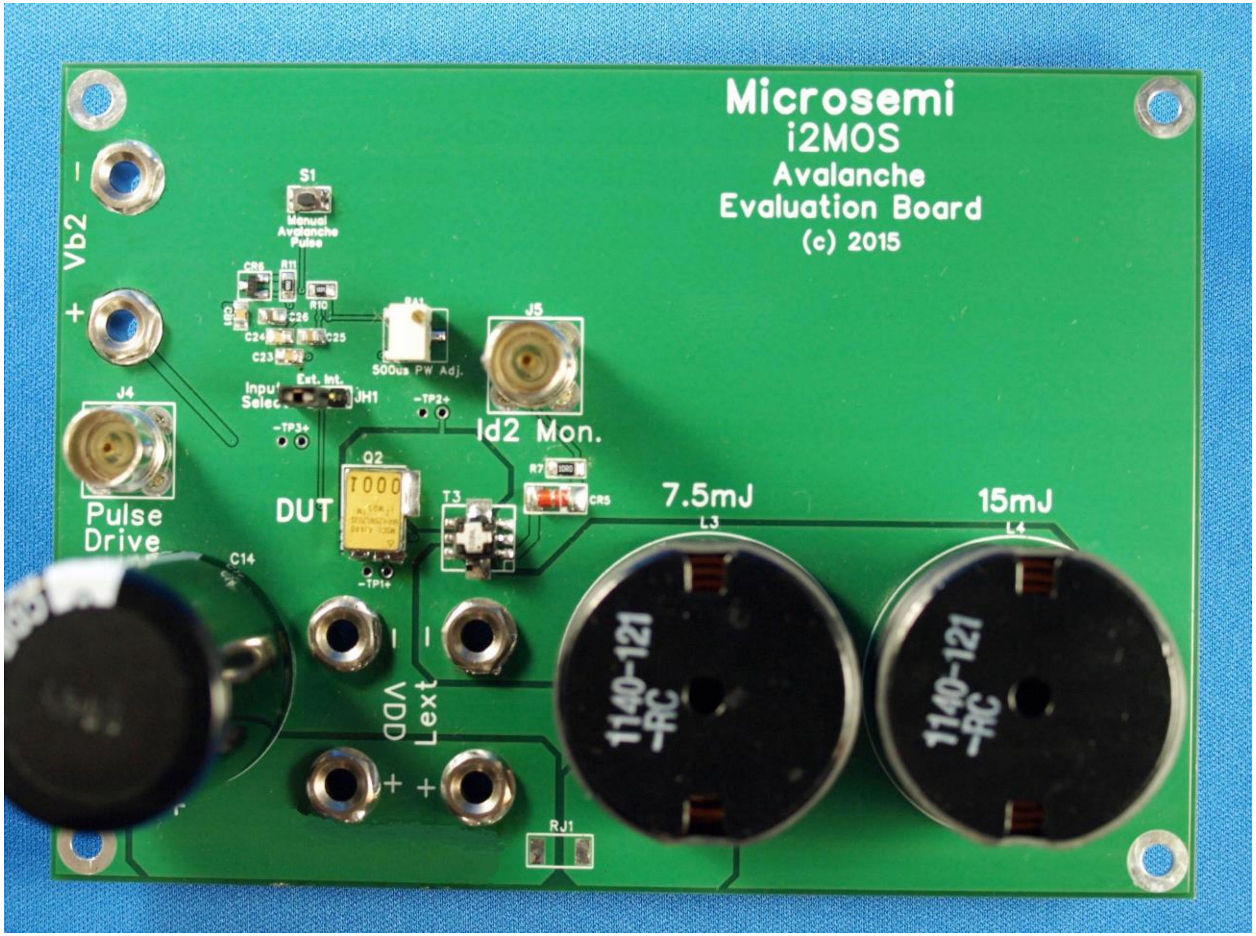
Data sheet Specs & Avalanche Test Circuit

Part #	Eas	Ear
MRH25N15U3	15 mJ	300 mJ
IRHNJ67234	7.5 mJ	56 mJ



Avalanche Test PCB



Board Size = 5.8 x 4.1 x 0.063", 4 Layer FR-4, Double Sided

Avalanche Test Procedure

Avalanche Test Has Two Regions:

1. Turn ON Device Under Test (DUT)

   Ramp Inductor Current to Desired I_d(pk) during ON Time (t_{on})

   $I_d(pk) = V_{dd} * t_{on} / L$

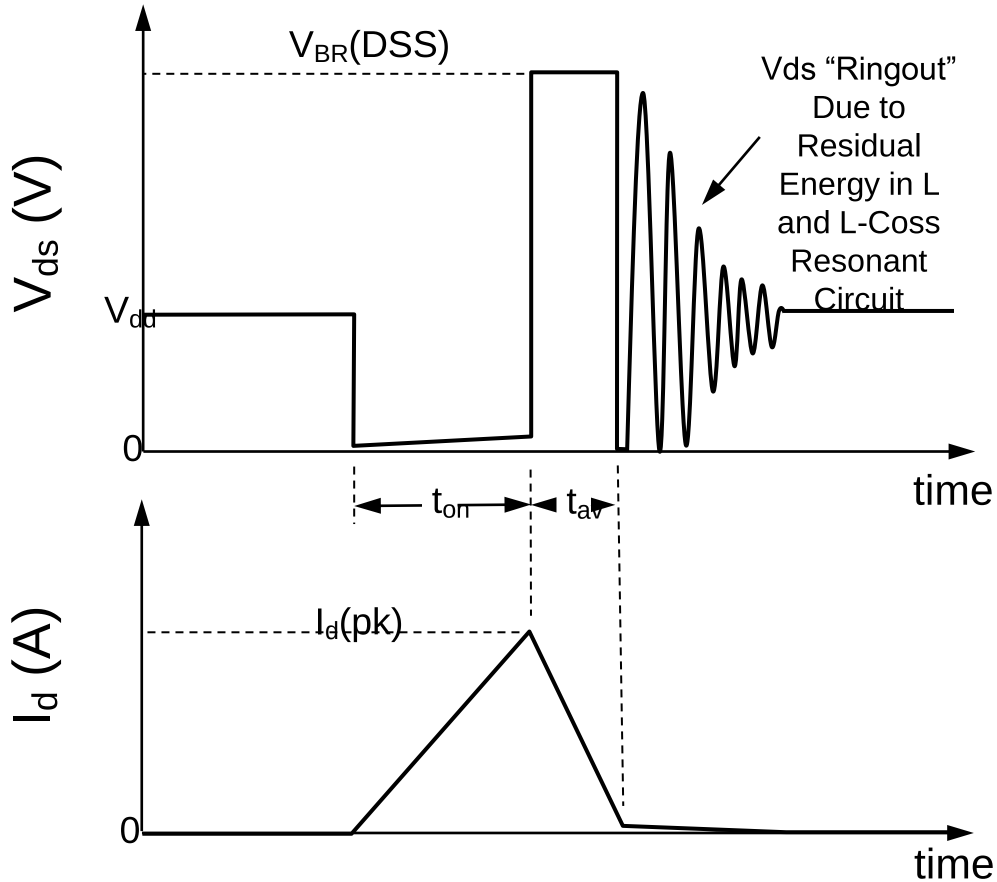
2. Turn OFF DUT

   Drain Voltage "Flys" to VBR(DSS)

   Avalanche Time (t_{av}) = $L * I_d(pk) / (V_{BR}(DSS) – V_{dd})$

   Avalanche Energy (Eav) = $V_{BR}(DSS) * I_d(pk) * t_{av}$

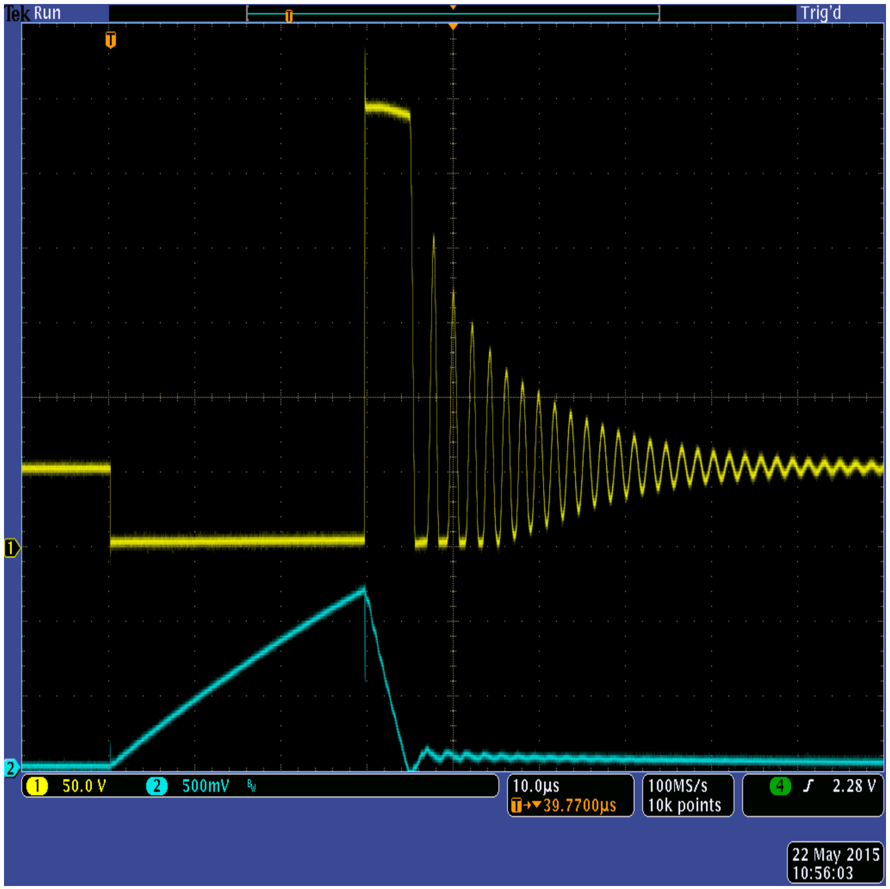
ON Time Adjusted to Obtain Desired I_d(pk) and Thus E_{av}



Ideal Waveforms

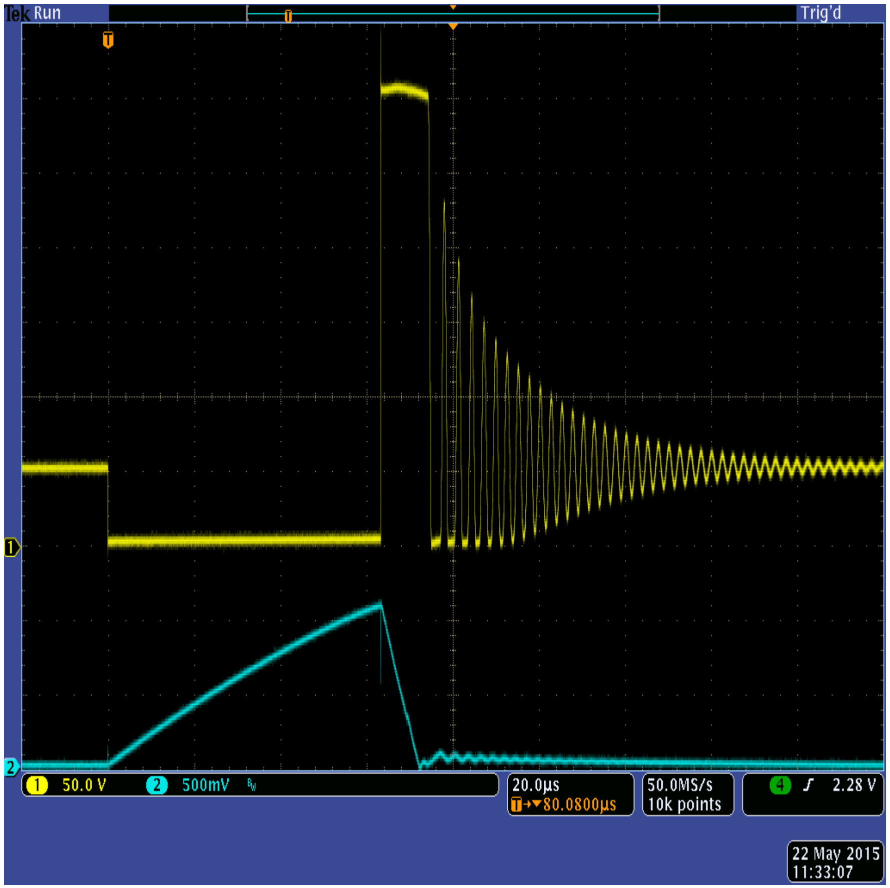
Measured Avalanche Performance

MRH25N15U3, 7.5mJ



$V_{BR}(DSS) = 283V$, $I_d(pk) = 12A$, $t_{on} = 29.5us$

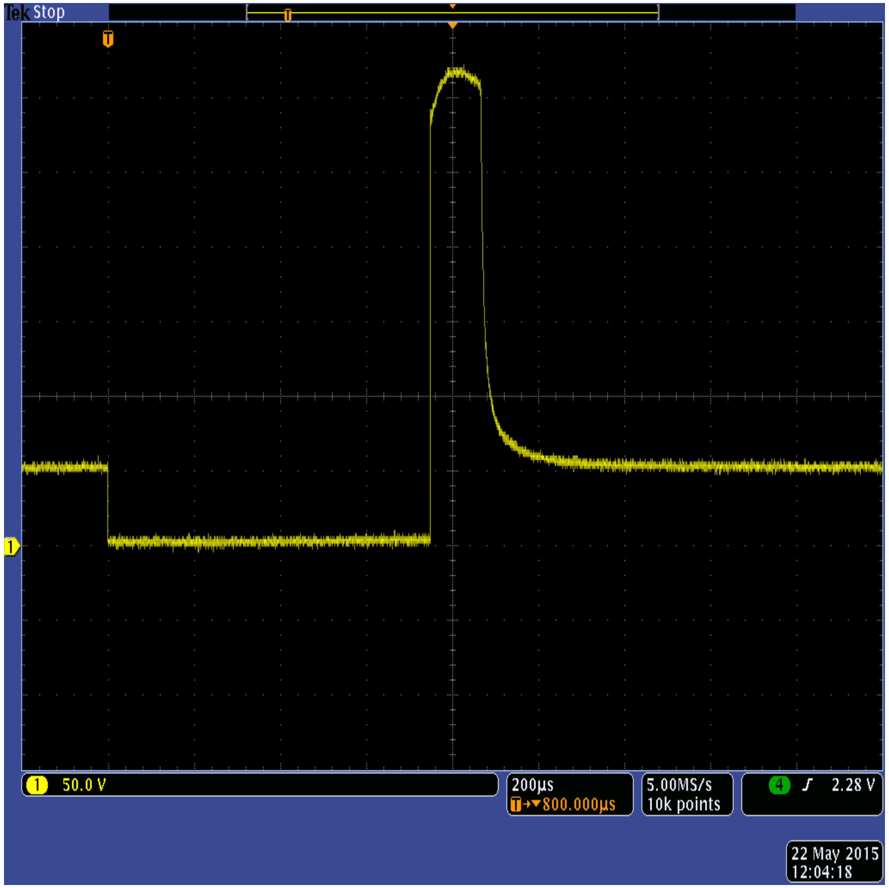
MRH25N15U3, 15mJ



$V_{BR}(DSS) = 304V$, $I_d(pk) = 11A$, $t_{on} = 71.5us$

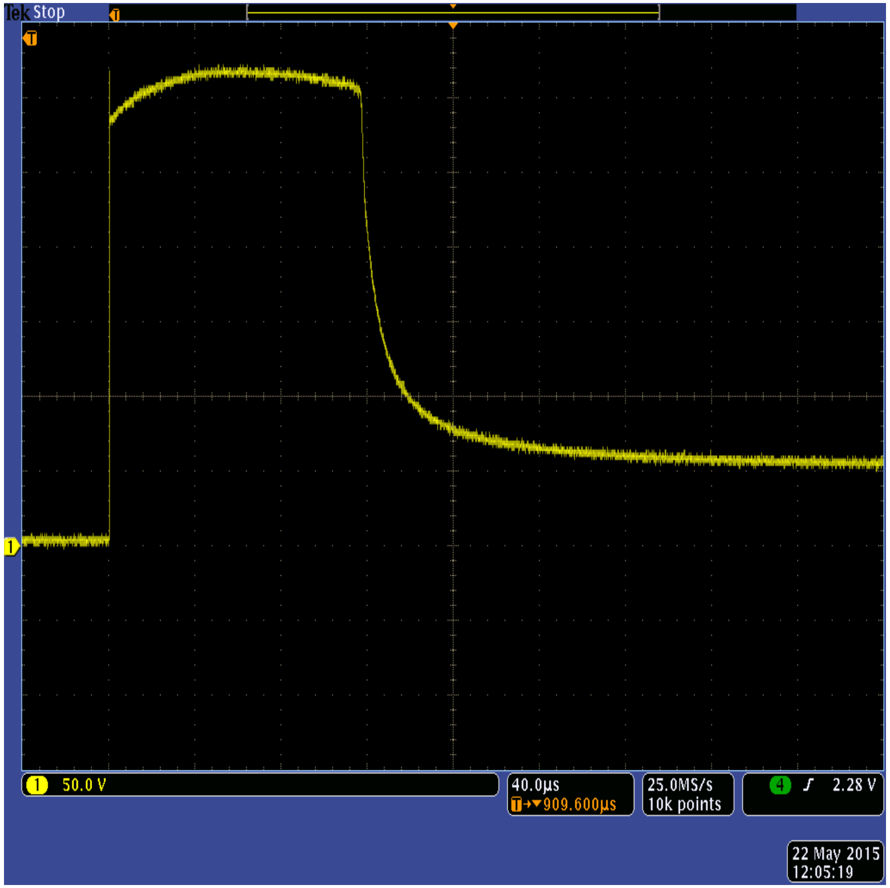
Measured Avalanche Performance

MRH25N15U3, 300mJ



V_{BR}(DSS) = 314V, I_d(pk) = 15A, t_{on} = 750us

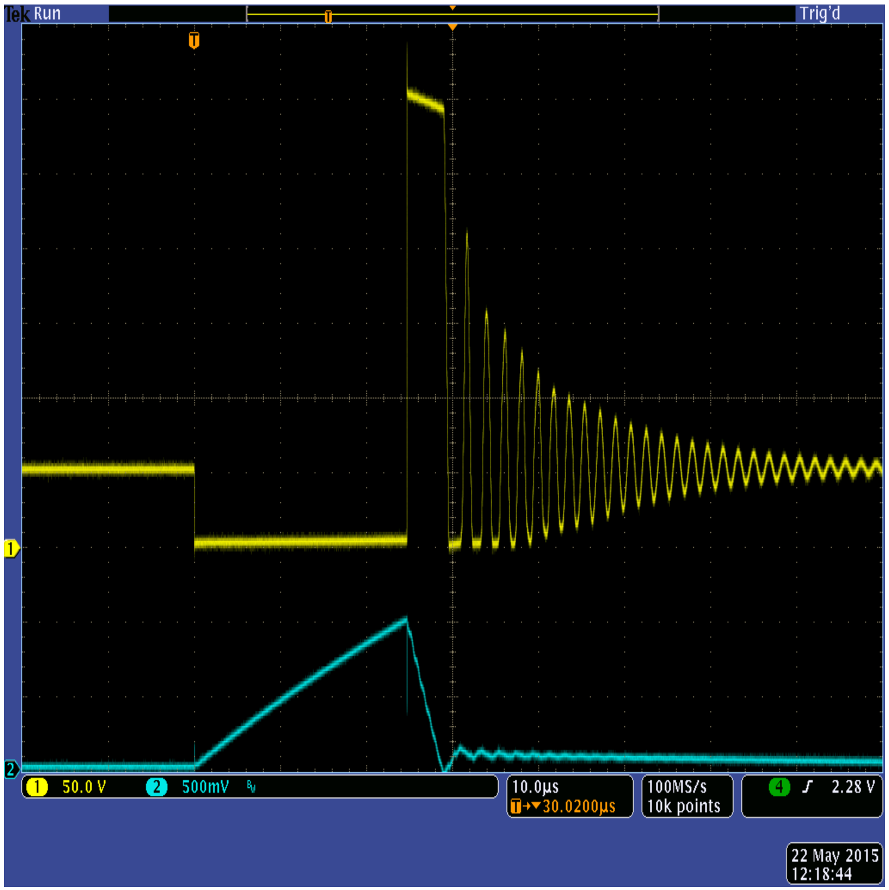
MRH25N15U3, 300mJ (Expanded)



V_{BR}(DSS) = 314V, I_d(pk) = 15A, t_{on} = 750us

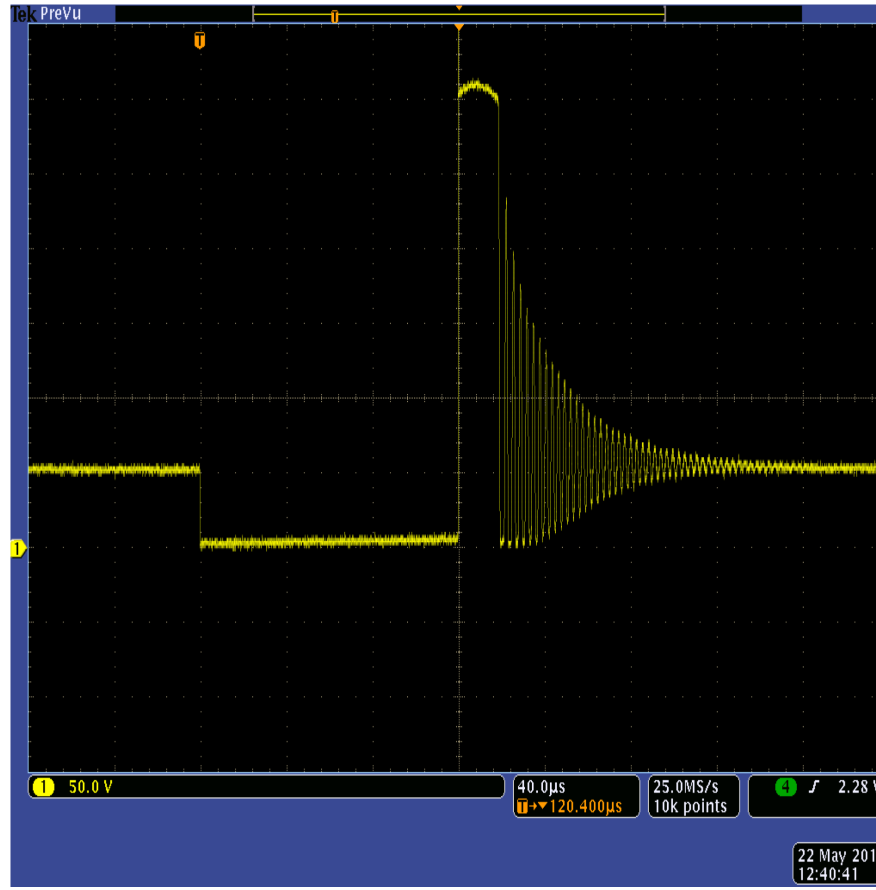
Measured Avalanche Performance

IRHNJ67234, 7.5mJ



V_{BR}(DSS) = 300V, I_d(pk) = 10A, t_{on} = 24.5us

IRHNJ67234, 56mJ



V_{BR}(DSS) = 302V, I_d(pk) = 16.7A, t_{on} = 120us

Summary

Efficiency

- MRH25N15U3 ***Demonstrated More Efficient*** Than IR IRHNJ67234
  - By up to 2.75%
- MGN25N15U3 Efficiency holds up over the full current range of 5A – 20A. Especially at higher load currents
- IRHNJ67234 Efficiency decreases due to higher conduction Losses
  - Useful Output Current Range Must Be De-Rated to 18A
- Increased Losses Mean More Aggressive Thermal Management Required (Bigger Heat Sink for Lower θ_{JA})

Avalanche Capability

- Microsemi MRH25N15U3 **Demonstrated 2X Repetitive Avalanche Capability** Over IR IRHNJ67234
- Microsemi MRH25N15U3 **Demonstrated 5.4X Single Event Avalanche Capability** Over IR IRHNJ67234

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