RTG4 Design Migration User Guide

From Libero SoC vRTG4 Launch to Libero SoC v11.6

Microsemi

Table of Contents

1 – Scope and Audience

This User Guide is intended for Libero SoC users with existing RTG4 projects created with Libero SoC vRTG4 Launch release (Version 11.5.7.11).

For RTG4 devices, Libero SoC v11.6 introduces support of SmartPower, I/O Advisor and SmartDebug. In addition, Libero SoC v11.6 includes enhancements such as Minimum Delay Violation Repair, Multiple-Pass Layout Graphical Interface option and Automatic Constraint Generation for CCC and Oscillator. Refer to the Libero SoC v11.6 Release Notes for details.

We recommend that you upgrade your Libero SoC vRTG4 Launch release design to Libero SoC v11.6 to benefit from important bug fixes and new features.

This User Guide describes the various scenarios when a Libero SoC vRTG4 Launch release project is first opened in Libero SoC v11.6 and the actions you need to take to continue with the design flow in Libero SoC v11.6.

Migrating from Libero SoC vRTG4 Launch Release to Libero SoC v11.6

Before Project Migration - Design Project Backup

Always backup your existing project first before project migration. When you open the existing project in Libero SoC v11.6 release, the Convert Project dialog box appears. Click the **OK** button to create a backup copy of your existing project.

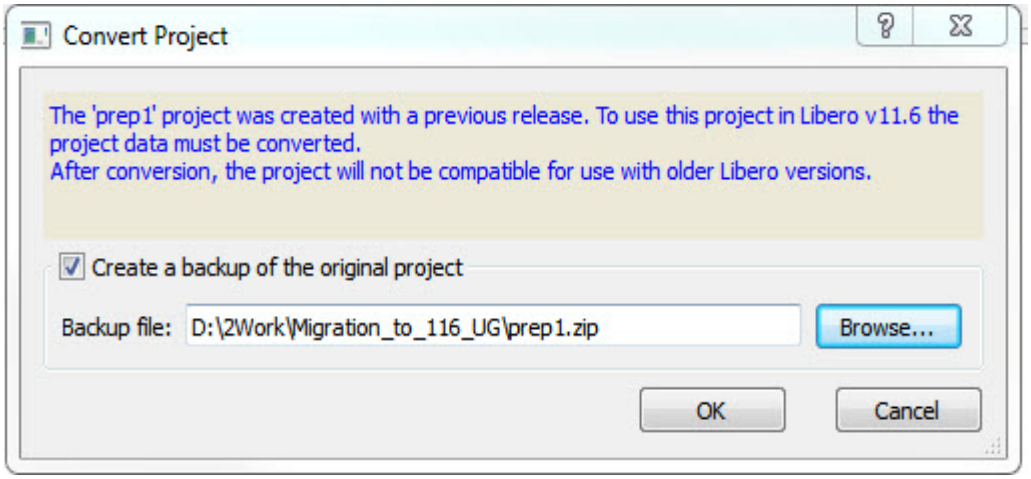

Figure 1-1 **• Convert Project - Backup of Existing Project**

During Project Migration

When you open in Libero SoC v11.6 an RTG4 design saved with Libero SoC vRTG4 Launch release (Version 11.5.7.11), design invalidation may occur. Design invalidation refers to one or both of the following:

- Design Components invalidation
- Design Flow Tool States Invalidation

Design Component Invalidation

When design components are invalidated because IP cores are incompatible with Libero SoC release version, you need to upgrade your IP cores to a version compatible with Libero SoC v11.6, regenerate your components that instantiate the IP cores and continue with design flow.

Design Flow Tool State Invalidation

When only the design flow tool states are invalidated but the design components are intact, you need to clean your design up to the point of invalidation and rerun the design flow to get your design back to its pre-v11.6 state. If the design flow tool states are invalidated because the design components are invalidated, you need to regenerate your design components first before you rerun the design flow.

This User Guide documents various Design Migration Scenarios where RTG4 designs are invalidated when Libero SoC vRTG4 Launch release (Version 11.5.7.11) projects are opened in Libero SoC v11.6. For each scenario, it describes the steps you need to take to complete your design in Libero SoC v11.6.

2 – IP Core Versions and Compatibility with Libero SoC v11.6

When new Libero SoC software is released, some IP cores may become incompatible with the new Libero SoC software. To support the new Libero SoC software release, new IP core versions are developed. New versions of the IP cores are required to support:

- New Core Parameters
- New Software Features
- Silicon Changes

A component that instantiates the incompatible IP cores may become invalidated when it is opened in the new Libero SoC software release.

IP Core Versions Incompatible with Libero SoC v11.6 Release

The Libero SoC v11.6 release makes several IP cores out-of-date. Table 2-1 lists Microsemi IP cores not compatible with the Libero SoC v11.6 release.

***Table 2-1* • IP core Incompatible with Libero SoC v11.6**

Core Name	Incompatible Version	Core Group	Latest Core Version
RTG4FCCC	v1.1.204	Clock & Management	v1.1.206
NPSS_SERDES_IF	v1.1.208	Peripherals	v1.1.215
PCIE_SERDES_IF	v1.1.207	Peripherals	v1.1.215
RTG4FDDRC	1.2.402	Memory & Controllers	v1.2.405
SimDRAM	1.0.100	Simulation Core	v1.0.101

Design Migration and IP Core Upgrade

When you open an existing RTG4 design in Libero SoC v11.6, Libero SoC v11.6 checks for special invalidation rules if any (such as production package pin changes and the FDDR_CLK to DDR_SMC_FIC_CLK clock ratio). It doesn't just invalidate the components when it contains an incompatible core version. An out-of-date core in your component may invalidate your component and/or design flow.

You cannot regenerate the component with the same version of the core. Regenerating the component with the same version of the core triggers an error message.

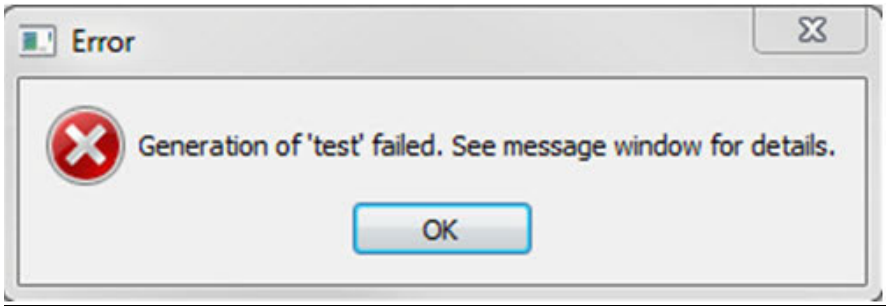

***Figure 2-1* • Libero SoC Error Message**

An explanation of the Error Message is given in the Message Window:

<Core_name> 's core version is not supported in this version of Libero SoC Software. To change the core version, select the instance in the SmartDesign, right-click and choose "Replace Instance Version".

To regenerate the component, you must follow the instructions in the Message Window and upgrade the core to the current version. Right-click the core in SmartDesign and select Replace Instance Version.

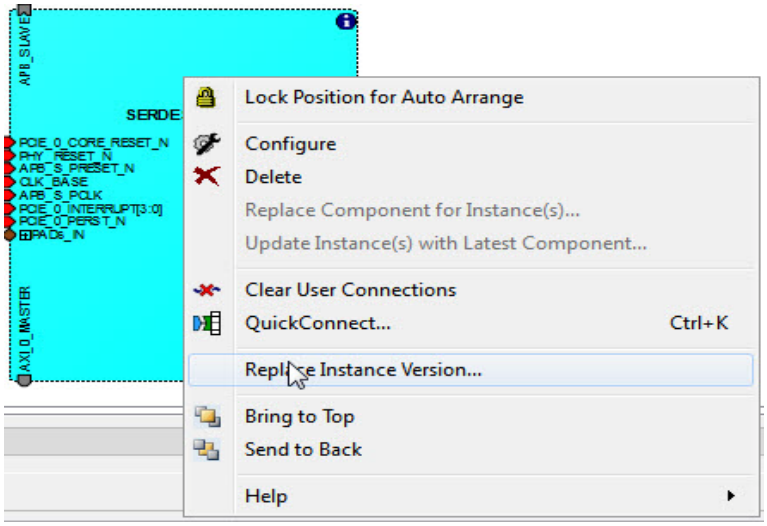

***Figure 2-2* • Replace Instance Version**

The *Change to Version* field is pre-populated with the latest version (if available in your vault). Click **OK** to accept the replacement.

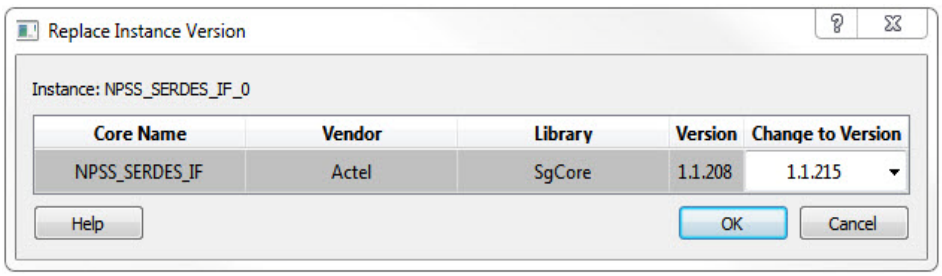

***Figure 2-3* • Replace Instance (Core) Version (To Latest)**

3 – Design Migration Scenarios

This chapter describes the various scenarios and actions you need to take to migrate your design from Libero SoC vRTG4_launch release to Libero SoC v11.6 release.

General Invalidation - Device Package Change

The 1657 CG package, the only package available for RTG4, has changed between the Libero SoC vRTG4 Launch release and the Libero SoC v11.6 release. This change impacts RTG4 design migration.

For details of the package changes, please refer to the following SpaceWire Pin Change docs:

SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon

SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit

For all Libero SoC RTG4 projects created with Libero SoC vRTG4 Launch release with the production device RT4G150-CG1657 package (Speed Grade -1 and STD), the design states are invalidated and the design flow reverts to the pre-compile state when the project is opened in Libero SoC v11.6. This invalidation is due to the package pin changes in the 1657 CG package of the RTG4-150 production die. It affects all projects with this die and package, regardless of the component and cores used in the project.

To continue the design flow in Libero SoC v11.6, you must rerun the complete design flow from the compile state.

Note: This design flow invalidation affects only the RT4G150-CG1657 production devices. Libero SoC vRTG4 Launch release projects with RTG4-ES (Engineering Sample) device are not impacted because there are no package changes in the Engineering Sample (ES) RT4G150-ES CG1657 device.

Scenario #1 Design Component contains PCIe_SERDES_IF Core (PCIe/EPCS/XAUI Mode)

In this scenario, your Libero SoC vRTG4 Launch release project contains the PCIe_SERDES_IF core version 1.2.207 and you open the design project in Libero SoC v11.6.

The scenario refers to situations when the core is used alone in the Libero SoC project to be migrated to Libero SoC v11.6. Existence of other cores in the design project and other project parameters (e.g. die/package) may trigger different behaviors which may include invalidation of the design flow states or invalidation of the components containing the cores.

Libero SoC v11.6 Behavior on Design Migration

When you migrate your design to Libero SoC v11.6 release, Libero SoC v11.6 behavior varies with the device type in your project. If the Libero SoC project is targeted for RT4G150 production (non-ES) devices, the design flow is invalidated after migration. If the Libero SoC project is targeted for RT4G150-ES (Engineering Sample) devices, the design flow is kept intact after migration.

PCIe_SERDES_IF Core in RT4G Production Devices

For PCIe_SERDES_IF core in RT4G150-CG1657 production devices, when the project is opened in Libero SoC v11.6, the design states are invalidated. The design flow reverts to the pre-compile state because the package pins have changed since the Libero SoC vRTG4 Launch release. A Warning Message alerts you to the design state invalidation.

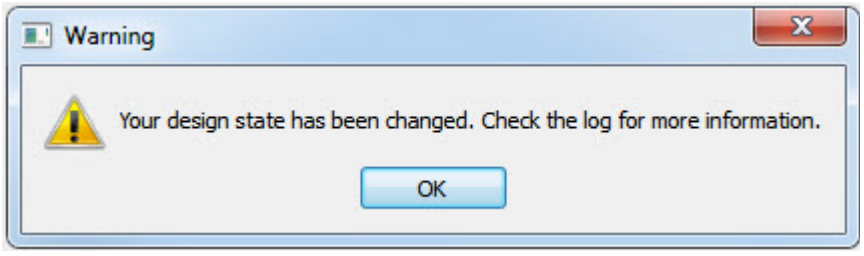

Figure 3-1 • **Warning Message**

The Log Window displays the design flow invalidation message:

Info: Your design has been invalidated to the pre-compile state because the package pins were not up-to-date.

In addition, the Log Window displays a message on the core version's incompatibility with Libero SoC v11.6:

Info: SmartDesign 'mytop' uses core 'PCIE_SERDES_IF' which is out of date. You must update to the latest version and regenerate your design.

Follow these steps to continue with the design in Libero SoC v11.6:

1. Upgrade (right-click on core > Replace Instance Version) the PCIe_SERDES_IF Core to the latest version (v1.1.215).

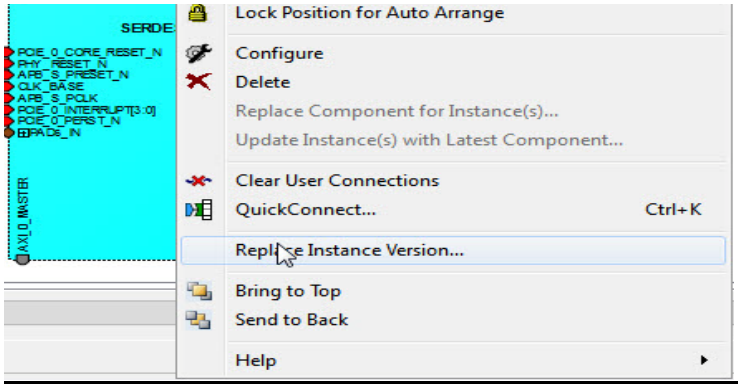

Figure 3-2 • **Replace Instance Version of Core**

2. Choose the latest version, 1.1.215, as the replacement version. Click **OK.**

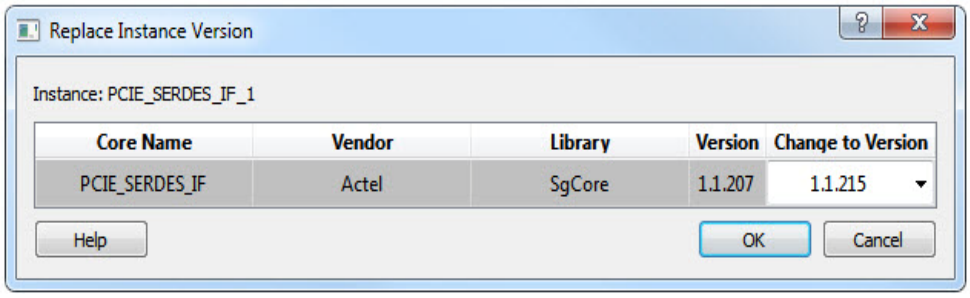

***Figure 3-3* • Upgrading Core to Latest Version**

3. Regenerate the component that instantiates the core.
4. Rerun the design flow.

PCIe_SERDES_IF core in RTG4 Engineering Sample (RT4G150_ES) Devices

After the project is migrated to Libero SoC v11.6, no design flow is invalidated. No component is invalidated. You may continue with the design flow in Libero SoC v11.6 with the original existing version of the PCIe_SERDES_IF core. Alternatively, you may update the version of PCIE_SERDES_IF core to the current version, re-generate the component and re-run your design flow in Libero v11.6.

Scenario #2 Design Component contains NPSS_SERDES_IF Core (EPCS/XAUI Mode)

In this scenario, your Libero SoC vRTG4 Launch release project contains the NPSS_SERDES_IF core version 1.1.208 and you open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (PCIE_SERDES_IF/FCCC/FDDR) or other project parameters (e.g. die/package) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

When you migrate your design to Libero SoC v11.6 release, Libero SoC v11.6 behavior varies with the device type in your old project. For RT4G150 production (non-ES) devices, the design flow is invalidated after migration. For RT4G150-ES (Engineering Sample) devices, the design flow is kept intact after migration.

NPSS_SERDES_IF Core in RT4G Production Devices

For NPSS_SERDES_IF Core in RT4G150-CG1657 production devices, when the project is opened in Libero SoC v11.6, the design states are invalidated. The design flow reverts to the pre-compile state

because the package pins have changed since the Libero SoC vRTG4 Launch release. A Warning Message alerts you to the design state invalidation.

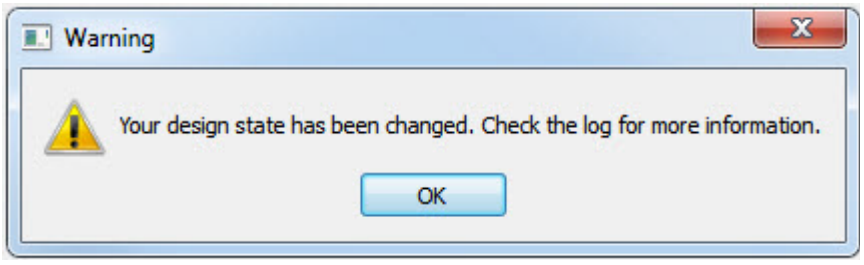

Figure 3-4 • **Warning Message**

The Log Window displays a message about design flow invalidation:

Info: Your design has been invalidated to the pre-compile state because the package pins were not up-to-date.

In addition, the Log window displays a message about core incompatibility:

Info: SmartDesign 'mytop' uses core 'NPSS_SERDES_IF' which is out of date. You must update to the latest version and regenerate your design

Follow these steps to continue with the design in Libero SoC v11.6:

1. upgrade the NPSS_SERDES_IF Core to the latest version (right-click on core > Replace Instance Version).

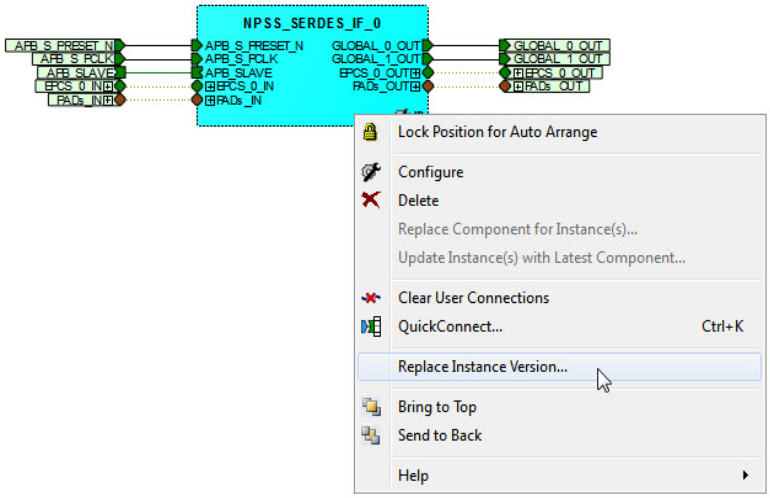

***Figure 3-5* • Replace Instance Version of Core**

2. Choose the current version, 1.1.215, as the replacement version. Click **OK.**

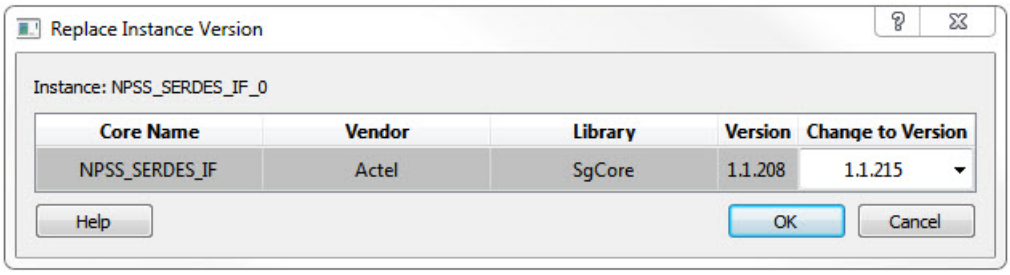

***Figure 3-6* • Upgrading to the Core's Current Version**

3. Regenerate the component that instantiates the core
4. Rerun design flow.

NPSS_SERDES_IF Core in RTG4 Engineering Sample (RT4G150_ES) Devices

After migration to Libero SoC v11.6, the design flow is kept intact. No design states or components are invalidated. You may continue with the design flow in Libero SoC v11.6 with the original existing version of the NPSS_SERDES_IF core. Alternatively, you may update the version of NPSS_SERDES_IF core to the current version, re-generate the component and re-run your design flow in Libero v11.6.

Scenario #3 Design Component Contains FDDR Core

In this scenario, your Libero SoC vRTG4 Launch design project contains the FDDR core version 1.2.402 (incompatible with Libero SoC v11.6) and you open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero SoC project. Existence of other cores (SERDES_IF/FCCC) in the design project or other design parameters (die/package) may trigger different

behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

When you migrate your design to Libero SoC v11.6 release, Libero SoC v11.6 behavior varies with the device type in your old project. For RT4G150 production (non-ES) devices, the design flow is invalidated after migration. For RT4G150-ES (Engineering Sample) devices, the design flow is kept intact after migration.

FDDR Core in RT4G Production Devices

For FDDR Core in RT4G150-CG1657 devices, when the project is opened in Libero SoC v11.6, the design states are invalidated. The design flow reverts to the pre-compile state because the package pins have changed since the Libero SoC vRTG4 Launch release. A Warning Message alerts you to the design state invalidation.

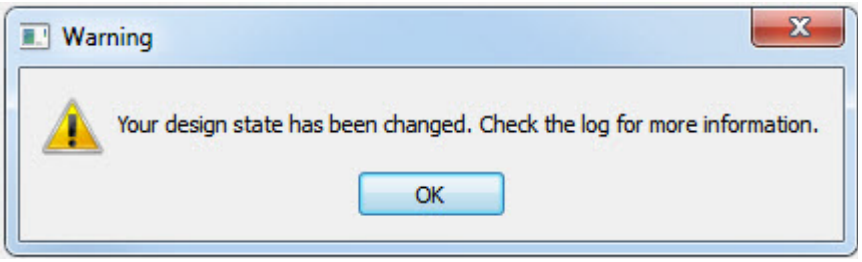

***Figure 3-7* • Warning Message**

The Log window displays the Design Flow Invalidation message:

Info: Your design has been invalidated to the pre-compile state because the package pins were not up-to-date.

In addition, the Log Window displays a message on the core version's incompatibility with Libero SoC v11.6.

Info: SmartDesign 'mytop' uses core 'RTG4FDDRC' which is out of date. You must update to the latest version and regenerate your design.

Follow these steps to continue with the design in Libero SoC v11.6:

1. Upgrade the RTG4FDDRC_0 Core to the current version (right-click on core > Replace Instance Version).

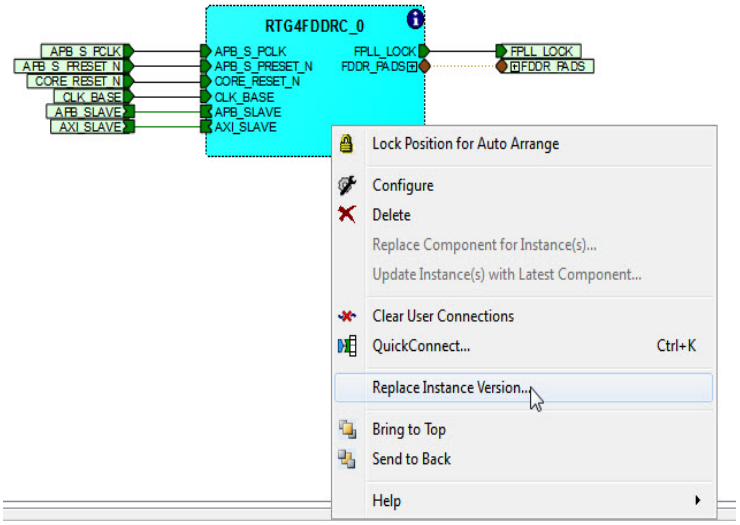

***Figure 3-8* • Replace Instance Version of Core**

2. Choose the current version, 1.2.405, as the replacement version.Click **OK**.

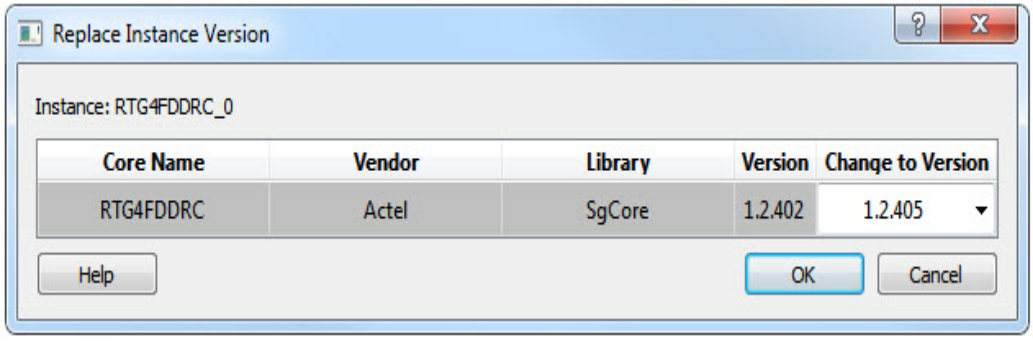

***Figure 3-9* • Upgrading to the Core's Current Version**

3. Regenerate the component that instantiates the core.
4. Rerun design flow.

FDDR core in RTG4 Engineering Sample (RT4G150_ES) Devices

After migration to Libero SoC v11.6, the design flow is kept intact. No design states or components are invalidated. You may continue with the design flow in Libero SoC v11.6 with the original existing version of the FDDR core. Alternatively, you may update the version of the FDDR core to the current version, re-generate the component and re-run your design flow in Libero SoC v11.6.

Scenario #4 Design Component Contains FCCC

In this scenario, your Libero SoC vRTG4 Release design project contains the Fabric CCC core version 1.1.204 and your CCC is configured to have a PLL output frequency of over 425 MHz.

Libero SoC v11.6 Behavior on Design Migration

The component instantiating the RTG4FCCC is invalidated. For both the RT4G150 and RT4G150-ES devices, the Log window gives this Message:

Info: Component 'SD1' is invalidated because the maximum PLL output frequency is limited to 425MHz. You must update to the latest version and regenerate your design.

In addition, if the die is the production RT4G150 die, the design flow is invalidated because of CG 1657 package changes. The invalidation message appears in the Log window:

Info: Your design has been invalidated to the pre-compile state because the package pins were not up-to-date.

User Follow-up Actions

Follow these steps to continue in Libero SoC v11.6 flow:

1. Upgrade the RTG4FCCC Core (Right-click on core > Replace Instance Version) to the current version.
2. Regenerate the component.
3. Rerun the design flow.

Scenario #5 Design Component Contains SimDRAM Core (SimDRAM)

In this scenario, you open in Libero SoC v11.6 a Libero vRTG4 Launch release design project which contains a SmartDesign testbench component that instantiates the SimDRAM core (v.1.0.100), which is a Microsemi simulation model for an external DDR memory.

Libero SoC v11.6 Behavior on Design Migration

When the project is opened in Libero SoC v11.6, no design states are invalidated and no component, including the SmartDesign Testbench component, is invalidated.

In the Log Window, this Error Message appears:

Error: Core 'Actel:Simulation:SimDRAM:1.0.100' is missing from the vault.

Libero SoC is searching in the vault for SimDRAM v1.0.100 which has been superseded by v.1.0.101 in Libero SoC v11.6. SimDRAM v.1.0.100 is incompatible with Libero SoC v11.6 and therefore not visible in Libero SoC v11.6 IP Catalog.

User Follow-up Actions

Libero SoC requires that you upgrade the SimDRAM core to the current version (v1.0.101) and then regenerate the SmartDesign Testbench component.

If you regenerate the SmartDesign Testbench component without first upgrading the SimDRAM core version, Libero SoC gives the Error Message:

Generation of SmartDesign Testbench <Component_name> failed. See Message Window for details.

The message window tells you to upgrade the SimDRAM core first.

SimDRAM_0's core version is not supported by this version of Libero SoC software. To change the core version, select the core instance in SmartDesign, right-click and choose "Replace Core Version".

Follow these steps to continue your design flow in Libero SoC v11.6:

1. Download the SimDRAM core current version 1.0.101 into your vault.
2. Upgrade the SimDRAM core to version 1.0.101 (right-click on core > Replace Core Version).
3. Regenerate the SmartDesign Testbench that instantiates the SimDRAM core.
4. Rerun simulation with the SmartDesign Testbench component as the Active Stimulus.

After Project Migration

After you have successfully migrated your design to Libero SoC v11.6, follow these steps to ensure your design goals are met with Libero SoC v11.6:

1. If design flow is invalidated to pre-compile state, run design flow to post-layout state. If design flow is not invalidated and in post-layout state, skip and go to Step 2.
2. Invoke SmartTime to generate the Timer Report. Review the Timing Report to ensure that your design meets your timing requirements.
3. Invoke SmartPower to generate the Power Report. Review the Power Report to ensure that your design meets your power requirements.

4 – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,600 employees globally. Learn more at **www.microsemi.com**.

5-02-00654-0/08.15