SmartFusion2/IGLOO2 Design Migration User Guide

Microsemi

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1 – Scope and Audience

This User Guide is intended for Libero users with existing SmartFusion2/IGLOO2 projects created with the Libero SoC v11.5 Release and subsequent Service Packs.

For SmartFusion2/IGLOO2 devices, Libero SoC v11.6 introduces several new features and enhancements which include Minimum Delay Violation Repair, Multiple-Pass Layout Graphical Interface, Synthesis and Compile Global Management Options, Synthesis Retiming from Libero Synthesis Dialog box, Automatic Constraint (False Path) Generation for CoreResetP, Automatic Constraints (Clock Period) Generation for CCC and Oscillator and Direct Connection Mode for System Builder. Refer to the Libero SoC v11.6 Release Notes for details.

We recommend that you upgrade your SmartFusion2/IGLOO2 design to Libero SoC v11.6 to benefit from important bug fixes and new features.

This User Guide describes the various scenarios when a Libero SoC v11.5 project is first opened in Libero SoC v11.6 and the actions you need to take to continue with the design flow in Libero SoC v11.6.

Migrating from Libero SoC v11.5 to Libero SoC v11.6 Release

Before Project Migration - Design Project Backup

Always backup your existing project first before project migration. When you open the existing project in the Libero SoC v11.6 release, the Convert Project dialog box appears. Click the **OK** button to create a backup copy of your existing project.

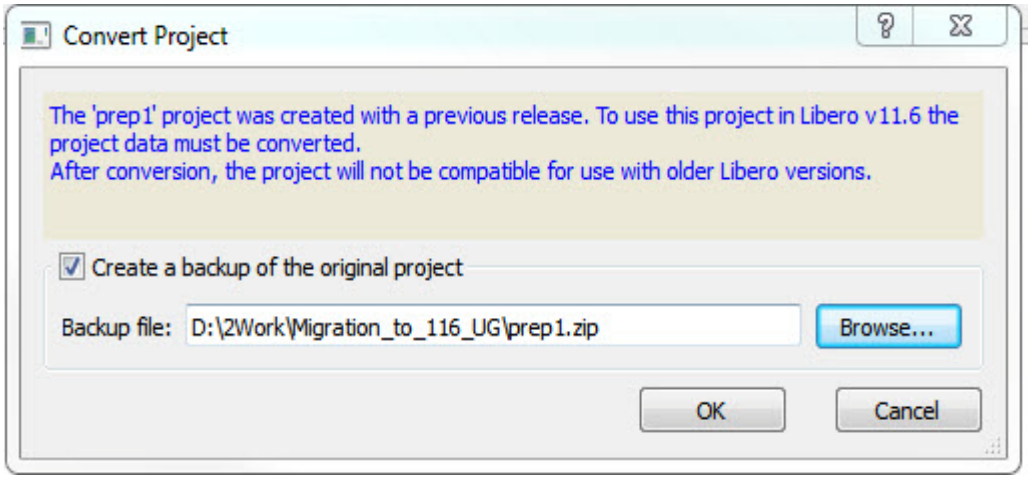

***Figure 1-1* • Convert Project - Backup of Existing Project**

During Project Migration - Upgrade IP Cores

When you open in Libero SoC v11.6 a project saved with Libero SoC v11.5 or subsequent Service Packs, design invalidation may occur. Design invalidation refers to one or both of the following:

- Design Components invalidation
- Design Flow Tool States Invalidation

Design Component Invalidation

When design components are invalidated because IP cores are incompatible with Libero release version, you must upgrade your IP cores to a version compatible with Libero SoC v11.6, regenerate your components that instantiate the IP cores and continue with design flow.

Design Flow Tool State Invalidation

When only the design flow tool states are invalidated but the design components are intact, you must clean your design up to the point of invalidation and rerun the design flow to get your design back to its pre-11.6 state. If the design flow tool state is invalidated because the design components are invalidated, you must upgrade and regenerate your design components first before you rerun the design flow.

This User Guide documents various Design Migration Scenarios where SmartFusion2/IGLOO2 designs are invalidated when Libero SoC v11.5 projects are opened in Libero SoC v11.6. For each scenario, it describes the steps you need to take to complete your design in Libero SoC v11.6.

After Project Migration

After you have successfully migrated your design to Libero 11.6, follow these steps in Libero SoC v11.6 to ensure your design goals are met:

1. If design flow is invalidated to pre-compile state, run design flow to post-layout state. If design flow is not invalidated and in post-layout state, skip to Step 2.
2. Invoke SmartTime to generate the Timer Report. Review the Timing Report to ensure that your design meets your timing requirements.
3. Invoke SmartPower to generate the Power Report. Review the Power Report to ensure that your design meets your power requirements.

2 – IP Core Versions and Compatibility with Libero

When new Libero software is released, some IP cores may become incompatible with the new Libero software. To support the new Libero software release, new IP core versions are developed. New versions of the IP cores are developed to support:

- New Core Parameters
- New Software Features
- Silicon Changes

A component that instantiates the incompatible and out-of-date IP cores may become invalidated when the design project migrates to a new Libero software release.

IP Core Versions Incompatible with Libero SoC v11.6 Release

With the Libero SoC v11.6 release, several IP cores have become incompatible. Table 2-1 lists Microsemi IP cores incompatible with Libero SoC v11.6 Release.

Table 2-1 • IP Cores Incompatible with Libero SoC v11.6

Core Name	Incompatible Version	Core Category	Latest Core Version
SERDES_IF	v1.2.201	Peripherals	v1.2.206
SERDES_IF	v1.2.103	Peripherals	v1.2.206
SERDES_IF2	v1.2.202	Peripheral	v1.2.208
SERDES_IF2	v1.2.204	Peripherals	v1.2.208
SERDES_IF2	v1.2.105	Peripherals	v1.2.208
SERDES_IF3	v1.2.202	Peripherals	v1.2.207
SERDES_IF3	v1.2.103	Peripherals	v1.2.207
MSS	1.1.209	Processor	v1.1.400
MSS	1.1.300	Processor	v1.1.400
FDDRC	1.1.204	Controllers	v1.1.301
FDDRC	1.1.205	Controllers	v1.1.301
SimDRAM	1.0.100	Simulation Model	v1.0.101
Tamper/Tamper2	2.1.200	Soft Configuration Core	v2.1.300

Design Migration and IP Core Upgrade

When you open an existing SmartFusion2 or IGLOO2 design in Libero SoC v11.6, Libero SoC v11.6 only checks for special invalidation rules, if any (such as the DDR AXI clock ratio). It does not just invalidate the components if it contains an incompatible core version. An out-of-date core in your component may invalidate your component and/or design flow.

You cannot regenerate the component with the same version of the core. Regenerating the component with the same version of the core triggers an error message..

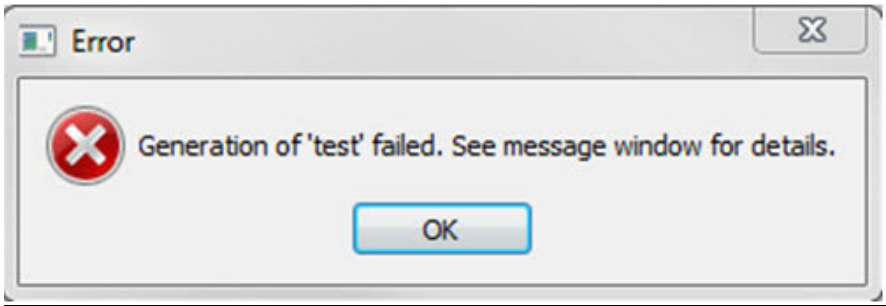

***Figure 2-1* • Libero Error Message**

An explanation of the Error Message is given in the Message Window:

<Core_name> 's core version is not supported in this version of Libero SoC Software. To change the core version, select the instance in the SmartDesign, right-click and choose "Replace Instance Version".

To regenerate the component, you must follow the instructions in the Message Window and upgrade the core to the current version. Right-click the core in SmartDesign and select Replace Instance Version.

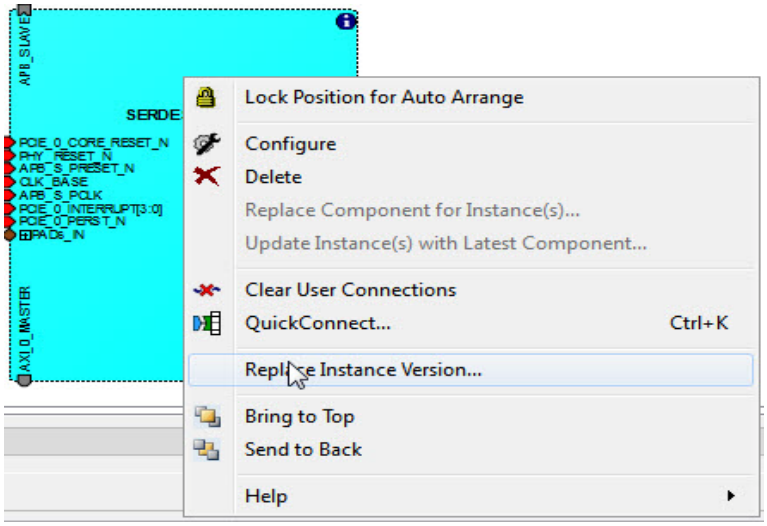

***Figure 2-2* • Replace Instance Version**

The **Change to Version** field is pre-populated with the latest version (if available in your vault). Click **OK** to accept the replacement.

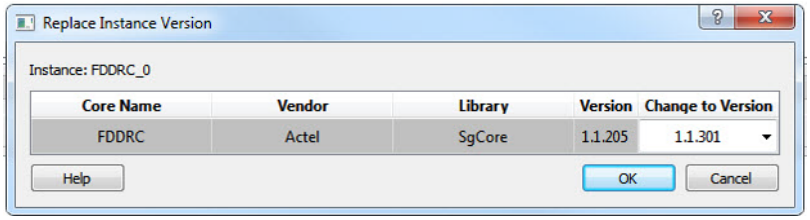

***Figure 2-3* • Replace Instance (Core) Version (To Latest)**

MSS Version Replacement

From the Design Hierarchy window, right-click MSS core and click **Replace Component Version**.

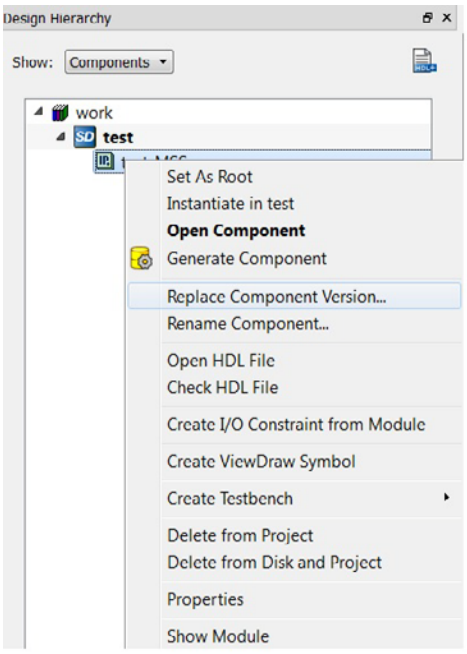

***Figure 2-4* • Replacement Component Version (To Latest) -- Design Hierarchy Window**

In the Replace Component Version dialog box, select the latest core version from the **Change to Version** drop-down list.

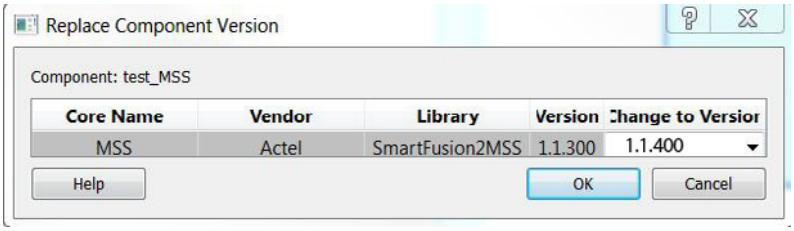

***Figure 2-5* • Replacement Core Version (To Latest)**

3 – Design Migration Scenarios

This chapter describes the various scenarios and actions you need to take to migrate your design from Libero SoC v11.5 (and subsequent Service Packs) to Libero SoC v11.6 release. Except for the MSS component, the scenarios listed here apply to both SmartFusion2 and IGLOO2 devices.

Scenario #1 Design Component Contains SERDES_IF Core (EPCS/XAUI Mode)

In this scenario, your Libero SoC v11.5 design project contains the SERDES_IF core version 1.2.201/1.2.103 (incompatible with Libero SoC v11.6) and you open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project. Existence of other cores in the design project or other die/package may trigger different behaviors which may include invalidation of the design flow states or invalidation of the components containing the cores.

Libero SoC v11.6 Behavior on Design Migration

The design flow states and design components remain intact. No design state is invalidated. Libero does not require you to upgrade the core SERDES_IF core to the latest version.

Note: If you plan to reconfigure the SERDES core to make a change or take advantage of the latest features, such as Signal Integrity options or Power Management options, you must upgrade to the latest SERDES core version.

User Follow-up Actions

There is no need to upgrade the SERDES_IF Core to the latest version. After opening your project in Libero SoC v11.6, you may continue with your design flow in Libero SoC v11.6 to generate programming file, timing and power reports.

Note: If you plan to reconfigure the SERDES core to make a change or take advantage of the latest features, such as Signal Integrity options or Power Management options, you "must" upgrade to the latest SERDES core version.

If you want to reconfigure the existing SERDES_IF settings or configure the new SERDES_IF options introduced in Libero SoC v11.6, such as the Signal Integrity options, you must first upgrade your SERDES_IP Core version to the latest version (Right-click core > Replace Instance Version), reconfigure the Signal Integrity options, regenerate the component and rerun the design flow.

Note: If you reconfigure Signal Integrity Options in the existing/old version of the core, you may hit a runtime error from Libero.

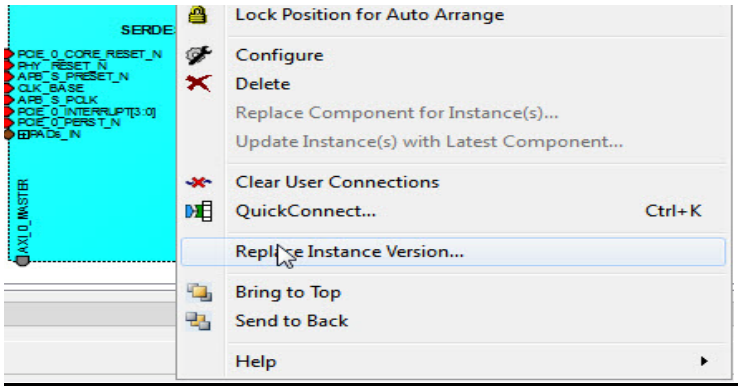

Figure 3-1 • **Replace Instance Version of Core**

Scenario #2 Design Component Contains SERDES_IF Core (PCIe Mode)

In this scenario, your Libero SoC v11.5 design project contains the SERDES_IF core version 1.2.201/1.2.103 (incompatible with Libero SoC v11.6) and you open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (MSS/HPMS/MDDR/FDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow states and design components remain intact. No design state is invalidated. Libero does not require you to upgrade the core SERDES_IF core to the latest version.

Note: If you plan to reconfigure the SERDES core to make a change or take advantage of the latest features, such as Power Management options, you "must" upgrade to the latest SERDES core version.

User Follow-up Actions

There is no need to upgrade the SERDES_IF Core to the latest version. After opening your project in Libero SoC v11.6, you may continue with your design flow in Libero SoC v11.6 to generate programming file, timing and power reports.

Note: If you plan to reconfigure the SERDES core to make a change or take advantage of the latest features, such as Power Management options, you "must" upgrade to the latest SERDES core version.

You may choose to upgrade the core to the current version (Right-click core > Replace Instance Version), regenerate the core and rerun the design flow.

If you want to reconfigure the existing SERDES_IF settings or configure the new SERDES_IF options introduced in Libero SoC v11.6, such as the Power Management Settings (ASPM) in PCIe, you must first upgrade your SERDES_IP Core version to the latest version (Right-click core > Replace Instance Version), reconfigure the desired options, regenerate the component and rerun the design flow.

Scenario #3 Design Component Contains SERDES_IF2 Core (EPCS/XAUI Mode)

In this scenario, your Libero SoC v11.5 design project contains the SERDES_IF2 core version 1.2.202/1.2.204/ 1.2.105 (incompatible with Libero SoC v11.6) and you open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (MSS/HPMS/MDDR/FDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow states and design components remain intact. No design state is invalidated. Libero does not require you to upgrade the core SERDES_IF2 core to the current version.

User Follow-up Actions

There is no need to upgrade the SERDES_IF Core to the current version. After opening your project in Libero SoC v11.6, you may continue with your design flow in Libero SoC v11.6 to generate programming file, timing and power reports. You may choose to upgrade the core to the current version (Right-click core > Replace Instance Version), regenerate the core and rerun the design flow.

If you want to reconfigure the Signal Integrity options of the SERDES_IF Core, you must first upgrade your SERDES_IP Core version to the current version (Right-click core > Replace Instance Version), reconfigure the core, regenerate the component and rerun the design flow

Note: If you reconfigure Signal Integrity Options in the existing/old version of the core, you may hit a runtime error from Libero.

Scenario #4 Design Component Contains SERDES_IF2 Core (PCIe Mode)

In this scenario, your Libero SoC v11.5 design project contains the SERDES_IF2 core version 1.2.202/ 1.2.204/1.2.105 (incompatible with Libero SoC v11.6) and you open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (MSS/HPMS/MDDR/FDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow states and design components remain intact. No design state is invalidated. Libero does not require you to upgrade the core SERDES_IF core to the current version.

User Follow-up Actions

There is no need to upgrade the SERDES_IF Core to the current version. After opening your project in Libero SoC v11.6, you may continue with your design flow in Libero SoC v11.6 to generate programming file, timing and power reports. You may choose to upgrade the core to the current version (Right-click core > Replace Instance Version), regenerate the core and rerun the design flow.

Scenario #5 Design Component Contains SERDES_IF3 (PCIe/ EPCS Mode)

In this scenario, your Libero SoC v11.5 design project contains the SERDES_IF3 core version 1.2.202/1.2.103 (incompatible with Libero SoC v11.6) and you open the design project in Libero 11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (MSS/HPMS/MDDR/FDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow states and design components remain intact. No design state is invalidated. The design component which contains the SERDES_IF3 core is not invalidated. Libero does not require you to upgrade the core SERDES_IF3 core to the current version.

User Follow-up Actions

There is no need to upgrade the SERDES_IF Core to the current version. After opening your project in Libero SoC v11.6, you may continue with your design flow in Libero SoC v11.6 to generate programming file, timing and power reports. You may choose to upgrade the core to the current version (Right-click core > Replace Instance Version), regenerate the component and rerun the design flow.

Scenario #6 Design Component Contains MSS/MDDR (DDR_AXI clock ratio=1)

In this scenario, your Libero SoC v11.5 design project contains the MSS core version 1.1.209/1.1.300 (incompatible with Libero SoC v11.6) and the MDDR is either disabled OR enabled with DDR_AXI clock ratio of 1 (MDDR_CLK to DDR_SMC_FIC_CLK is on a 1:1 ratio). You open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (FDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow states and design components remain intact. No design state is invalidated. The design component which contains the MSS core is not invalidated. Libero does not require you to upgrade the MSS core to the latest version if you don't plan to reconfigure/regenerate the MSS component OR rerun the design flow from the pre-Compile state.

User Follow-up Actions

You may continue with the design flow (post-compile state) to generate programming file, timing or power report.

However, if you want to reconfigure/regenerate the MSS component OR rerun the design flow from the pre-Compile state, you must first upgrade the MSS core version to 1.1.400 and regenerate the MSS component before you recompile your design. If you don't, Compile gives you an error with the Info: *Your design contains an MDDR. The DDR clock frequency parameter is not set; you must re-generate the MSS component and re-run the flow.*

If you've used System Builder in your design which includes the MDDR, System Builder automatically instantiates the latest version of the MSS (automatic upgrade) to replace the old MSS version when you regenerate the System Builder component.

Scenario #7 Design Component Contains MSS/MDDR (DDR_AXI clock ratio > 1)

In this scenario, your Libero SoC v11.5 design project contains the MSS core version 1.1.209/1.1.300 (incompatible with Libero SoC v11.6) and the MDDR is enabled with DDR_AXI clock ratio bigger than 1 (MDDR_CLK to DDR_SMC_FIC_CLK ratio is bigger than 1). You open the design project in Libero SoC v11.6.

Libero SoC v11.6 Behavior on Design Migration

When you open the design in Libero SoC v11.6, you see an info message in the Libero log window:

Info: Your design contains an MDDR. The DDR clock frequency parameter is not set; you must re-generate the MSS component and re-run the flow.

All design flow states are invalidated. If your design is a regular Smart Design-based design (NOT a System Builder design) that uses MSS, then the MSS component is invalidated. Libero requires you to upgrade the MSS core to the latest version. To upgrade the MSS core version, right-click the MSS component in the Libero Design Hierarchy window > Replace Component Version. If you do not upgrade the core version to the latest, an error message appears in the Message Window when you regenerate the component:

test_MSS_0's core version is not supported by this version of the Libero SoC Software. To change the MSS version, select the component in the Design Hierarchy, right-click and choose "Replace Component Version".

If your design is a System Builder-based design that includes MDDR, then the System Builder component is invalidated. Libero requires you to open the System Builder block and regenerate the design in System Builder.

User Follow-up Actions

Libero requires that you update the MSS core (right-click the MSS component in the Libero Design Hierarchy window > Replace Component Version) and regenerate the MSS component and rerun the complete design flow.

If you've used System Builder in your design which includes the MDDR, System Builder automatically instantiates the latest version of the MSS (automatic upgrade) to replace the old MSS version when you regenerate the System Builder component.

Scenario #8 Design Component Contains FDDR (DDR_AXI clock ratio = 1)

In this scenario, your Libero SoC v11.5 design project contains the FDDRC core version 1.1.204/1.1.205
(incompatible with Libero SoC v11.6) with DDR_AXI clock ratio equal to 1 (FDDR_CLK to DDR_SMC_FIC_CLK ratio = 1:1). You open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (MSS/HPMS/MDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow and design components remain intact. No design state is invalidated. The design component which contains the FDDR core is not invalidated. Libero does not require you to upgrade the FDDR core to the latest version if you don't plan to reconfigure the FDDR OR rerun the design flow from the pre-Compile state.

User Follow-up Actions

No corrective action is required if you want to continue with the design flow (post-compile state) to generate programming file, timing or power report.

However, if you want to reconfigure the FDDR OR rerun the design flow from the pre-Compile state, you must upgrade the FDDR core version to the latest version and regenerate the component before you recompile your design. If you don't, Libero gives you an error with the Info: *Your design contains an FDDR. The DDR clock frequency parameter is not set; you must replace the FDDR with the latest version, re-generate the core and re-run the flow.*

If you've used System Builder in your design which includes the FDDR, System Builder automatically instantiates the latest version of the FDDR (automatic upgrade) to replace the old FDDR version when you regenerate the System Builder component.

Scenario #9 Design Component Contains FDDR (DDR_AXI clock ratio > 1)

In this scenario, your Libero SoC v11.5 design project contains the FDDRC core version 1.1.204/1.1.205 (incompatible with Libero SoC v11.6) with DDR_AXI clock ratio bigger than 1 (FDDR_CLK to DDR_SMC_FIC_CLK ratio is bigger than 1). You open the design project in Libero SoC v11.6.

Libero SoC v11.6 Behavior on Design Migration

When you open the design in Libero SoC v11.6, the following message appears:

Info: Your design contains an FDDR. The DDR clock frequency parameter is not set; you must replace the FDDR with the latest version, re-generate the core and re-run the flow.

All design states are invalidated. If your design is a regular Smart Design based design (NOT a System Builder design) that uses FDDR, then the smart design component containing FDDR is invalidated. Libero requires you to upgrade the FDDR core to the latest version. Update the core (right-click core > Replace Instance Version) to continue. If you do not upgrade the core version, an error message appears in the Message Window when you regenerate using the old core version:

test_FDDR_0's core version is not supported by this version of the Libero SoC Software. To change the MSS version, select the component in the Design Hierarchy, right-click and choose "Replace Component Version".

If your design is a System Builder based design that includes FDDR, then the System Builder component is invalidated. Libero requires you to open the System Builder block and regenerate the design in System Builder.

User Follow-up Actions

Libero requires that you update the FDDR core (right-click core > Replace Instance Version) and regenerate the component and rerun the complete design flow.

If you've used System Builder in your design which includes the FDDR, System Builder automatically instantiates the latest version of the FDDR (automatic upgrade) to replace the old FDDR version when you regenerate the System Builder component.

Scenario #10 FDDR in M2S150/M2GL150 Devices

You open in Libero SoC v11.6 a project created in Libero SoC v11.5. The die used is M2S150 (SmartFusion2) or M2GL150 (IGLOO2) and your design contains an FDDR core v1.1.204/1.1.205.

Libero SoC v11.6 Behavior on Design Migration

Design flow is not invalidated. The component containing the FDDR core is not invalidated.

User Follow-up Actions

Do not continue with the design flow even though the design flow is not invalidated. The FDDR will not work with versions 1.1.204 or 1.1.205 because the FDDR PLL soft reset bit is incorrectly set to “1” in the configuration registers.

You must:

1. Upgrade the FDDRC core to the current version 1.1.301 (right-click core > Replace Instance Version)
2. Regenerate the Component that instantiates the FDDRC.
3. Rerun the design flow

Scenario #11 Design Component Contains Tamper/Tamper2 Core

In this scenario, your Libero SoC v11.5 design project contains the Tamper/Tamper2 core version v2.1.200. You open the design project in Libero SoC v11.6. The scenario refers to situations when the core is used alone in the Libero project to be migrated to Libero SoC v11.6. Existence of other cores (MSS/HPMS/MDDR/FDDR) in the design project may trigger different behaviors which may include invalidation of the design flow states or invalidation of the component containing the core.

Libero SoC v11.6 Behavior on Design Migration

The design flow and design components remain intact. No design state is invalidated. The design component which contains the Tamper/Tamper2 core is not invalidated. Libero does not require you to upgrade the Tamper/Tamper2 core to the current version (v2.1.300). An Info Icon appears at the top right corner of the Tamper/Tamper2 core to notify you that a newer version of the core exists in your vault.

User Follow-up Actions

You have two options:

- Continue with the design flow in Libero SoC v11.6 to generate programming files and Timing and Power Reports.
- Upgrade the Tamper/Tamper2 core (right-click core > Replace Instance Version) to the current version (v2.1.300) and regenerate the component. After the regeneration of the component, all design states are invalidated. You must rerun the complete design flow.

Scenario #12 Design Component Contains SimDRAM Core

In this scenario, you open in Libero SoC v11.6 a Libero SoC v11.5 design project which contains a SmartDesign testbench component that instantiates the SimDRAM core (v.1.0.100), which is a Microsemi simulation model for an external DDR memory.

Libero SoC v11.6 Behavior on Design Migration

When the project is opened in Libero SoC v11.6, no design states are invalidated and no component, including the SmartDesign Testbench component, is invalidated.

User Follow-up Actions

Libero requires that you upgrade the SimDRAM core (right-click core > Replace Instance Version) to the current version (v1.0.101) and then regenerate the SmartDesign Testbench.

If you regenerate the SmartDesign Testbench without first upgrading the SimDRAM core version, Libero gives the Error Mesage:

Generation of SmartDesign Testbench <Component_name> failed. See Mesage Window for details.

The message window tells you to upgrade the SimDRAM core first.

SimDRAM_0's core version is not supported by this version of Libero SoC software. To change the core version, select the core instance in SmartDesign, right-click and choose "Replace Core Version".

Scenario #13 MDDR/FDDR Driving External LPDDR Memory

When you open in Libero SoC v11.6 a project created by Libero SoC v11.5 (or earlier) release and the project contains an MDDR/FDDR driving an external LPDDR memory, the ODT (On-die Termination) setting for the LPDDR may not be in the lowest power setting after the design is migrated to Libero SoC v11.6. To ensure that you get the lowest possible power consumption for the LDPPDRL

1. Open the Configurator and import a register configuration file (MDDR/FDDR Configurator > Import Configuration) that contains the following register settings:
   - PHY_LOCAL_ODT_CR.REG_PHY_RD_LOCAL_ODT 0x0
   - PHY_LOCAL_ODT_CR.REG_PHY_WR_LOCAL_ODT 0x0
   - PHY_LOCAL_ODT_CR.REG_PHY_IDLE_LOCAL_ODT 0x0
2. Save the Configuration and regenerate the component.
3. Rerun the design flow.

4 – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,600 employees globally. Learn more at **www.microsemi.com**.

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