



Libero® SoC v2022.3

SmartFusion® 2 FPGA Fabric DDR Controller Configuration User Guide

Introduction

The SmartFusion® 2 FPGA has two embedded DDR controllers—one accessible via the MSS (MDDR) and the other intended for direct access from the FPGA Fabric (FDDR). The MDDR and FDDR both control off-chip DDR memories.

To fully configure the Fabric DDR controller, you must:

1. Use the Fabric External Memory DDR Controller Configurator to configure the DDR Controller, select its datapath bus interface (AXI or AHBLite), and select the DDR clock frequency as well as the fabric datapath clock frequency.
2. Set the register values for the DDR controller registers to match your external DDR memory characteristics.
3. Instantiate the Fabric DDR as part of a user application and make datapath connections.
4. Connect the DDR controller's APB configuration interface as defined by the Peripheral Initialization solution.

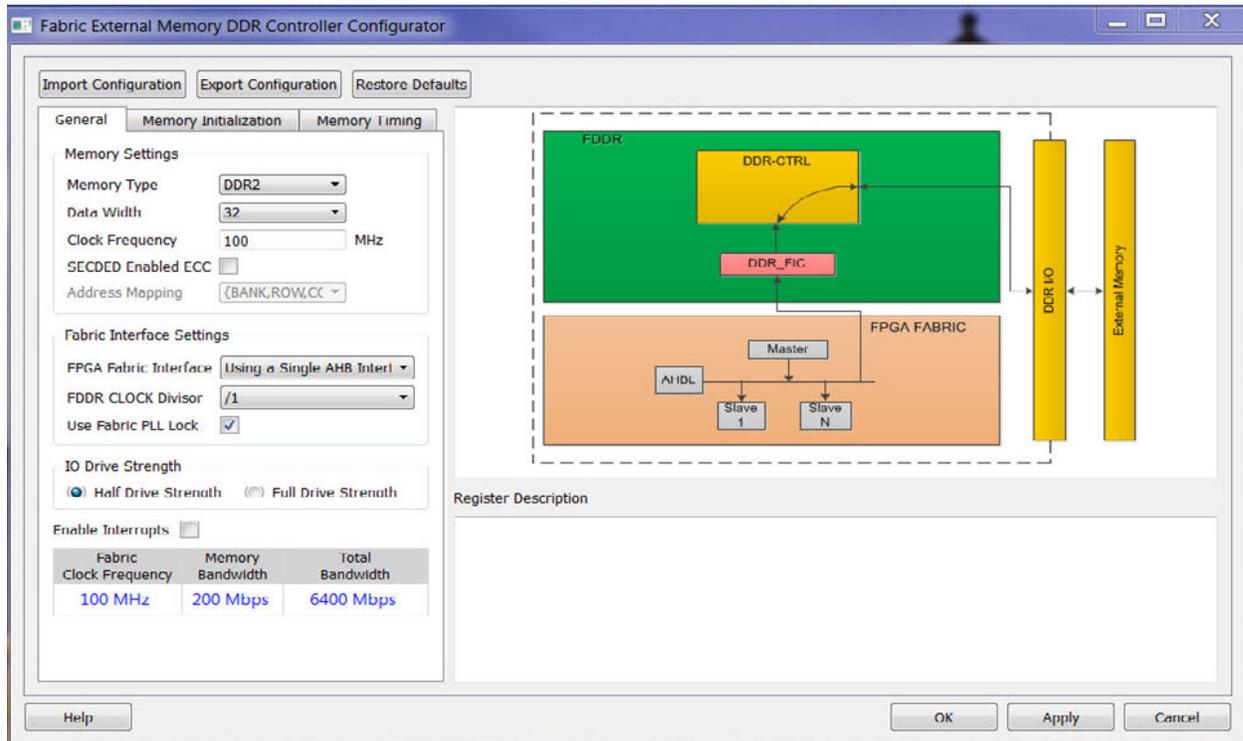
Table of Contents

Introduction.....	1
1. Fabric External Memory DDR Controller Configurator.....	3
1.1. Memory Settings.....	3
1.2. Fabric Interface Settings.....	3
2. FDDR Controller Configuration.....	6
2.1. Fabric DDR Control Registers.....	6
2.2. Fabric DDR Registers Configuration.....	6
2.3. Importing DDR Configuration Files.....	7
2.4. Exporting DDR Configuration Files.....	8
2.5. Firmware.....	8
2.6. Fabric DDR Configuration Path.....	9
3. Port Description.....	11
3.1. FDDR Core Ports.....	11
3.2. Interrupt Ports.....	11
3.3. APB3 Configuration Interface.....	11
3.4. DDR PHY Interface.....	12
3.5. AXI Bus Interface.....	13
3.6. AHB0 Bus Interface.....	14
3.7. AHB1 Bus Interface.....	15
4. Revision History.....	17
Microchip FPGA Support.....	18
Microchip Information.....	18
The Microchip Website.....	18
Product Change Notification Service.....	18
Customer Support.....	18
Microchip Devices Code Protection Feature.....	18
Legal Notice.....	19
Trademarks.....	19
Quality Management System.....	20
Worldwide Sales and Service.....	21

1. Fabric External Memory DDR Controller Configurator

The Fabric External Memory DDR (FDDR) Configurator is used to configure the overall datapath and the external DDR memory parameters for the Fabric DDR Controller. The following figure shows the configurator overview of FDDR.

Figure 1-1. FDDR Configurator Overview



1.1 Memory Settings

Use **Memory Settings** to configure your memory options in the MDDR.

- **Memory Type:** LPDDR, DDR2, or DDR3
- **Data Width:** 32-bit, 16-bit, or 8-bit
- **Clock Frequency:** Any value (Decimal/Fractional) in the range of 20 MHz to 333 MHz
- **SECEDED Enabled ECC:** ON or OFF
- **Address Mapping:** {ROW,BANK,COLUMN},{BANK,ROW,COLUMN}

1.2 Fabric Interface Settings

FPGA Fabric Interface

The FPGA Fabric interface is a data interface between the FDDR and the FPGA design. Because the FDDR is a memory controller, it is intended to be a target on an AXI or AHB bus. The Initiator of the bus initiates bus transactions, which are in turn interpreted by the FDDR as memory transactions and communicated to the off-chip DDR Memory. FDDR fabric interface has the following options:

- **Using an AXI-64 Interface:** One initiator accesses the FDDR through a 64-bit AXI interface.
- **Using a Single AHB-32 Interface:** One initiator accesses the FDDR through a single 32-bit AHB interface.
- **Using Two AHB-32 Interfaces:** Two masters access the FDDR using two 32-bit AHB interfaces.

FPGA CLOCK Divisor

Specifies the frequency ratio between the DDR Controller Clock (CLK_FDDR) and the clock controlling the fabric interface (CLK_FIC64). The CLK_FIC64 frequency must be equal to that of the AHB/AXI subsystem that is connected to the FDDR AHB/AXI bus interface. For example, if you have a DDR RAM running at 200 MHz and your Fabric/AXI Subsystem runs at 100 MHz, you must select a divisor of 2 (see the following figure).

Figure 1-2. Fabric Interface Settings - AXI Interface and FDDR Clock Divisor Agreement

The image shows a configuration window titled "Fabric Interface Settings". It contains three controls: a dropdown menu for "FPGA Fabric Interface" with the selected value "Using an AXI Interface", a dropdown menu for "FDDR CLOCK Divisor" with the selected value "/2", and a checkbox for "Use Fabric PLL Lock" which is currently unchecked.

Use Fabric PLL LOCK

If CLK_BASE is sourced from a Fabric CCC, you can connect the fabric CCC LOCK output to the FDDR FAB_PLL_LOCK input. CLK_BASE is not stable until the Fabric CCC locks. Therefore, Microchip recommends that you hold the FDDR in reset mode (that is, assert the CORE_RESET_N input) until CLK_BASE is stable. The LOCK output of the Fabric CCC indicates that the Fabric CCC output clocks are stable. By checking the Use FAB_PLL_LOCK option, you can expose the FAB_PLL_LOCK input port of the FDDR. You can then connect the LOCK output of the Fabric CCC to the FAB_PLL_LOCK input of the FDDR.

1.2.1 I/O Drive Strength

Select one of the following drive strengths for your DDR I/Os:

- Half Drive Strength
- Full Drive Strength

Depending on your DDR Memory type and the I/O Strength you select, Libero® SoC sets the DDR I/O Standard for your FDDR system as follows:

Table 1-1. IO Drive Strength

DDR Memory Type	Half Drive Strength	Full Drive Strength
DDR3	SSTL15I	SSTL15II
DDR2	SSTL18I	SSTL18II
LPDDR	LPDRI	LPDRII

1.2.2 Enable Interrupts

The FDDR is capable of raising interrupts when certain predefined conditions are satisfied. Check **Enable Interrupts** in the FDDR configurator if you would like to use these interrupts in your application. This exposes the interrupt signals on the FDDR instance. You can connect these interrupt signals as your design requires. The following Interrupt signals and their preconditions are available:

- **FIC_INT**: Generated when there is an error in the transaction between the Initiator and the FDDR.
- **IO_CAL_INT**: Enables you to recalibrate DDR I/Os by writing to DDR controller registers via the APB configuration interface. When calibration is complete, this interrupt is raised. For details about I/O recalibration, see the [SmartFusion2 SoC FPGA Documentation](#).
- **PLL_LOCK_INT**: Indicates that the FDDR FPLL has locked.
- **PLL_LOCKLOST_INT**: Indicates that the FDDR FPLL has lost lock.
- **FDDR_ECC_INT**: Indicates a single or two-bit error has been detected.

1.2.3 Fabric Clock Frequency

Clock frequency calculation based on your current Clock frequency and CLOCK divisor, displayed in MHz.

Fabric Clock Frequency (in MHz) = Clock Frequency / CLOCK divisor

1.2.4 Memory Bandwidth

Memory bandwidth calculation based on your current Clock Frequency value in Mbps.

Memory Bandwidth (in Mbps) = 2 * Clock Frequency

1.2.5 Total Bandwidth

Total bandwidth calculation based on your current Clock Frequency, Data Width, and CLOCK divisor in Mbps.

Total Bandwidth (in Mbps) = (2 * Clock Frequency * Data Width) / CLOCK Divisor

2. FDDR Controller Configuration

When you use the Fabric DDR Controller to access an external DDR Memory, the DDR Controller must be configured at runtime. This is done by writing configuration data to dedicated DDR controller configuration registers. This configuration data is dependent on the characteristics of the external DDR memory and your application. This section describes how to enter these configuration parameters in the FDDR controller configurator and how the configuration data is managed as part of the overall Peripheral Initialization solution. See the [SmartFusion2 DDR Controller and Serial High Speed Controller Standalone Initialization Methodology](#) for detailed information.

2.1 Fabric DDR Control Registers

The Fabric DDR Controller has a set of registers that need to be configured at runtime. The configuration values for these registers represent different parameters (for example, DDR mode, PHY width, burst mode, ECC, and so on). For details about the DDR controller configuration registers, see the [SmartFusion2 SoC FPGA Documentation](#).

2.2 Fabric DDR Registers Configuration

Use the **Memory Initialization** and **Memory Timing** tabs (as shown in the following figures) to enter parameters that correspond to your DDR Memory and application. Values you enter in these tabs are automatically translated to the appropriate register values. When you click a specific parameter, its corresponding register is described in the **Register Description Window**. See [Figure 1-1](#). The following figure shows the memory initialization window for FDDR Configurator.

Figure 2-1. FDDR Configuration - Memory Initialization

Parameter	Value	Unit
Burst Length	4	Bits
Burst Order	Sequential	
Timing Mode	1T	
CAS Latency	3	Clks
Self Refresh Enabled	NO	Bursts
Auto Refresh Burst Count	Single	
Powerdown Enabled	YES	
Stop the Clock	NO	
Deep Powerdown Enabled	NO	
Powerdown Entry Time	192	
Additive CAS Latency		Clks
CAS Write Latency	5	Clks
Zqinit	0	Clks
ZQCS	0	Clks
ZQCS Interval	0	Clks
Local ODT	Disable	
Drive Strength	Full	
Partial-Array Self Refresh	Quarter array	

Following figure shows the Memory timing tab for The FDDR configurator.

Figure 2-2. FDDR Configuration - Memory Timing Tab

Import Configuration Export Configuration Restore Defaults		
General Memory Initialization Memory Timing		
Time to Hold Reset before INIT	0	Clks
MRD	0	Clks
RAS (Min)	0	Clks
RAS (Max)	1024	Clks
RCD	0	Clks
RP	0	Clks
REFI	2624	Clks
RC	0	Clks
XP	0	Clks
CKE	0	Clks
RFC	35	Clks
WR	2	Clks
FAW	0	Clks
Time b/w RESET release and CKE assertion	67584	Clks

2.3 Importing DDR Configuration Files

In addition to entering DDR Memory parameters using the Memory Initialization and Timing tabs, you can import DDR register values from a file. To do so, click the **Import Configuration** button and navigate to the text file containing DDR register names and values. The following figure shows the import configuration syntax.

Figure 2-3. DDR Register Configuration File Syntax

```
ddrc_dyn_soft_reset_CR      0x00 ;
ddrc_dyn_refresh_1_CR      0x27DE ;
ddrc_dyn_refresh_2_CR      0x030F ;
ddrc_dyn_powerdown_CR      0x02 ;
ddrc_dyn_debug_CR          0x00 ;
ddrc_ecc_data_mask_CR      0x0000 ;
ddrc_addr_map_col_1_CR     0x3333 ;
ddrc_addr_map_col_3_CR     0x3300 ;
ddrc_init_1_CR             0x0001 ;
ddrc_cke_rstn_cycles_CR1   0x0100 ;
ddrc_cke_rstn_cycles_CR2   0x0008 ;
ddrc_init_emr2_CR          0x0000 ;
ddrc_init_emr3_CR          0x0000 ;
ddrc dram bank act timing CR 0x1947;
```



Important: If you choose to import register values rather than entering them using the GUI, you must specify all necessary register values. See [SmartFusion2 SoC FPGA Documentation](#) for details.

2.4 Exporting DDR Configuration Files

You can also export the current register configuration data into a text file. This file will contain register values that you imported (if any) as well as those that were computed from GUI parameters you entered in this dialog box.

If you want to undo changes you have made to the DDR register configuration, you can do so with restore default. This deletes all register configuration data, and you must either re-import or reenter this data. The data is reset to the hardware reset values.

2.4.1 Generated Data

Click **OK** to generate the configuration. Based on your input in the **General, Memory Timing and Memory Initialization** tabs, the FDDR Configurator computes values for all DDR configuration registers and exports these values into your firmware project and simulation files. The exported file syntax is shown in the following figure.

Figure 2-4. Exported DDR Register Configuration File Syntax

```
# Exported: 2013-Sep-02 05:07:16
# Libero DDR Configurator GUI Version = 2.0
# DDR Controller Type = DDR2
# Bus Width = 32-bits
# Memory Bandwidth = 200 Mbps
# Total Bandwidth = 6400 Mbps
#
# Validation Status:
# Target Device Manufacturer:
# Target Device:
#
# User Comments:
#
#
DDRC_ADDR_MAP_BANK_CR.REG_DDRC_ADDRMAP_BANK_B2      0xa
DDRC_ADDR_MAP_BANK_CR.REG_DDRC_ADDRMAP_BANK_B1      0xa
DDRC_ADDR_MAP_BANK_CR.REG_DDRC_ADDRMAP_BANK_B0      0xa
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B7       0x3
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B4       0x3
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B3       0x3
DDRC_ADDR_MAP_COL_1_CR.REG_DDRC_ADDRMAP_COL_B2       0x3
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B11      0xf
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B10      0xf
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B9       0xf
DDRC_ADDR_MAP_COL_2_CR.REG_DDRC_ADDRMAP_COL_B8       0x3
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_ADDRMAP_COL_B6       0x3
DDRC_ADDR_MAP_COL_3_CR.REG_DDRC_ADDRMAP_COL_B5       0x3
```

2.5 Firmware

When you generate the SmartDesign, the following files are generated in the `<project_dir>/firmware/drivers_config/sys_config` directory. These files are required for the CMSIS firmware core to compile properly and contain information regarding your current design, including peripheral configuration data and clock configuration information for the MSS. Do not edit these files manually, as they are recreated every time your root design is regenerated.

- `sys_config.c`
- `sys_config.h`
- `sys_config_mddr_define.h`: MDDR configuration data.
- `sys_config_fddr_define.h`: FDDR configuration data.
- `sys_config_mss_clocks.h`: MSS clocks configuration

Simulation

When you generate the SmartDesign associated with your MSS, the following simulation files are generated in the `<project dir>/simulation` directory:

test.bfm	Top-level BFM file that is first executed during any simulation that exercises the SmartFusion 2 MSS Arm® Cortex®-M3 processor. It executes <code>peripheral_init.bfm</code> and <code>user.bfm</code> , in that order
peripheral_init.bfm	Contains the BFM procedure that emulates the <code>CMSIS::SystemInit()</code> function run on the Cortex-M3 before you enter the <code>main()</code> procedure. It copies the configuration data for any peripheral used in the design to the correct peripheral configuration registers and then waits for all the peripherals to be ready before asserting that the user can use these peripherals.
FDDR_init.bfm	Contains BFM write commands that simulate writes of the Fabric DDR Configuration register data you entered (using the Edit Registers dialog box) into the DDR Controller registers.
user.bfm	Intended for user commands. You can simulate the datapath by adding your own BFM commands in this file. Commands in this file will be executed after <code>peripheral_init.bfm</code> has completed.

Using the preceded files, the configuration path is simulated automatically. You only need to edit the `user.bfm` file to simulate the datapath. Do not edit the `test.bfm`, `peripheral_init.bfm`, or `MDDR_init.bfm` files as these files are recreated every time your root design is regenerated.

2.6 Fabric DDR Configuration Path

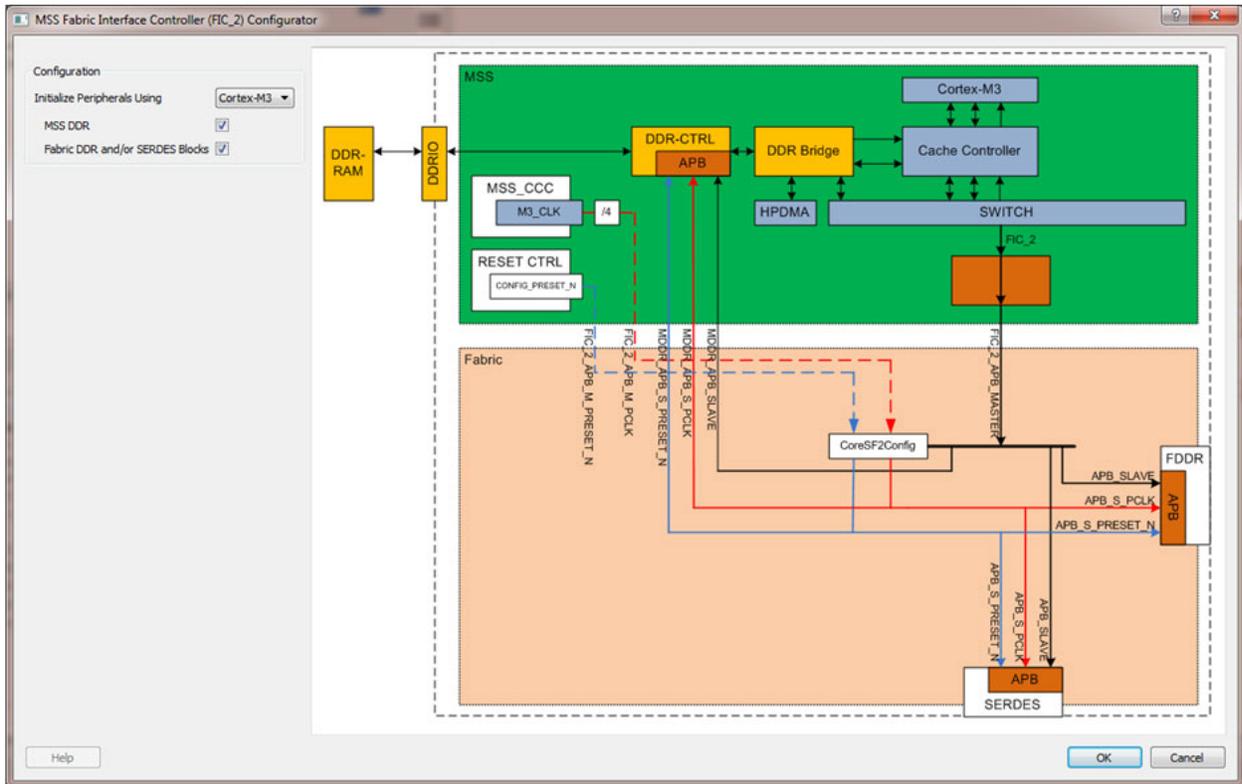
The Peripheral Initialization solution requires that, in addition to specifying Fabric DDR Configuration register values, you configure the APB configuration data path in the MSS (FIC_2). The `SystemInit()` function writes the data to the FDDR configuration registers via the FIC_2 APB interface.



Important: If you are using System Builder, the configuration path is set and connected automatically.

The following figure shows the overview of the FIC_2 Configurator.

Figure 2-5. FIC_2 Configurator Overview

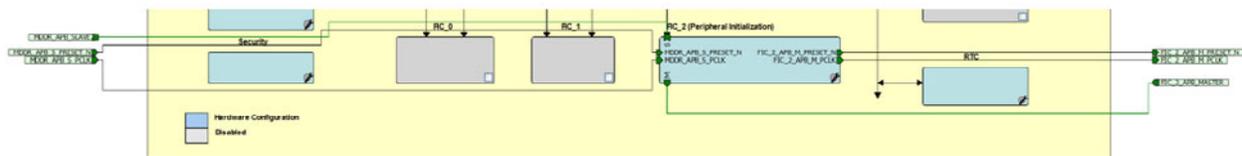


To configure the FIC_2 interface:

1. Open the FIC_2 configurator dialog (as shown in the preceded figure) from the MSS configurator.
2. Select the **Initialize peripherals using Cortex-M3** option.
3. Make sure that the MSS DDR is selected, as are the Fabric DDR/SERDES blocks if you are using them.
4. Click **OK** to save your settings. This exposes the FIC_2 configuration ports (Clock, Reset, and APB bus interfaces), as shown in the following figure.
5. Generate the MSS. The FIC_2 ports (FIC_2_APB_MASTER, FIC_2_APB_M_PCLK, and FIC_2_APB_M_RESET_N) are now exposed at the MSS interface and can be connected to CoreSF2Config and CoreSF2Reset as per the Peripheral Initialization solution specification.

For details on configuring and connecting the CoreSF2Config and CoreSF2Reset cores, see the Peripheral Initialization Configuration Guide. The following figure shows the FIC_2 Ports.

Figure 2-6. FIC_2 Ports



3. Port Description

The following section lists the ports details.

3.1 FDDR Core Ports

The FDDR core ports signals are listed in the following table.

Table 3-1. FDDR Core Ports

Port Name	Direction	Description
CORE_RESET_N	IN	FDDR Controller Reset
CLK_BASE	IN	FDDR Fabric Interface Clock
FPLL_LOCK	OUT	FDDR PLL Lock output - high when FDDR PLL is locked
CLK_BASE_PLL_LOCK	IN	Fabric PLL Lock Input. This input is exposed only when the Use FAB_PLL_LOCK option is selected.

3.2 Interrupt Ports

This group of ports is exposed when you select the Enable Interrupts option.

Table 3-2. Interrupt Ports

Port Name	Direction	Description
PLL_LOCK_INT	OUT	Asserts when FDDR PLL locks.
PLL_LOCKLOST_INT	OUT	Asserts when FDDR PLL lock is lost.
ECC_INT	OUT	Asserts when an ECC Event occurs.
IO_CALIB_INT	OUT	Asserts when I/O calibration is complete.
FIC_INT	OUT	Asserts when there is an error in the AHB/AXI protocol on the Fabric interface.

3.3 APB3 Configuration Interface

The APB3 configuration interface ports signals are listed in the following table.

Table 3-3. APB3 Configuration Interface

Port Name	Direction	Description
APB_S_PENABLE	IN	Target Enable
APB_S_PSEL	IN	Target Select
APB_S_PWRITE	IN	Write Enable
APB_S_PADDR[10:2]	IN	Address
APB_S_PWDATA[15:0]	IN	Write Data

.....continued

Port Name	Direction	Description
APB_S_PREADY	OUT	Target Ready
APB_S_PSLVERR	OUT	Target Error
APB_S_PRDATA[15:0]	OUT	Read Data
APB_S_PRESET_N	IN	Target Reset
APB_S_PCLK	IN	Clock

3.4 DDR PHY Interface

The DDR PHY interface signals are listed in the following table.

Table 3-4. DDR PHY Interface

Port Name	Direction	Description
FDDR_CAS_N	OUT	DRAM CASN
FDDR_CKE	OUT	DRAM CKE
FDDR_CLK	OUT	Clock, P side
FDDR_CLK_N	OUT	Clock, N side
FDDR_CS_N	OUT	DRAM CSN
FDDR_ODT	OUT	DRAM ODT
FDDR_RAS_N	OUT	DRAM RASN
FDDR_RESET_N	OUT	DRAM Reset for DDR3
FDDR_WE_N	OUT	DRAM WEN
FDDR_ADDR[15:0]	OUT	Dram Address bits
FDDR_BA[2:0]	OUT	Dram Bank Address
FDDR_DM_RDQS[4:0]	INOUT	Dram Data Mask
FDDR_DQS[4:0]	INOUT	Dram Data Strobe Input/Output - P Side
FDDR_DQS_N[4:0]	INOUT	Dram Data Strobe Input/Output - N Side
FDDR_DQ[35:0]	INOUT	DRAM Data Input/Output
FDDR_FIFO_WE_IN[2:0]	IN	FIFO in signal
FDDR_FIFO_WE_OUT[2:0]	OUT	FIFO out signal
FDDR_DM_RDQS ([3:0]/[1:0]/[0])	INOUT	Dram Data Mask
FDDR_DQS ([3:0]/[1:0]/[0])	INOUT	Dram Data Strobe Input/Output - P Side
FDDR_DQS_N ([3:0]/[1:0]/[0])	INOUT	Dram Data Strobe Input/Output - N Side
FDDR_DQ ([31:0]/[15:0]/[7:0])	INOUT	DRAM Data Input/Output
FDDR_DQS_TMATCH_0_IN	IN	FIFO in signal

.....continued

Port Name	Direction	Description
FDDR_DQS_TMATCH_0_OUT	OUT	FIFO out signal
FDDR_DQS_TMATCH_1_IN	IN	FIFO in signal (32-bit only)
FDDR_DQS_TMATCH_1_OUT	OUT	FIFO out signal (32-bit only)
FDDR_DM_RDQS_ECC	INOUT	Dram ECC Data Mask
FDDR_DQS_ECC	INOUT	Dram ECC Data Strobe Input/Output - P Side
FDDR_DQS_ECC_N	INOUT	Dram ECC Data Strobe Input/Output - N Side
FDDR_DQ_ECC ([3:0]/[1:0]/[0])	INOUT	DRAM ECC Data Input/Output
FDDR_DQS_TMATCH_ECC_IN	IN	ECC FIFO in signal
FDDR_DQS_TMATCH_ECC_OUT	OUT	ECC FIFO out signal (32-bit only)



Important: Port widths for some ports change depending on the selection of the PHY width. The notation "[a:0]/ [b:0]/[c:0]" is used to denote such ports, where "[a:0]" refers to the port width when a 32-bit PHY width is selected, "[b:0]" corresponds to a 16-bit PHY width, and "[c:0]" corresponds to an 8-bit PHY width.

3.5 AXI Bus Interface

The AXI Bus interface ports signals are listed in the following table.

Table 3-5. AXI Bus Interface

Port Name	Direction	Description
AXI_S_AWREADY	OUT	Write address ready
AXI_S_WREADY	OUT	Write address ready
AXI_S_BID[3:0]	OUT	Response ID
AXI_S_BRESP[1:0]	OUT	Write response
AXI_S_BVALID	OUT	Write response valid
AXI_S_ARREADY	OUT	Read address ready
AXI_S_RID[3:0]	OUT	Read ID Tag
AXI_S_RRESP[1:0]	OUT	Read Response
AXI_S_RDATA[63:0]	OUT	Read data
AXI_S_RLAST	OUT	Read Last - This signal indicates the last transfer in a read burst.
AXI_S_RVALID	OUT	Read address valid
AXI_S_AWID[3:0]	IN	Write Address ID
AXI_S_AWADDR[31:0]	IN	Write address
AXI_S_AWLEN[3:0]	IN	Burst length
AXI_S_AWSIZE[1:0]	IN	Burst size

.....continued		
Port Name	Direction	Description
AXI_S_AWBURST[1:0]	IN	Burst type
AXI_S_AWLOCK[1:0]	IN	Lock type - This signal provides additional information about the atomic characteristics of the transfer.
AXI_S_AWVALID	IN	Write address valid
AXI_S_WID[3:0]	IN	Write Data ID tag
AXI_S_WDATA[63:0]	IN	Write data
AXI_S_WSTRB[7:0]	IN	Write strobes
AXI_S_WLAST	IN	Write last
AXI_S_WVALID	IN	Write valid
AXI_S_BREADY	IN	Write ready
AXI_S_ARID[3:0]	IN	Read Address ID
AXI_S_ARADDR[31:0]	IN	Read address
AXI_S_ARLEN[3:0]	IN	Burst length
AXI_S_ARSIZE[1:0]	IN	Burst size
AXI_S_ARBURST[1:0]	IN	Burst type
AXI_S_ARLOCK[1:0]	IN	Lock Type
AXI_S_ARVALID	IN	Read address valid
AXI_S_RREADY	IN	Read address ready
AXI_S_CORE_RESET_N	IN	MDDR Global Reset
AXI_S_RMW	IN	Indicates whether all bytes of a 64-bit lane are valid for all beats of an AXI transfer. 0: Indicates that all bytes in all beats are valid in the burst and the controller must default to write commands. 1: Indicates that some bytes are invalid and the controller must default to RMW commands. This is classed as an AXI write address channel sideband signal and is valid with the AWVALID signal. Only used when ECC is enabled.

3.6 AHB0 Bus Interface

The AHB0 bus interface port signals are listed in the following table.

Table 3-6. AHB0 Bus Interface

Port Name	Direction	Description
AHB0_S_HREADYOUT	OUT	AHBL target ready - When high for a write indicates the target is ready to accept data and when high for a read indicates that data is valid.
AHB0_S_HRESP	OUT	AHBL response status - When driven high at the end of a transaction indicates that the transaction has completed with errors. When driven low at the end of a transaction indicates that the transaction has completed successfully.
AHB0_S_HRDATA[31:0]	OUT	AHBL read data - Read data from the target to the initiator
AHB0_S_HSEL	IN	AHBL target select - When asserted, the target is the currently selected AHBL target on the AHB bus.
AHB0_S_HADDR[31:0]	IN	AHBL address - byte address on the AHBL interface
AHB0_S_HBURST[2:0]	IN	AHBL Burst Length
AHB0_S_HSIZE[1:0]	IN	AHBL transfer size - Indicates the size of the current transfer (8/16/32 byte transactions only)
AHB0_S_HTRANS[1:0]	IN	AHBL transfer type - Indicates the transfer type of the current transaction.
AHB0_S_HMASTLOCK	IN	AHBL lock - When asserted the current transfer is part of a locked transaction.
AHB0_S_HWRITE	IN	AHBL write - When high indicates that the current transaction is a write. When low indicates that the current transaction is a read.
AHB0_S_HREADY	IN	AHBL ready - When high, indicates that the target is ready to accept a new transaction.
AHB0_S_HWDATA[31:0]	IN	AHBL write data - Write data from the initiator to the target

3.7 AHB1 Bus Interface

The AHB1 bus interface port signals are listed in the following table.

Table 3-7. AHB1 Bus Interface

Port Name	Direction	Description
AHB1_S_HREADYOUT	OUT	AHBL target ready - When high for a write, indicates the target is ready to accept data, and when high for a read, indicates that data is valid.
AHB1_S_HRESP	OUT	AHBL response status - When driven high at the end of a transaction indicates that the transaction has completed with errors. When driven low at the end of a transaction, indicates that the transaction has completed successfully.
AHB1_S_HRDATA[31:0]	OUT	AHBL read data - Read data from the target to the initiator
AHB1_S_HSEL	IN	AHBL target select - When asserted, the target is the currently selected AHBL target on the AHB bus.
AHB1_S_HADDR[31:0]	IN	AHBL address - byte address on the AHBL interface
AHB1_S_HBURST[2:0]	IN	AHBL Burst Length
AHB1_S_HSIZE[1:0]	IN	AHBL transfer size - Indicates the size of the current transfer (8/16/32 byte transactions only).
AHB1_S_HTRANS[1:0]	IN	AHBL transfer type - Indicates the transfer type of the current transaction.
AHB1_S_HMASTLOCK	IN	AHBL lock - When asserted, the current transfer is part of a locked transaction.
AHB1_S_HWRITE	IN	AHBL write - When high, indicates that the current transaction is a write. When low, indicates that the current transaction is a read.
AHB1_S_HREADY	IN	AHBL ready - When high, indicates that the target is ready to accept a new transaction.
AHB1_S_HWDATA[31:0]	IN	AHBL write data - Write data from the initiator to the target

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	12/2022	The following is the list of changes in revision A of the document: <ul style="list-style-type: none">• The document was migrated to the Microchip template.• The document number was updated to DS50003443A from 50200382.• Updated: Figure 2-1 and Figure 2-2.

Microchip FPGA Support

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