Total Ionizing Dose Test Report

No. 14T-RTSX72SU-CQ256-D6AA61

May 28, 2014

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO2)
2. Power Supply Current (ICCA/ICCI)	Passed 40 krad (SiO2)
3. Input Threshold (VIL/VIH)	Passed 100 krad (SiO2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO2)
5. Propagation Delay	Passed 100 krad (SiO2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a resistor; during annealing each input or output is grounded through a 1K Ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D6AA61
Quantity Tested	6
Serial Number	40 krad(SiO2): 14643, 14649 60 krad(SiO2): 14661, 14665 100 krad(SiO2): 14667, 14860
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

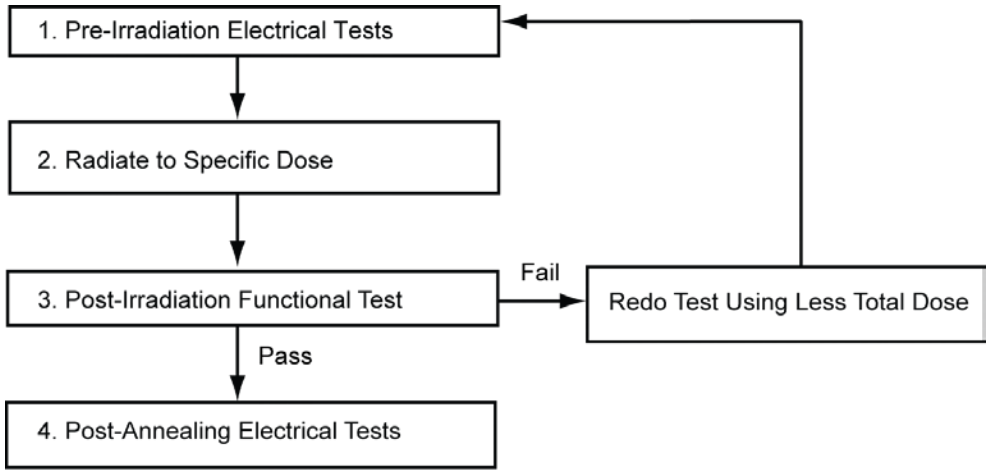


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging or rebound test mentioned in TM1019.8 is unnecessary, because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VTIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at CLOCK input to the time of switching state at output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2.ICC (ICCA/ICCI)	DUT power supply
3.Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4.Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5.Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
14643	40 krad	1.28	3	2	0.73	1	4
14649	40 krad	1.32	3	2	0.74	1	2
14661	60 krad	1.31	23	22	0.74	27	38
14665	60 krad	1.32	22	24	0.73	26	32
14667	100 krad	1.29	294	194	0.74	214	69
14860	100 krad	1.24	274	206	0.73	210	79

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI is 25 mA in the RTSXSU spec sheet.

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT.

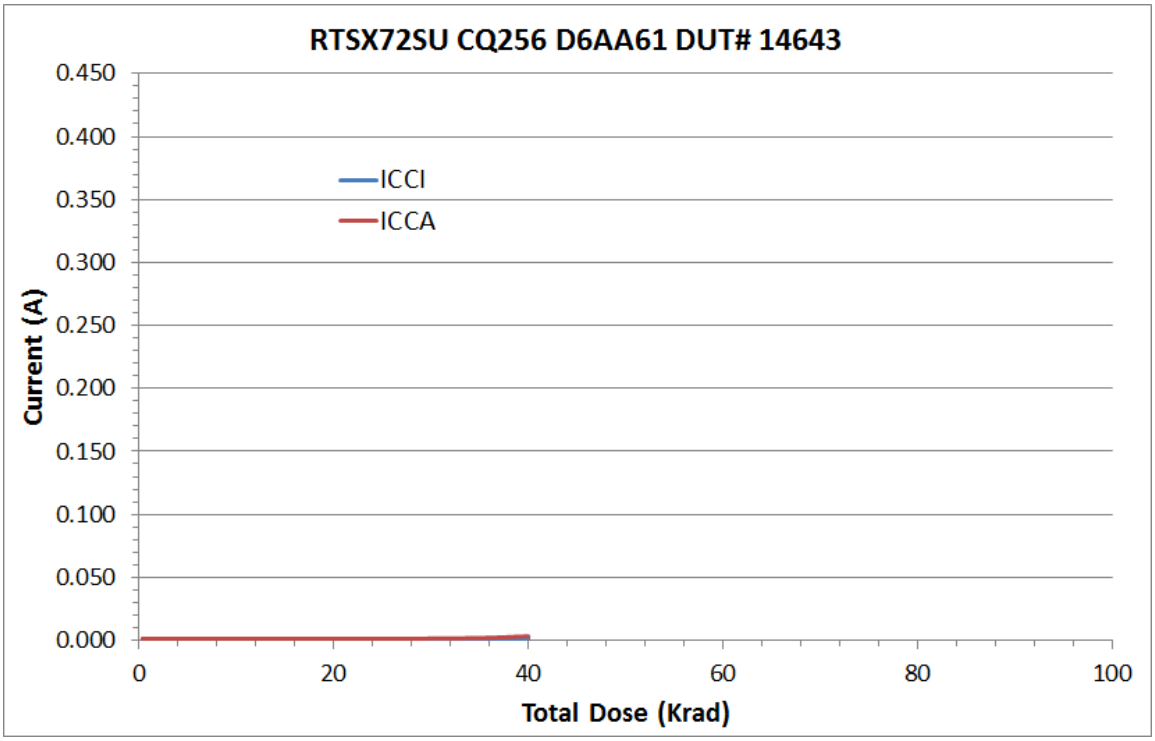


Figure 2 DUT 14643 Influx ICCA and ICCI

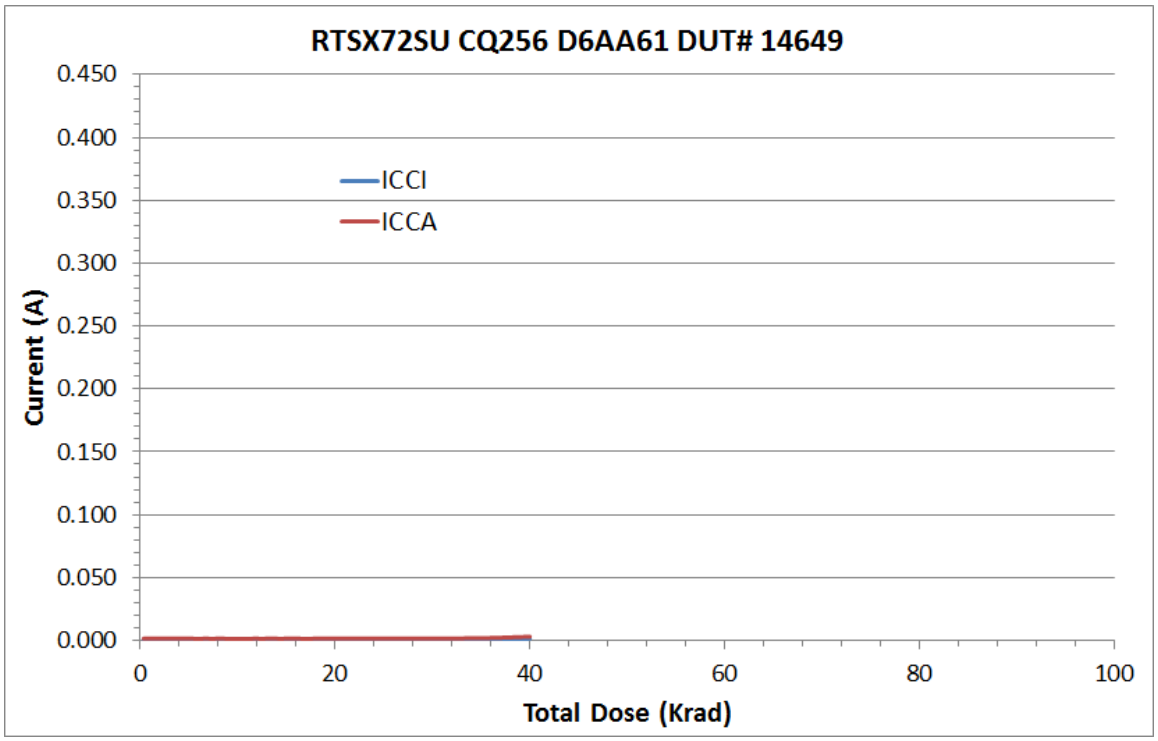


Figure 3 DUT 14649 Influx ICCA and ICCI

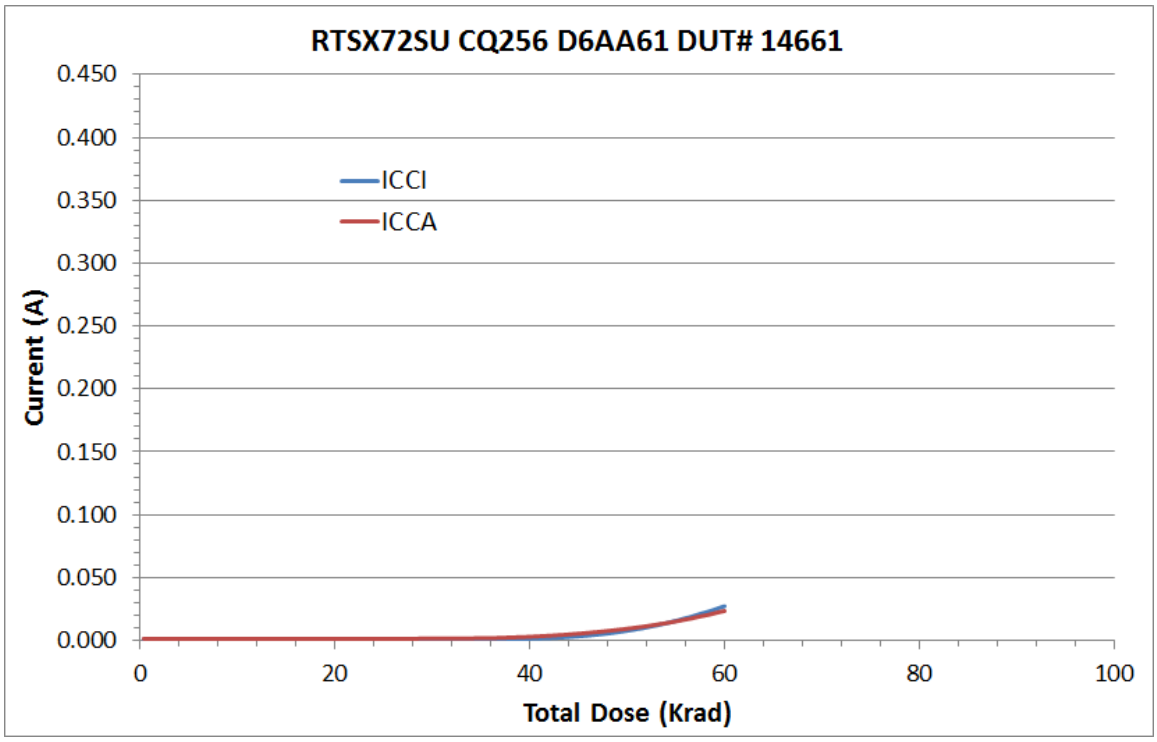


Figure 4 DUT 14661 Influx ICCA and ICCI

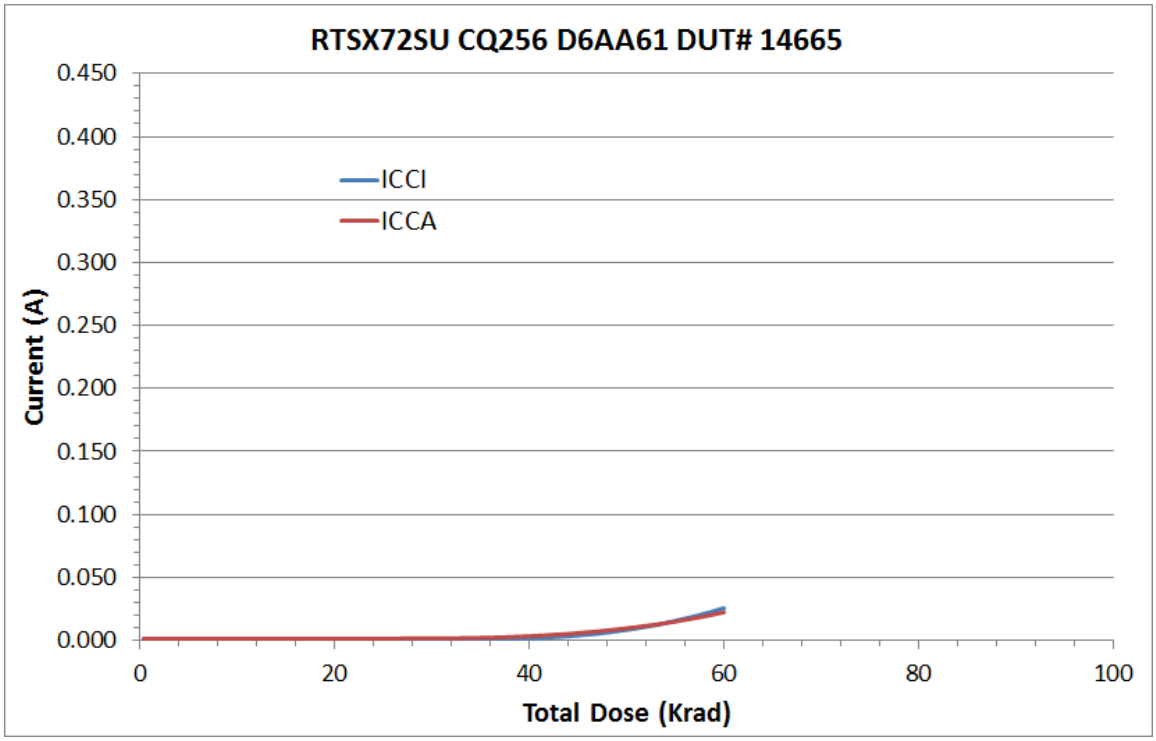


Figure 5 DUT 14665 Influx ICCA and ICCI

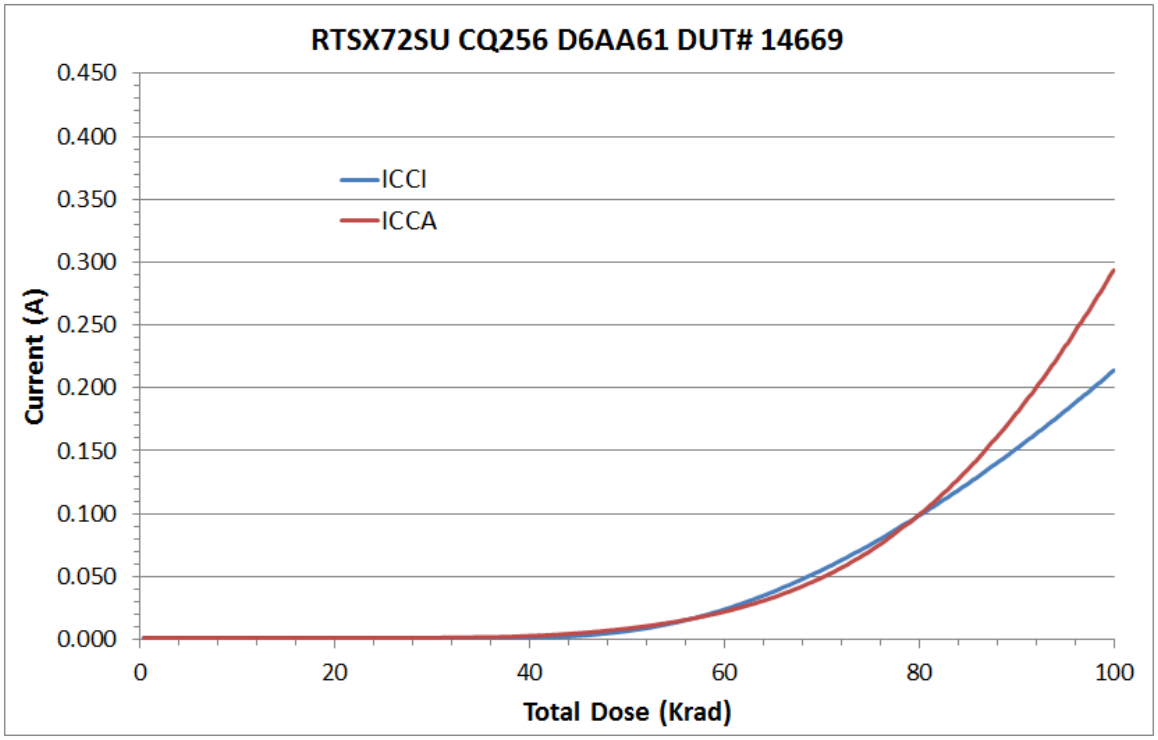


Figure 6 DUT 14667 Influx ICCA and ICCI

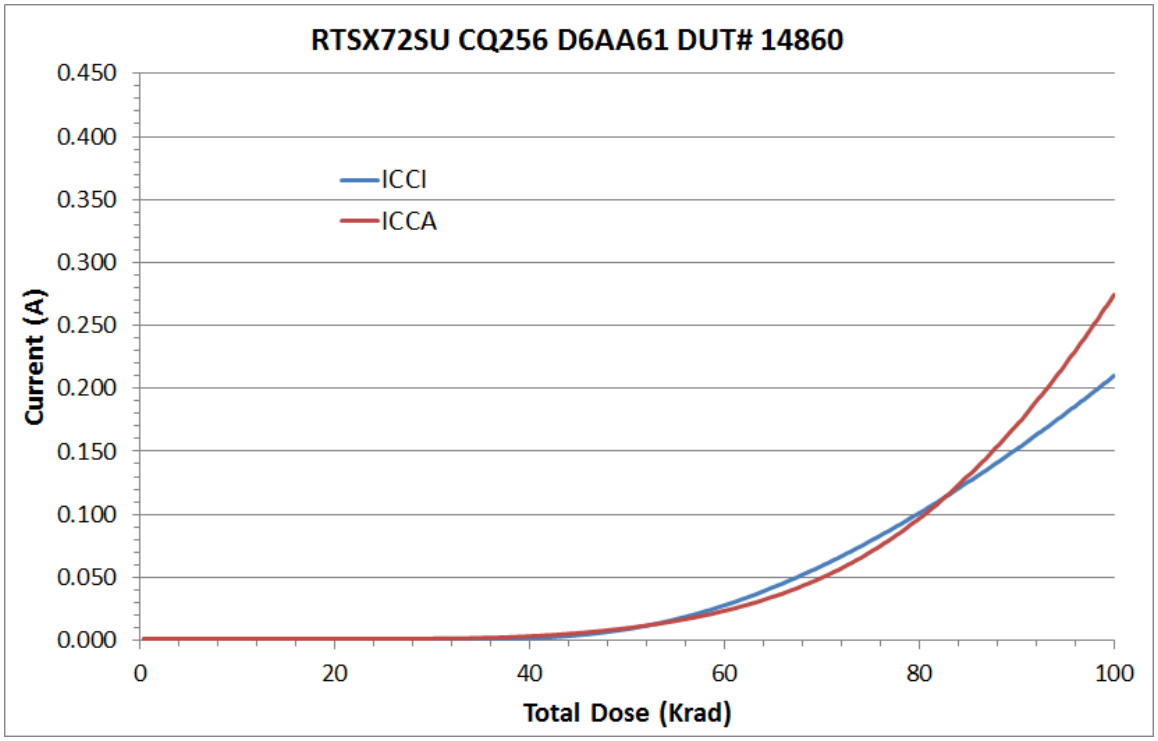


Figure 7 DUT 14860 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds.

Some parameters of certain samples show more post-annealing shift, which could be caused by measurement sensitivity from the setup, as no obvious dose dependence is seen.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	14643 (40 krad)				14649 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1130	1510	1250	1460	1130	1390	1265	1465
DAH/QA0H	1395	1400	1455	1455	1395	1400	1470	1460
ENCNTRH/YO0H	1440	1430	1450	1435	1440	1425	1430	1435
IDII0/IDIO0	1375	1445	1395	1470	1375	1440	1410	1475
IDII1/IDIO1	1400	1435	1395	1425	1475	1425	1385	1425
IDII2/IDIO2	1235	1385	1375	1420	1420	1380	1255	1400
IDII3/IDIO3	1465	1400	1470	1405	1460	1400	1470	1410
IDII4/IDIO4	1425	1415	1425	1375	1425	1370	1435	1380
IDII5/IDIO5	1340	1420	1240	1435	1335	1420	1245	1440
IDII6/IDIO6	1380	1380	1430	1420	1425	1375	1440	1420
IDII7/IDIO7	1415	1405	1440	1490	1445	1400	1460	1460

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	14661 (60 krad)				14665 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1125	1525	1220	1445	1135	1510	1235	1450
DAH/QA0H	1425	1425	1445	1425	1410	1405	1450	1410
ENCNTRH/YO0H	1440	1425	1420	1420	1450	1430	1425	1420
IDII0/IDIO0	1380	1425	1430	1430	1375	1425	1385	1440
IDII1/IDIO1	1435	1415	1470	1415	1475	1410	1475	1415
IDII2/IDIO2	1245	1380	1320	1380	1240	1380	1290	1390
IDII3/IDIO3	1470	1400	1460	1395	1465	1405	1465	1400
IDII4/IDIO4	1435	1410	1405	1360	1425	1405	1305	1415
IDII5/IDIO5	1370	1480	1315	1395	1365	1395	1355	1390
IDII6/IDIO6	1420	1380	1410	1375	1370	1375	1365	1370
IDII7/IDIO7	1405	1395	1415	1390	1415	1430	1425	1395

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	14667 (100 krad)				14860 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1125	1545	1215	1435	1115	1515	1225	1415
DAH/QA0H	1410	1420	1430	1395	1385	1395	1405	1405
ENCNTRH/YO0H	1440	1425	1425	1415	1420	1410	1405	1390
IDII0/IDIO0	1385	1445	1425	1430	1355	1430	1405	1405
IDII1/IDIO1	1470	1430	1460	1400	1460	1420	1445	1385
IDII2/IDIO2	1230	1375	1430	1420	1225	1370	1300	1365
IDII3/IDIO3	1460	1390	1450	1385	1450	1380	1440	1370
IDII4/IDIO4	1430	1370	1405	1360	1415	1400	1240	1330
IDII5/IDIO5	1335	1420	1250	1405	1325	1400	1255	1375
IDII6/IDIO6	1385	1380	1395	1385	1385	1365	1380	1345
IDII7/IDIO7	1440	1385	1425	1385	1395	1450	1350	1450

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	14643 (40 krad)		14649 (40 krad)		14661 (60 krad)		14665 (60 krad)		14667 (100 krad)		14860 (100 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	10	10	10	10	10	10	10	10	10	10	10	10
12 mA	120	121	119	119	119	118	120	120	120	119	118	118
20 mA	201	201	199	199	197	197	200	200	199	199	196	196
50 mA	505	506	499	500	496	496	503	502	500	501	493	493
100 mA	1031	1033	1020	1022	1013	1013	1027	1027	1021	1023	1008	1008

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	14643 (40 krad)		14649 (40 krad)		14661 (60 krad)		14665 (60 krad)		14667 (100 krad)		14860 (100 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4978	4978	4978	4978	4979	4974	4979	4977	4979	4976	4978	4975
8 mA	4844	4842	4845	4843	4846	4840	4846	4843	4846	4840	4845	4840
20 mA	4608	4605	4612	4608	4613	4605	4612	4607	4612	4603	4612	4602
50 mA	3970	3959	3979	3968	3984	3967	3981	3969	3979	3957	3979	3956
100 mA	2519	2478	2545	2505	2558	2509	2553	2508	2552	2458	2527	2432

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion; take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Anneal (µs)	Degradation (%)
14643	40 krad	1.36	1.36	0.00%
14649	40 krad	1.38	1.39	0.73%
14661	60 krad	1.33	1.34	0.75%
14665	60 krad	1.34	1.34	0.37%
14667	100 krad	1.38	1.42	2.90%
14860	100 krad	1.34	1.38	2.99%

F. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

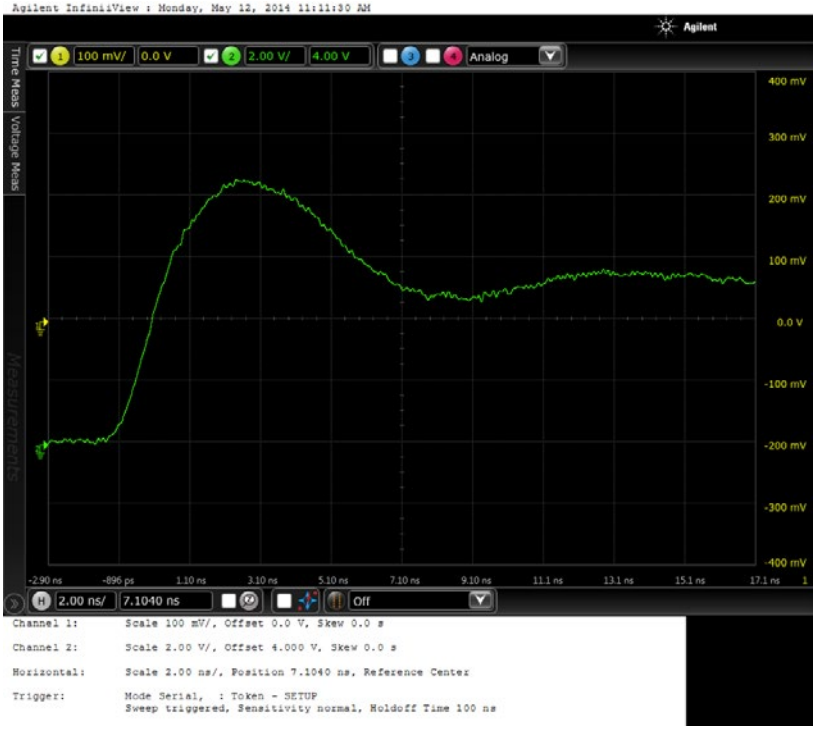


Figure 9a DUT 14643 Pre-Irradiation Rising Edge

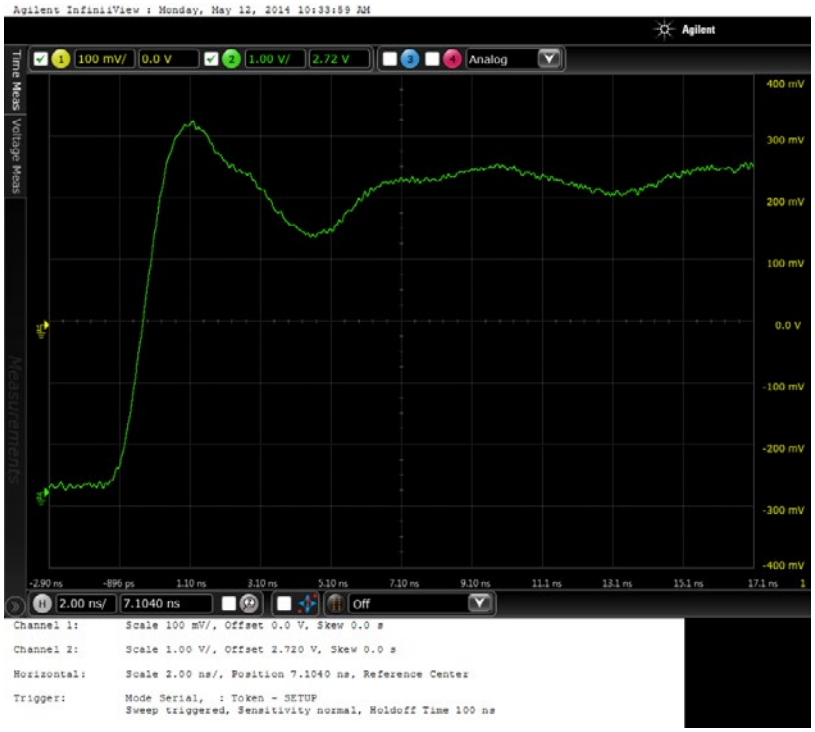


Figure 9b DUT 14643 Post-Annealing Rising Edge

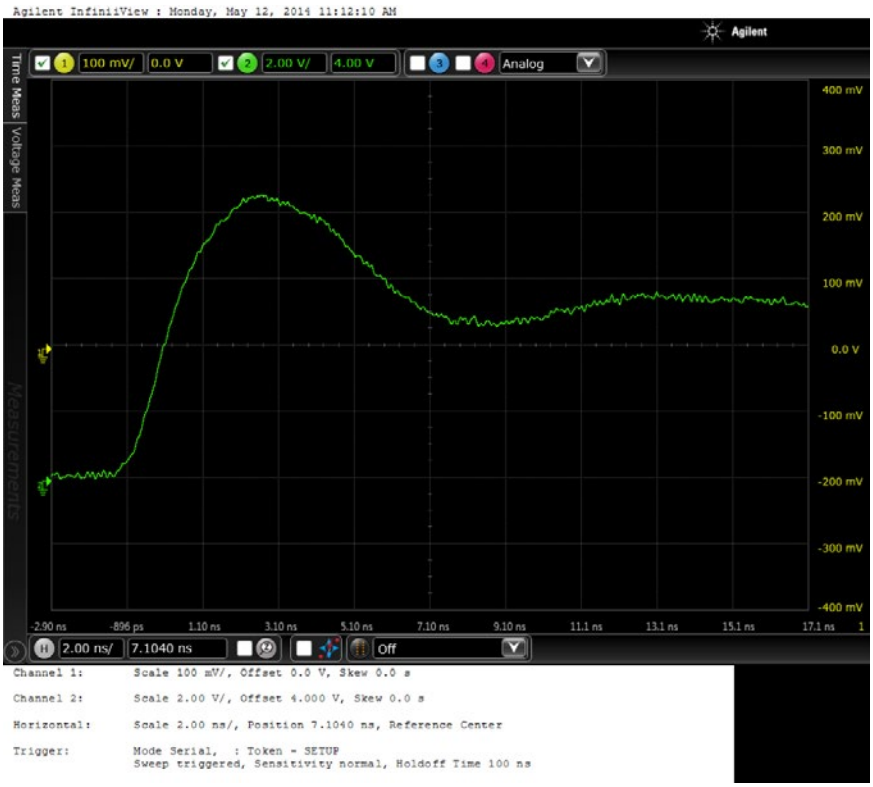


Figure 10a DUT 14649 Pre-Irradiation Rising Edge

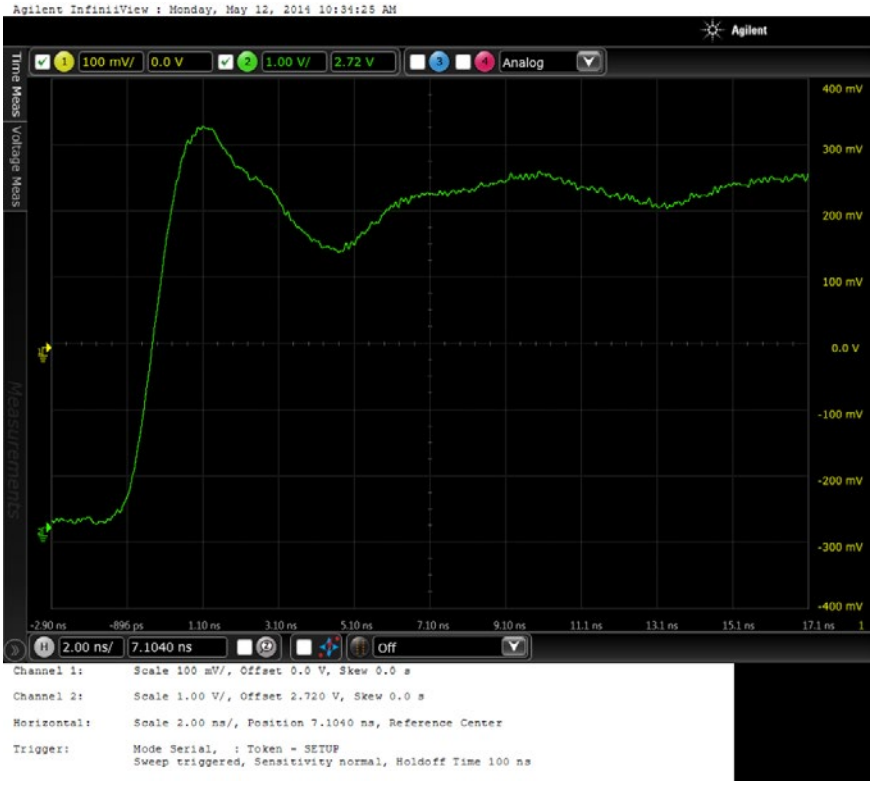


Figure 10b DUT 14649 Post-Annealing Rising Edge

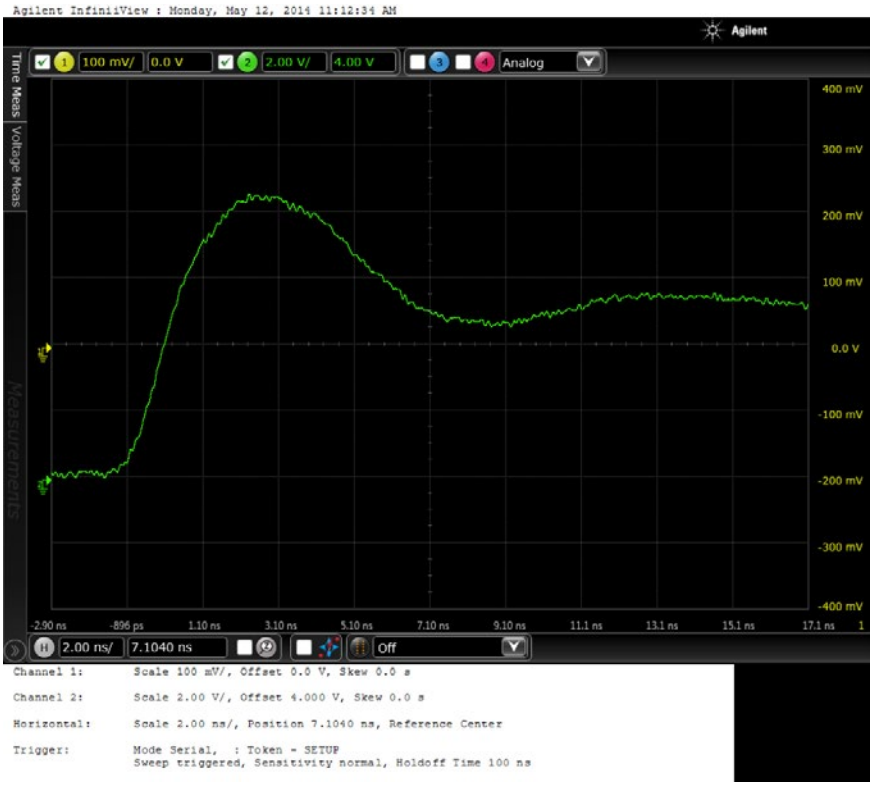


Figure 11a DUT 14661 Pre-Radiation Rising Edge

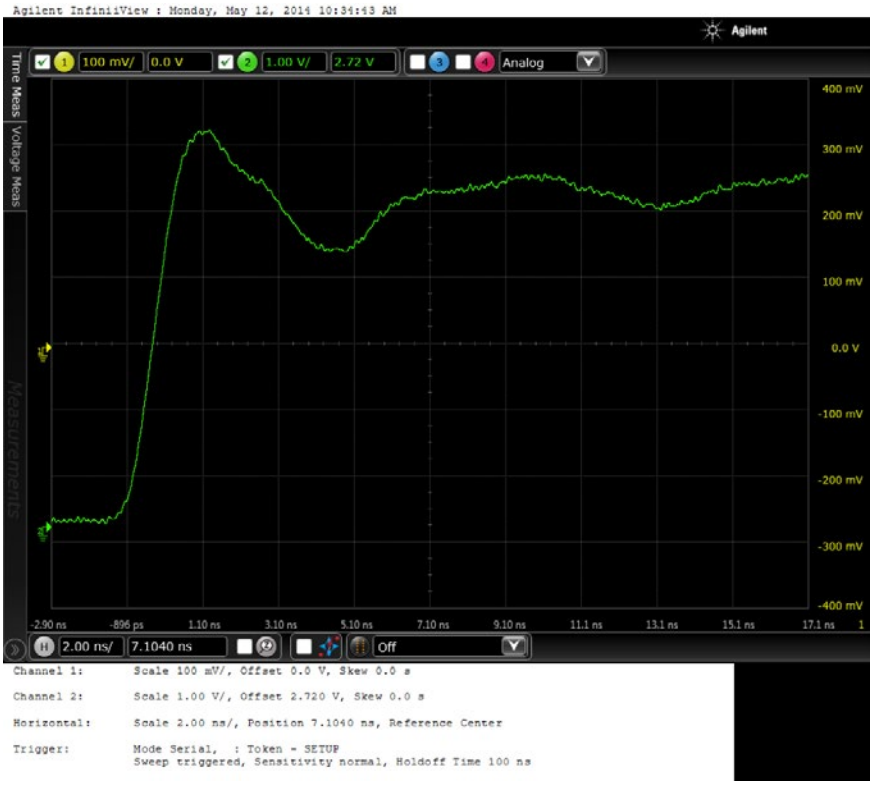


Figure 11b DUT 14661 Post-Annealing Rising Edge

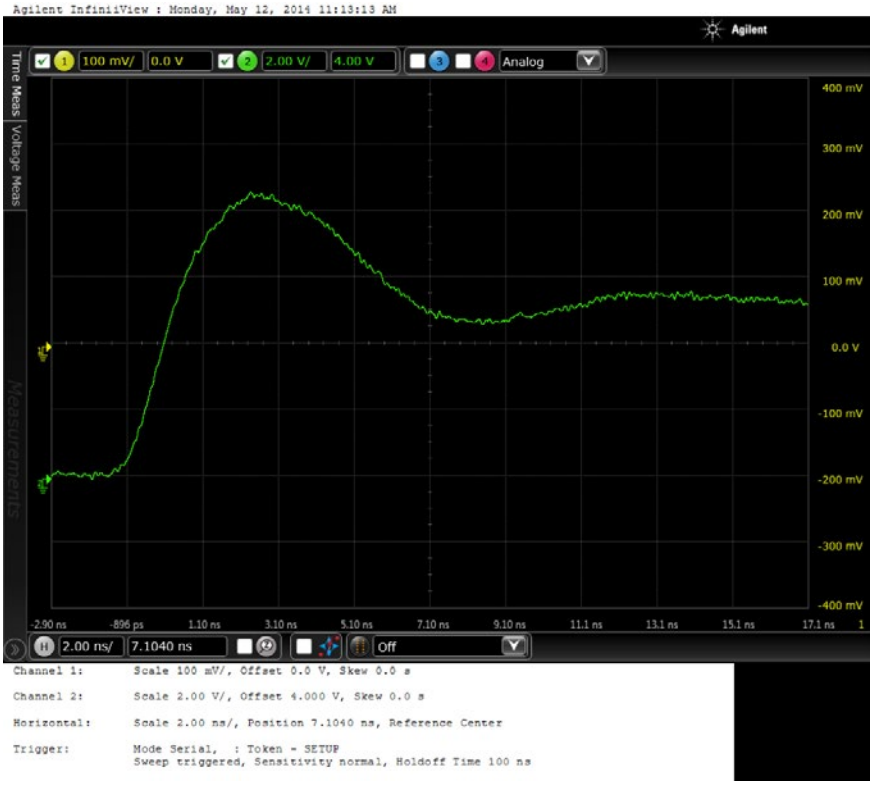


Figure 12a DUT 14665 Pre-Irradiation Rising Edge

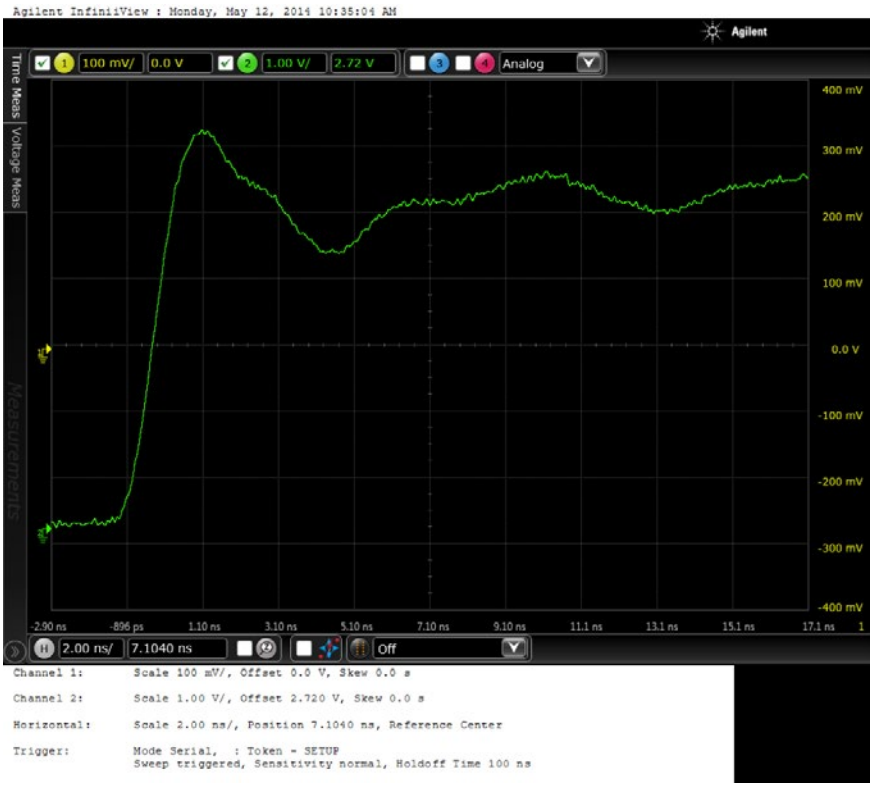


Figure 12b DUT 14665 Post-Annealing Rising Edge

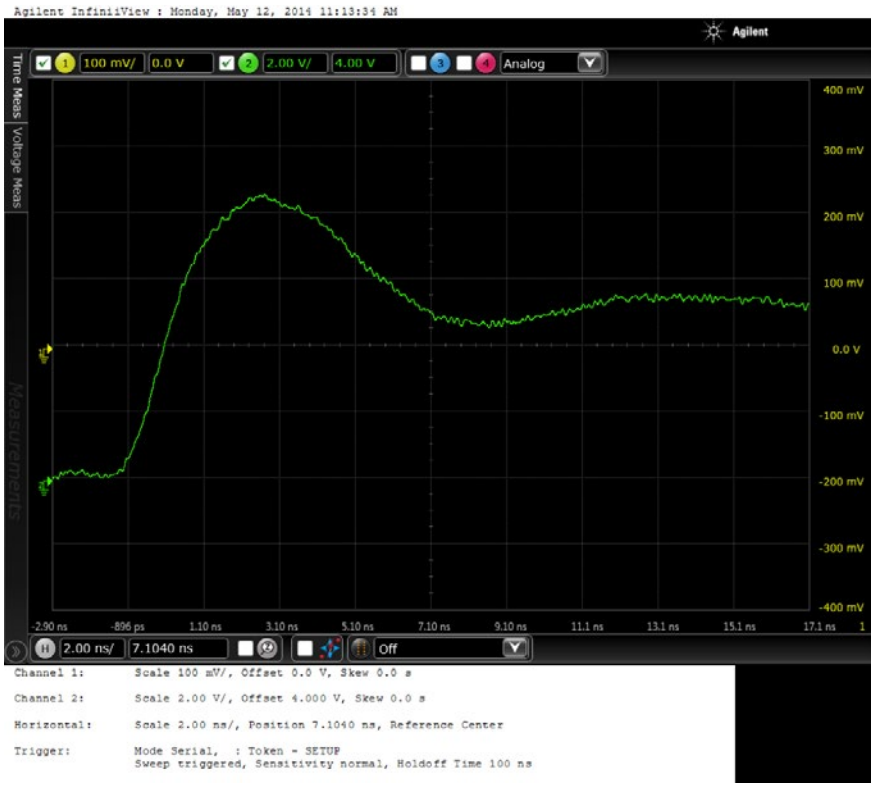


Figure 13a DUT 14667 Pre-Irradiation Rising Edge

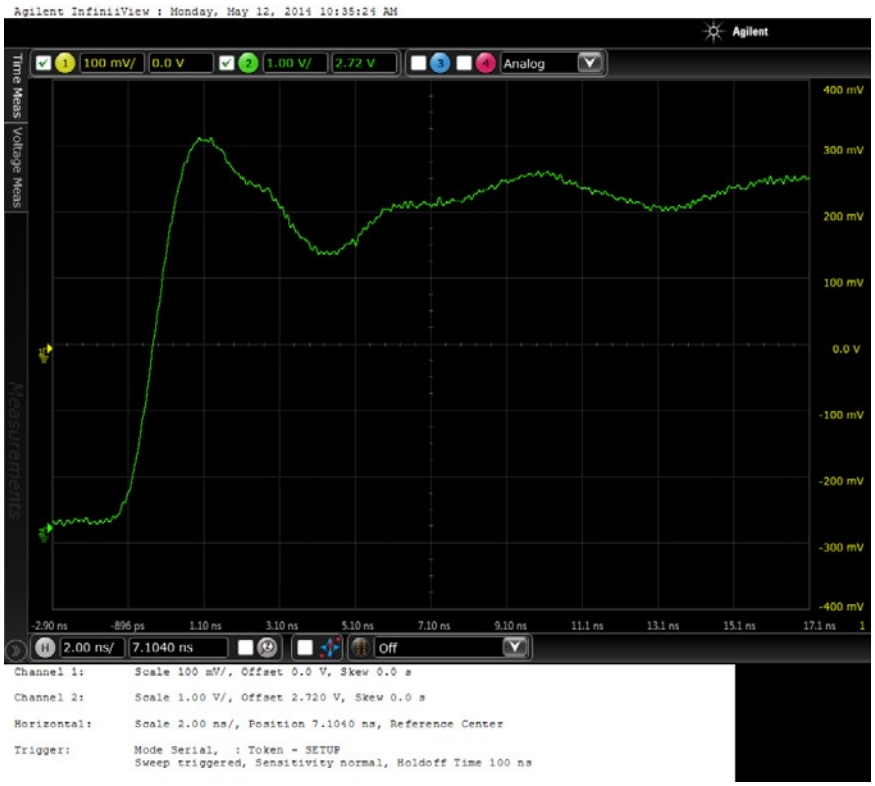


Figure 13b DUT 14667 Post-Annealing Rising Edge

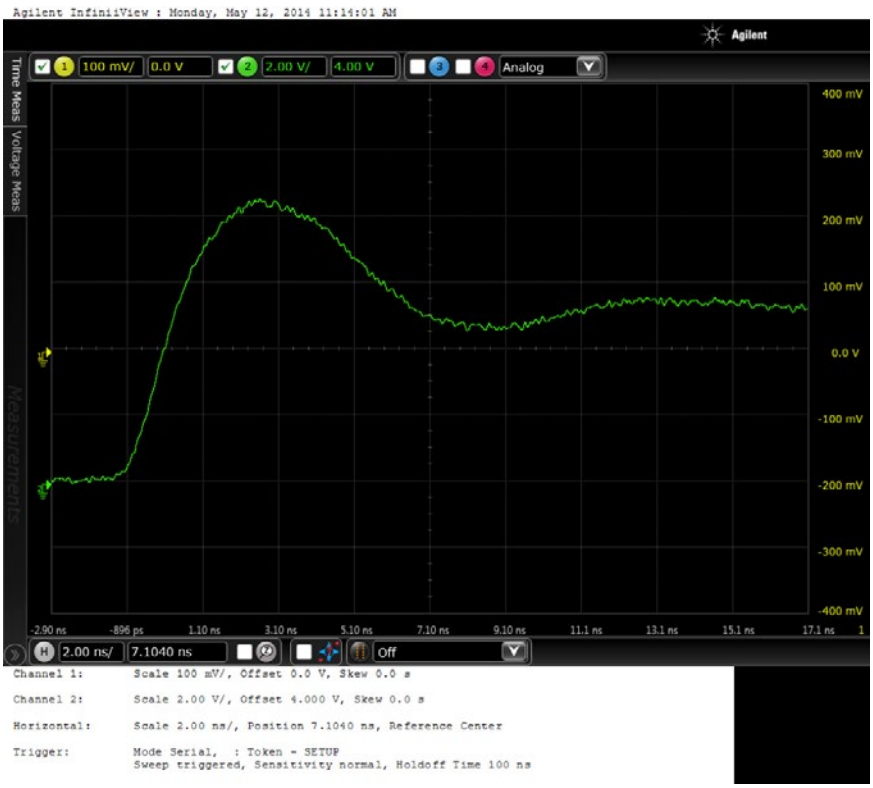


Figure 14a DUT 14860 Pre-Irradiation Rising Edge

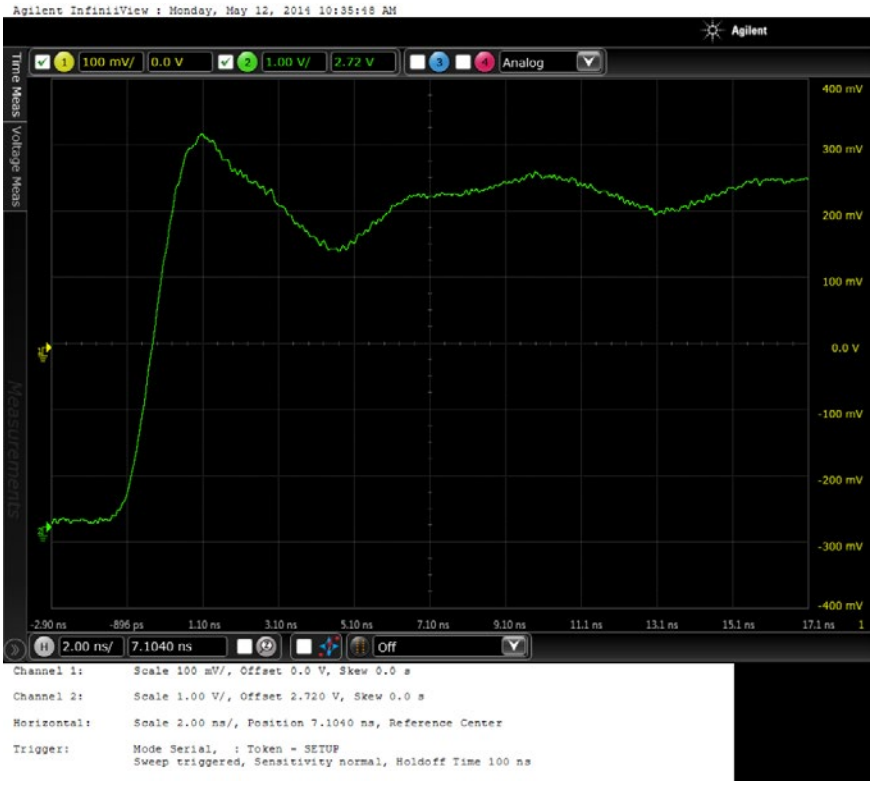


Figure 14b DUT 14860 Post-Annealing Rising Edge

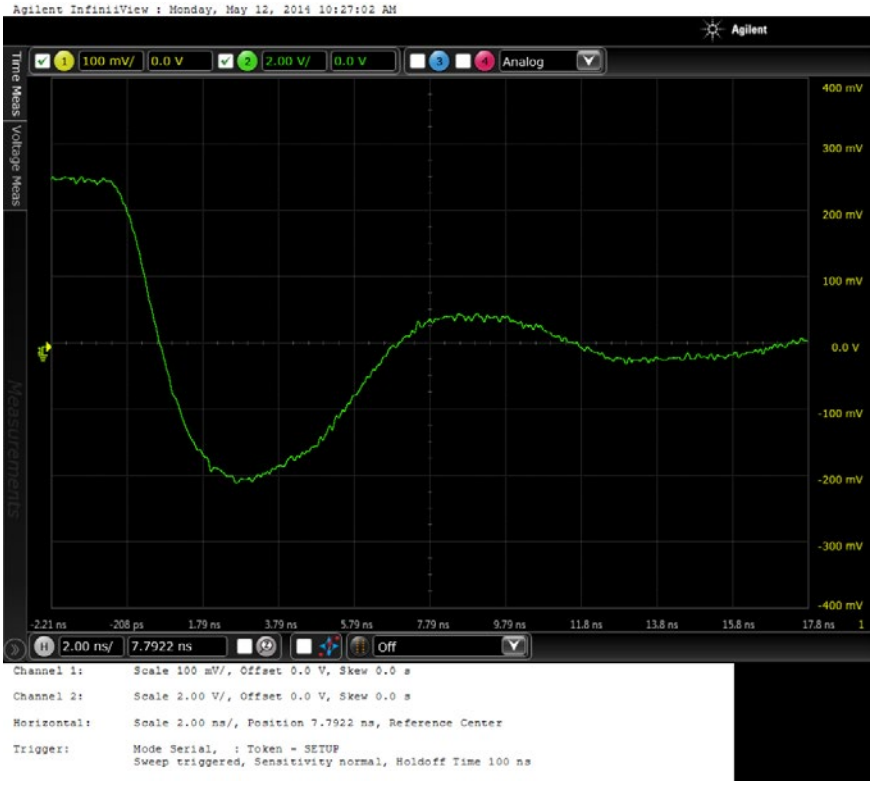


Figure 15a DUT 14643 Pre-Radiation Falling Edge

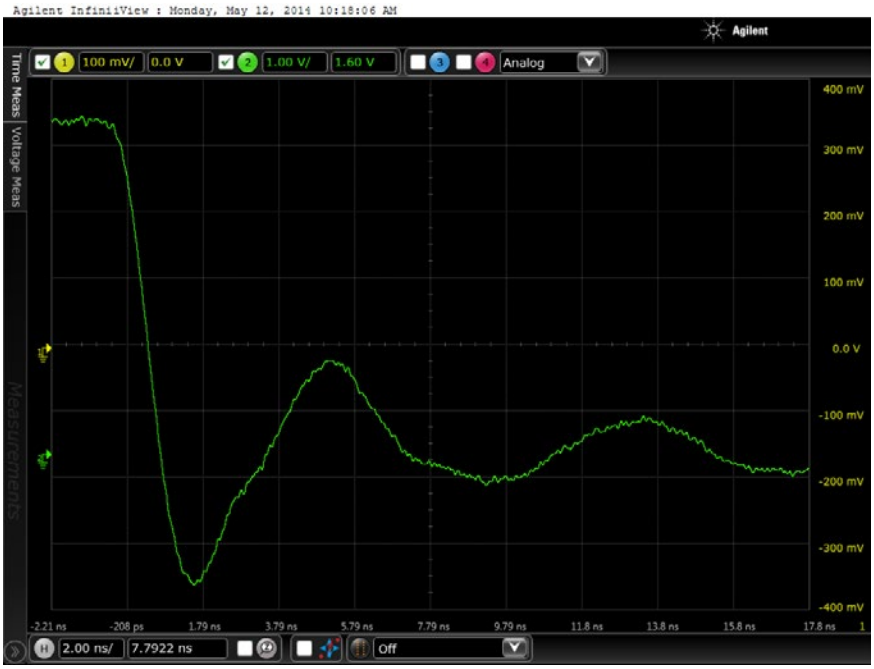


Figure 15b DUT 14643 Post-Annealing Falling Edge

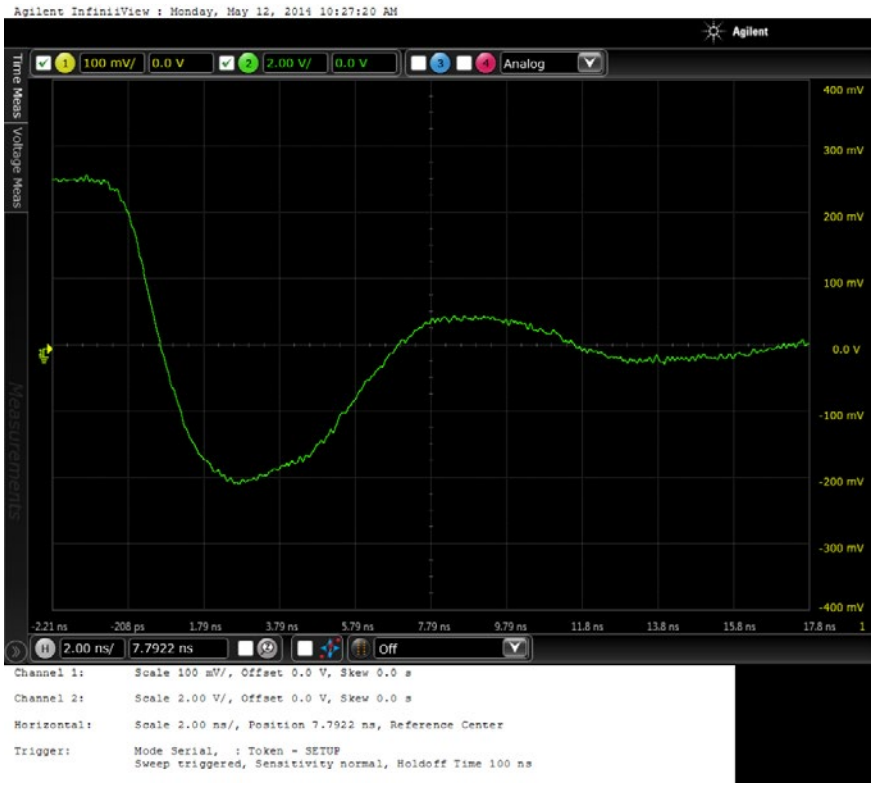


Figure 16a DUT 14649 Pre-Irradiation Falling Edge

Figure 16b DUT 14649 Post-Annealing Falling Edge

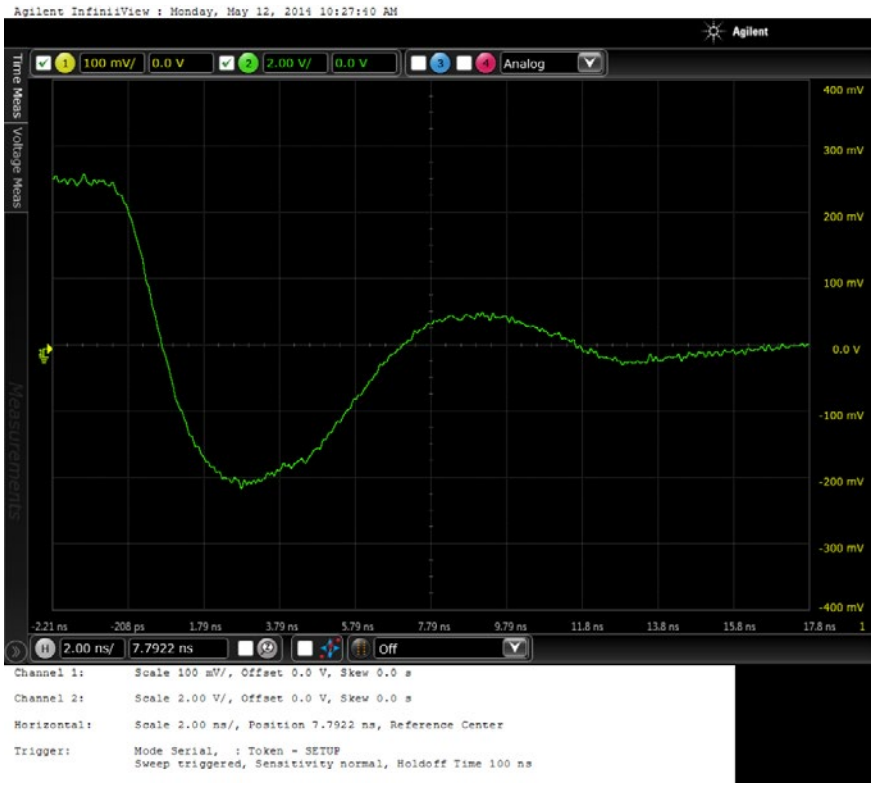


Figure 17a DUT 14661 Pre-Irradiation Falling Edge

Figure 17b DUT 14661 Post-Annealing Falling Edge

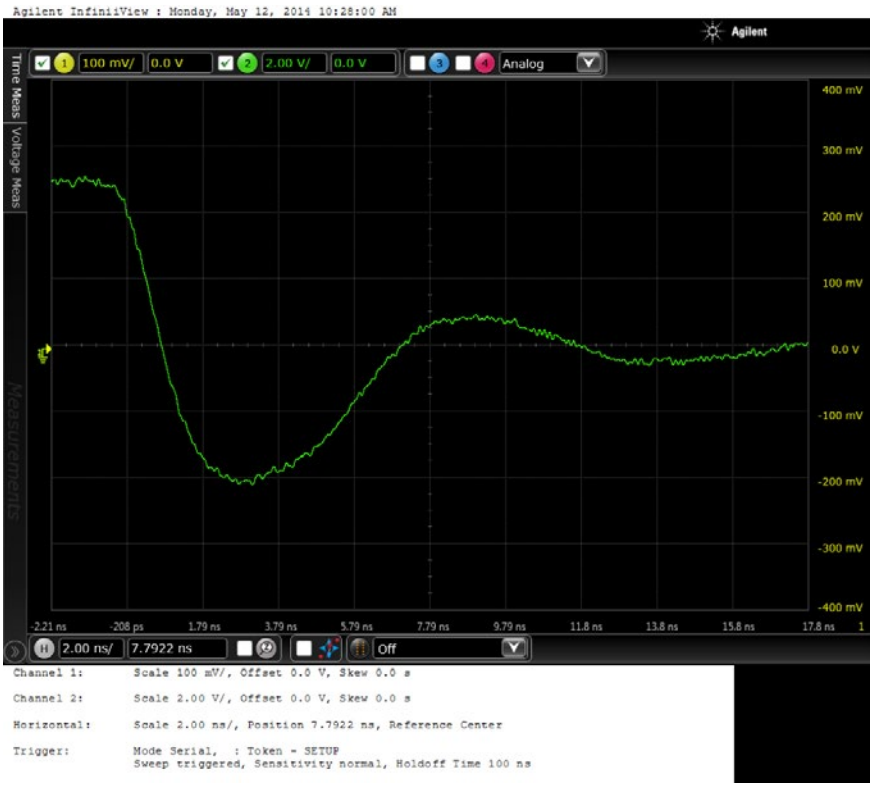


Figure 18a DUT 14665 Pre-Irradiation Falling Edge

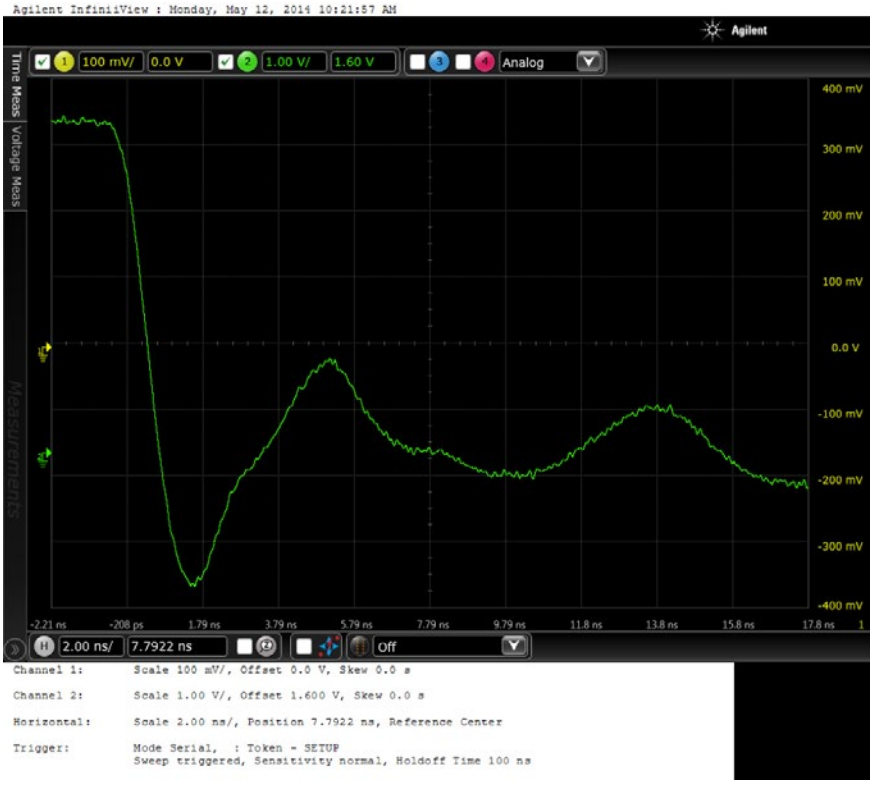


Figure 18b DUT 14665 Post-Annealing Falling Edge

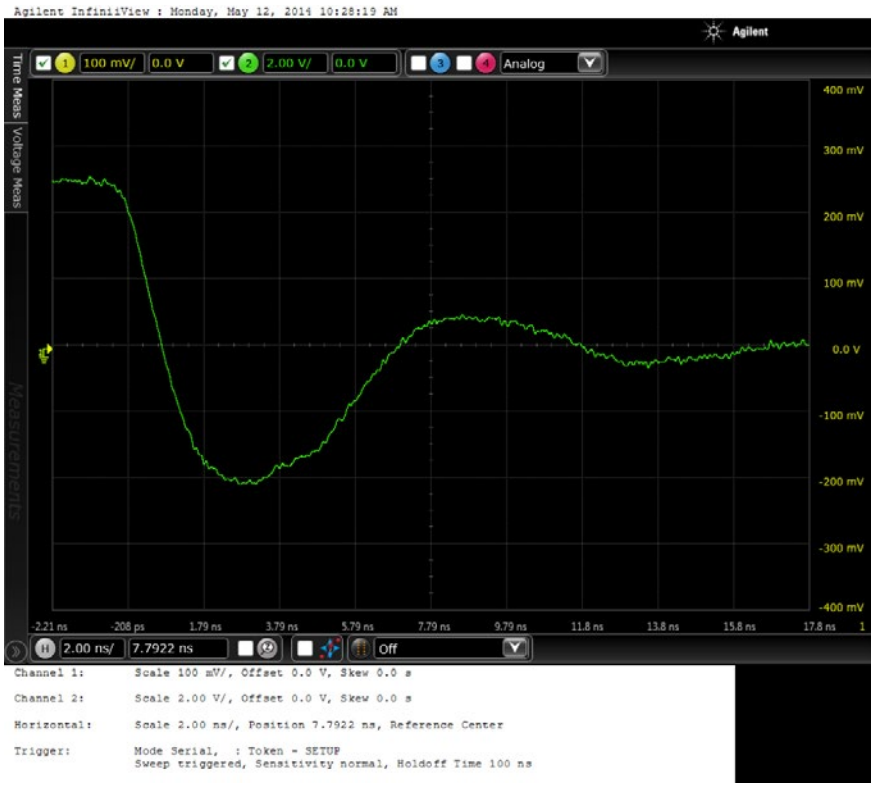


Figure 19a DUT 14667 Pre-Irradiation Falling Edge

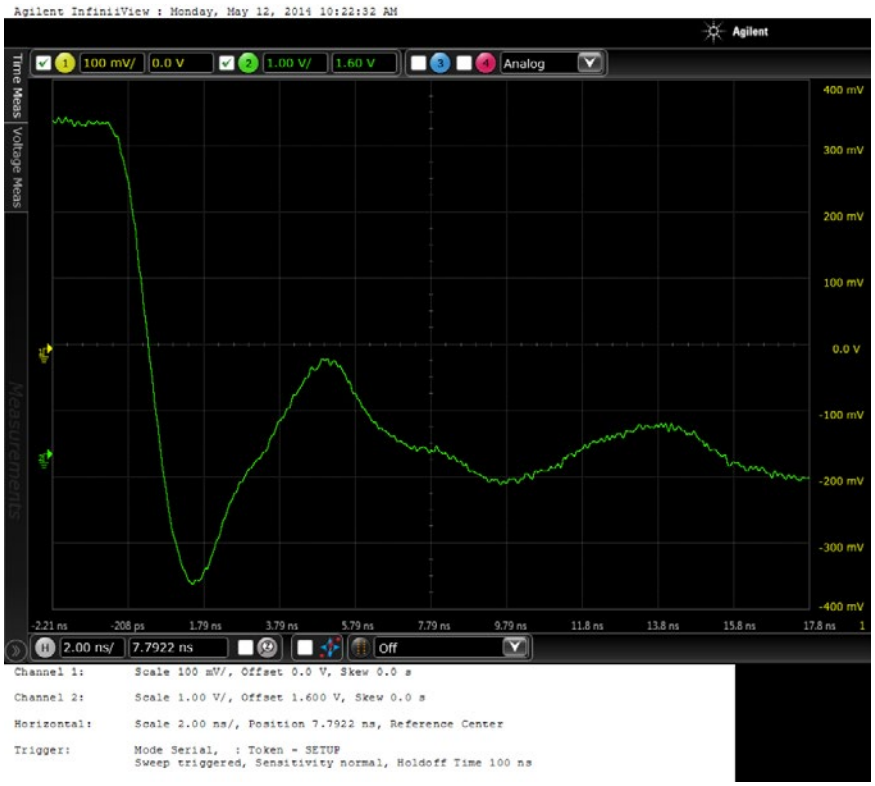


Figure 19b DUT 14667 Post-Annealing Falling Edge

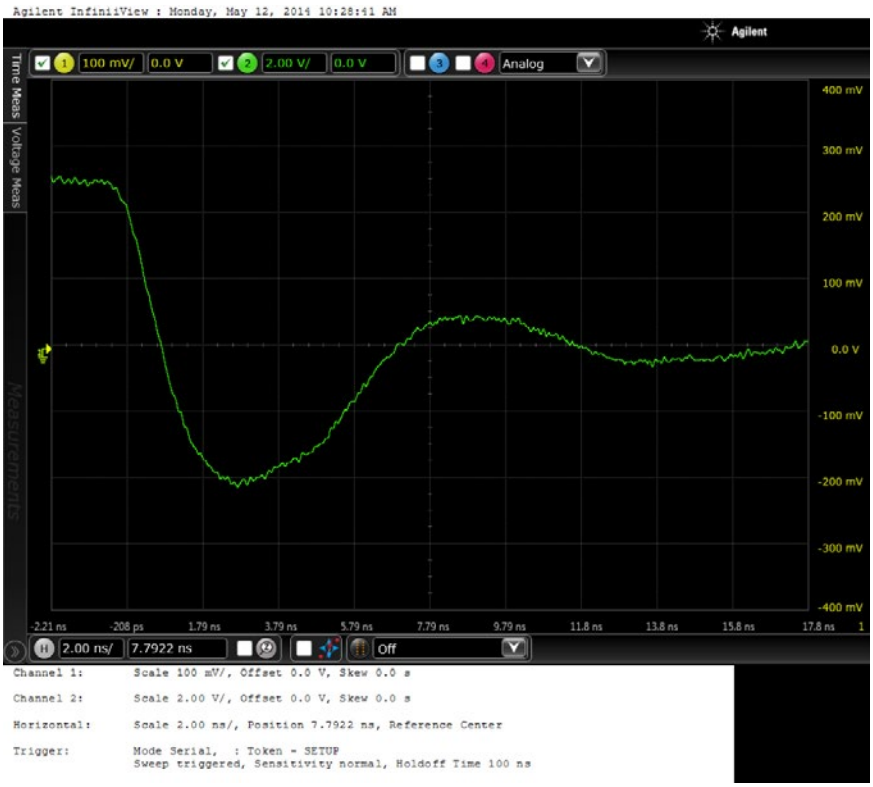


Figure 20a DUT 14860 Pre-Irradiation Falling Edge

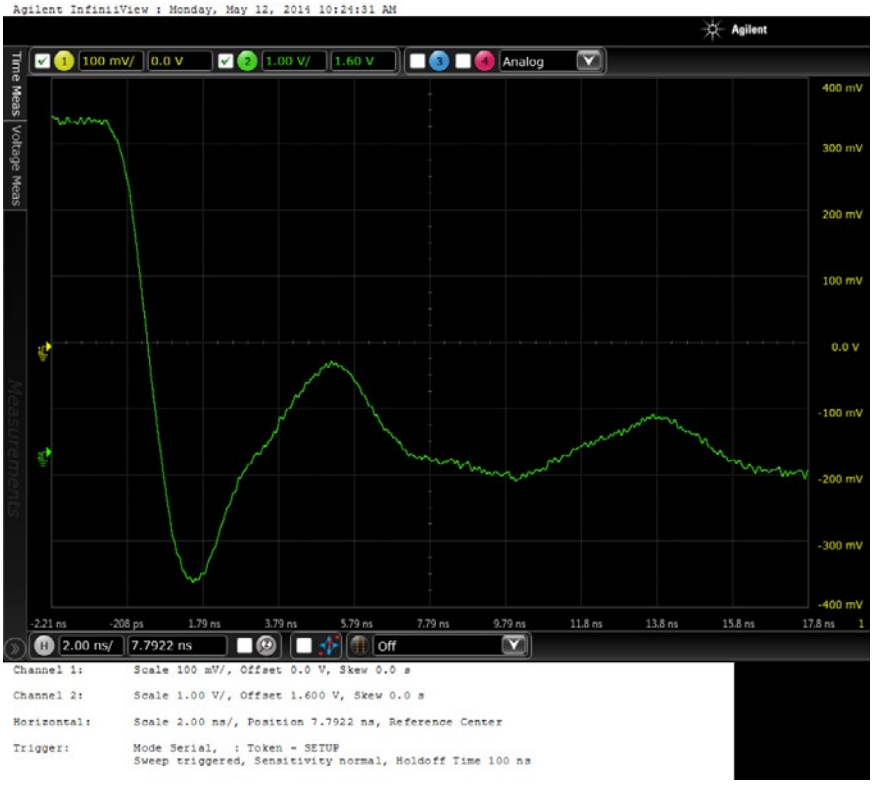


Figure 20b DUT 14860 Post-Annealing Falling Edge

Appendix A: DUT Bias

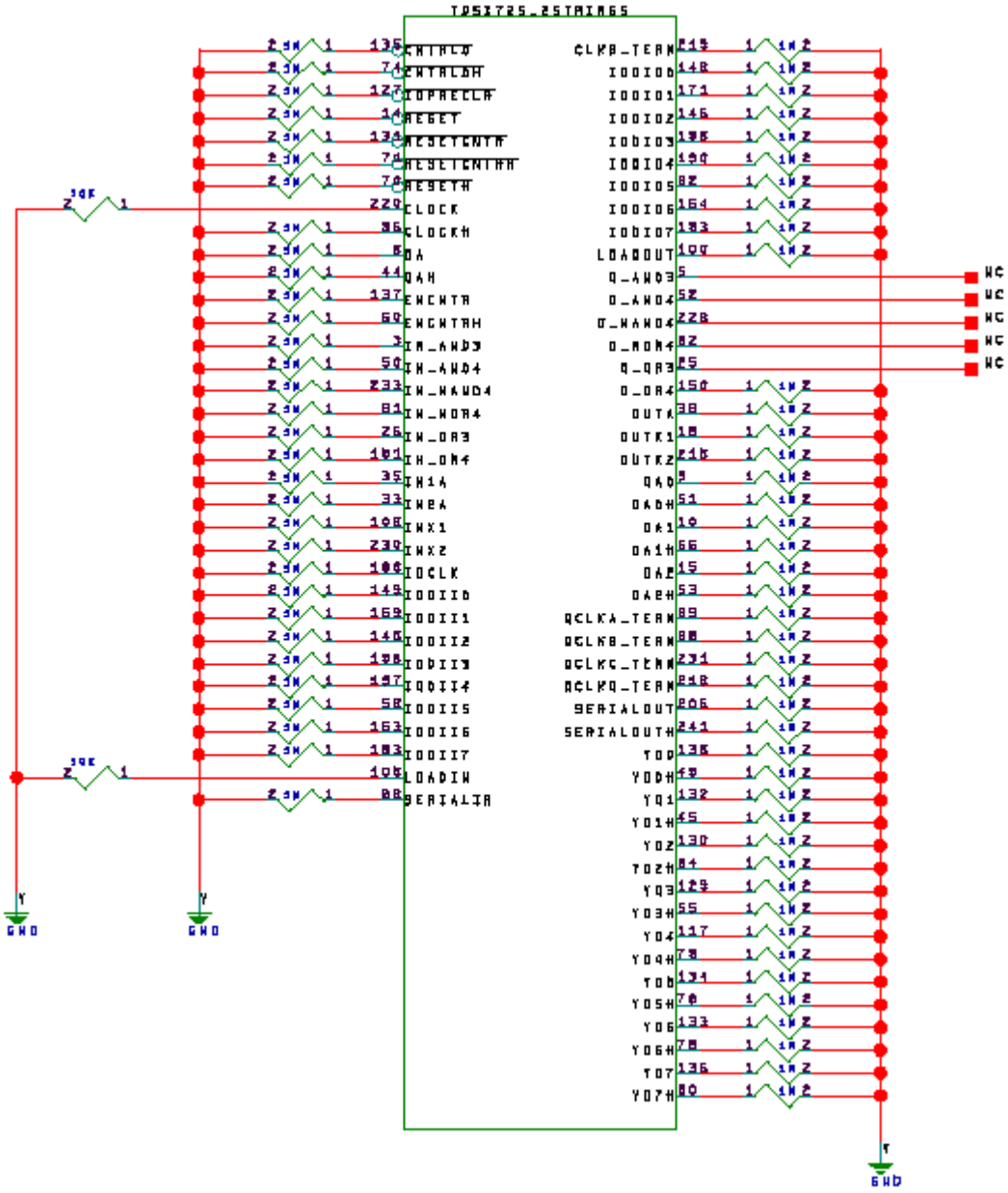


Figure A1 I/O Bias During Irradiation

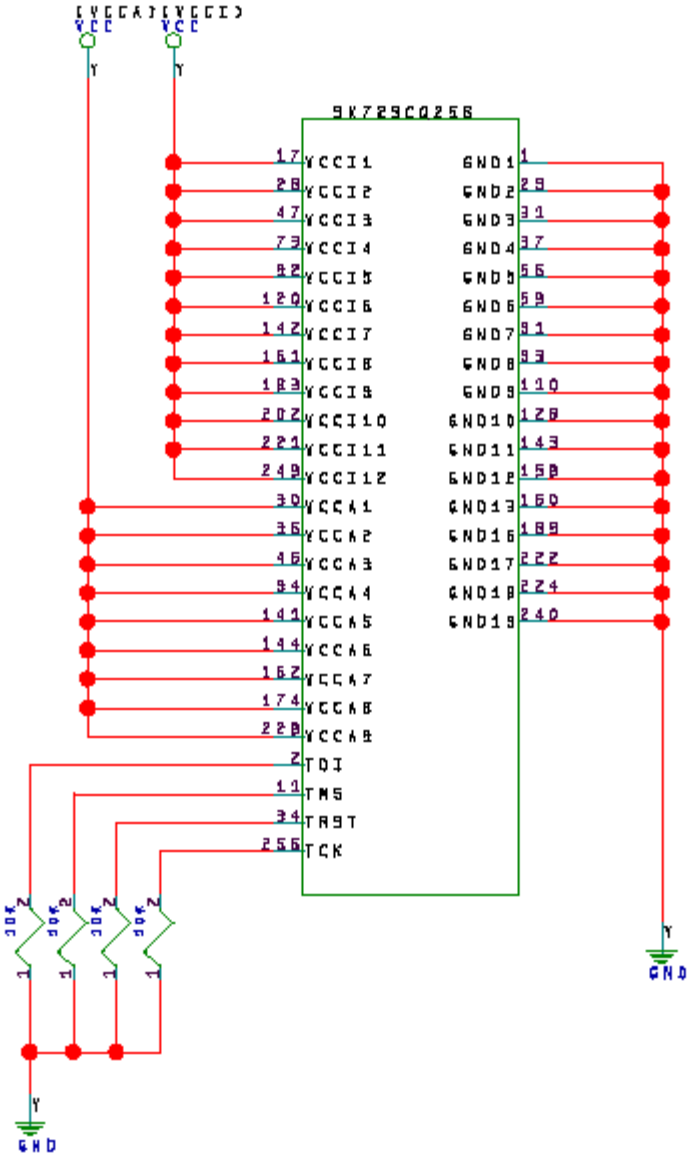
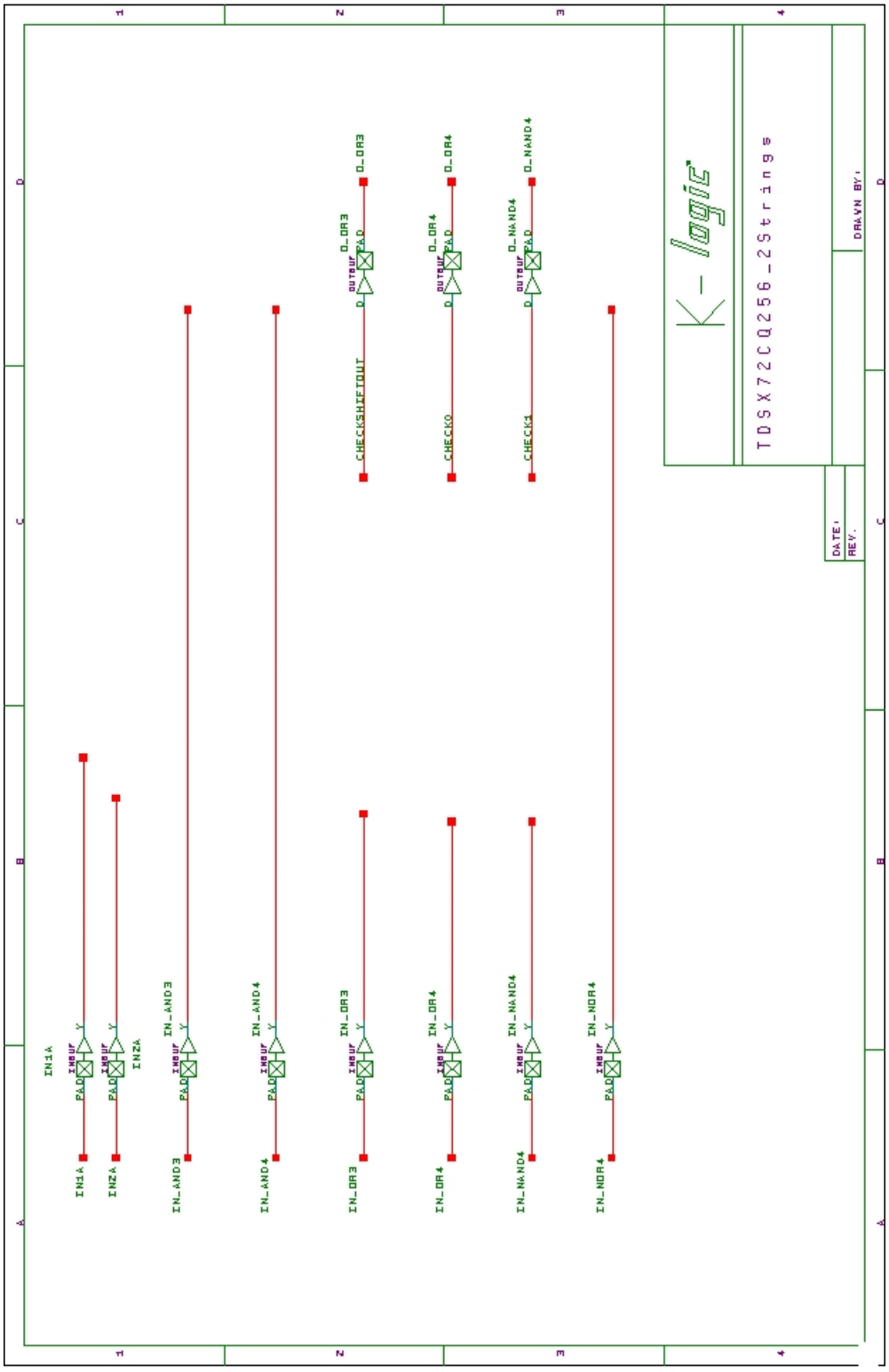
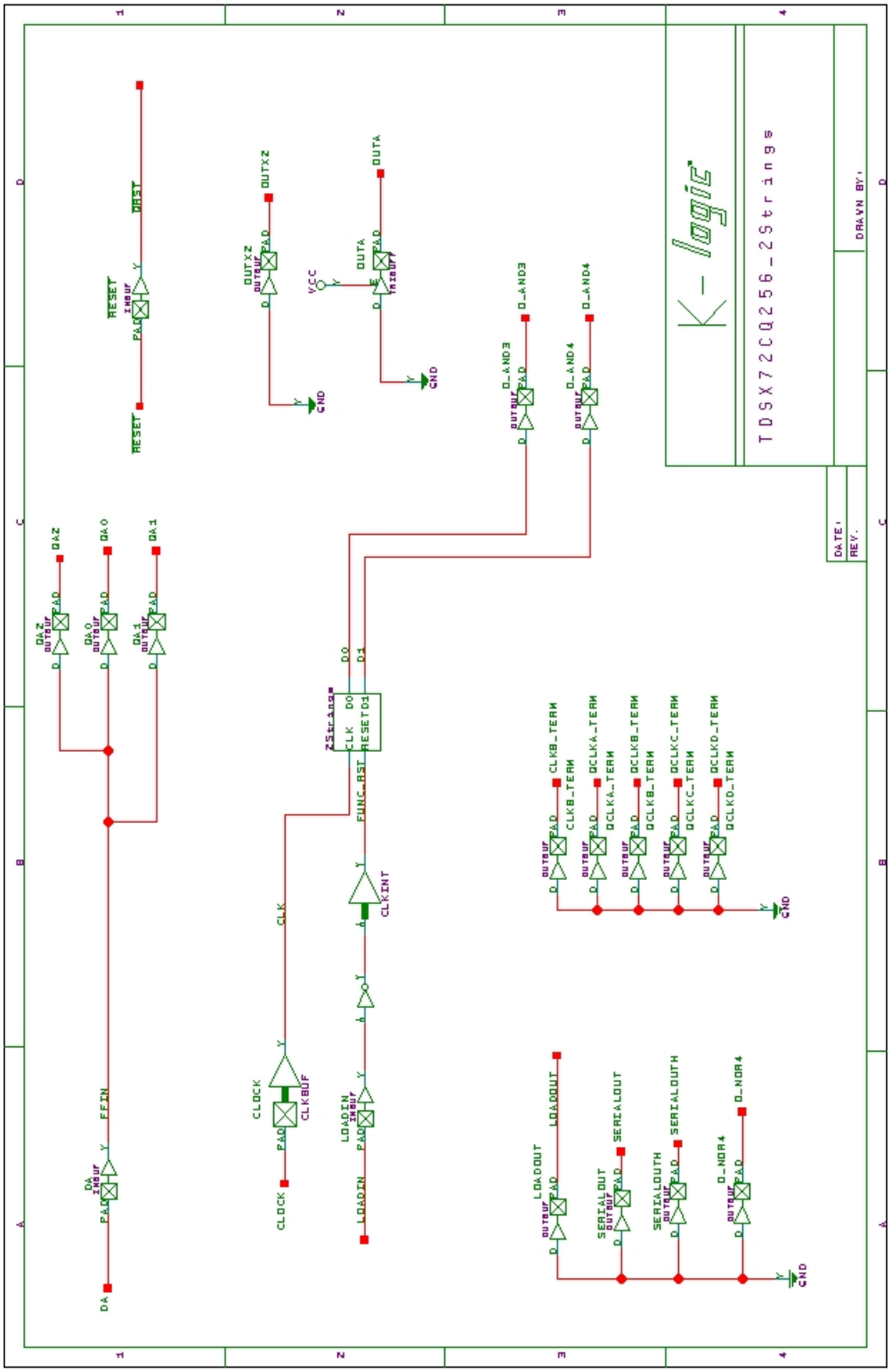
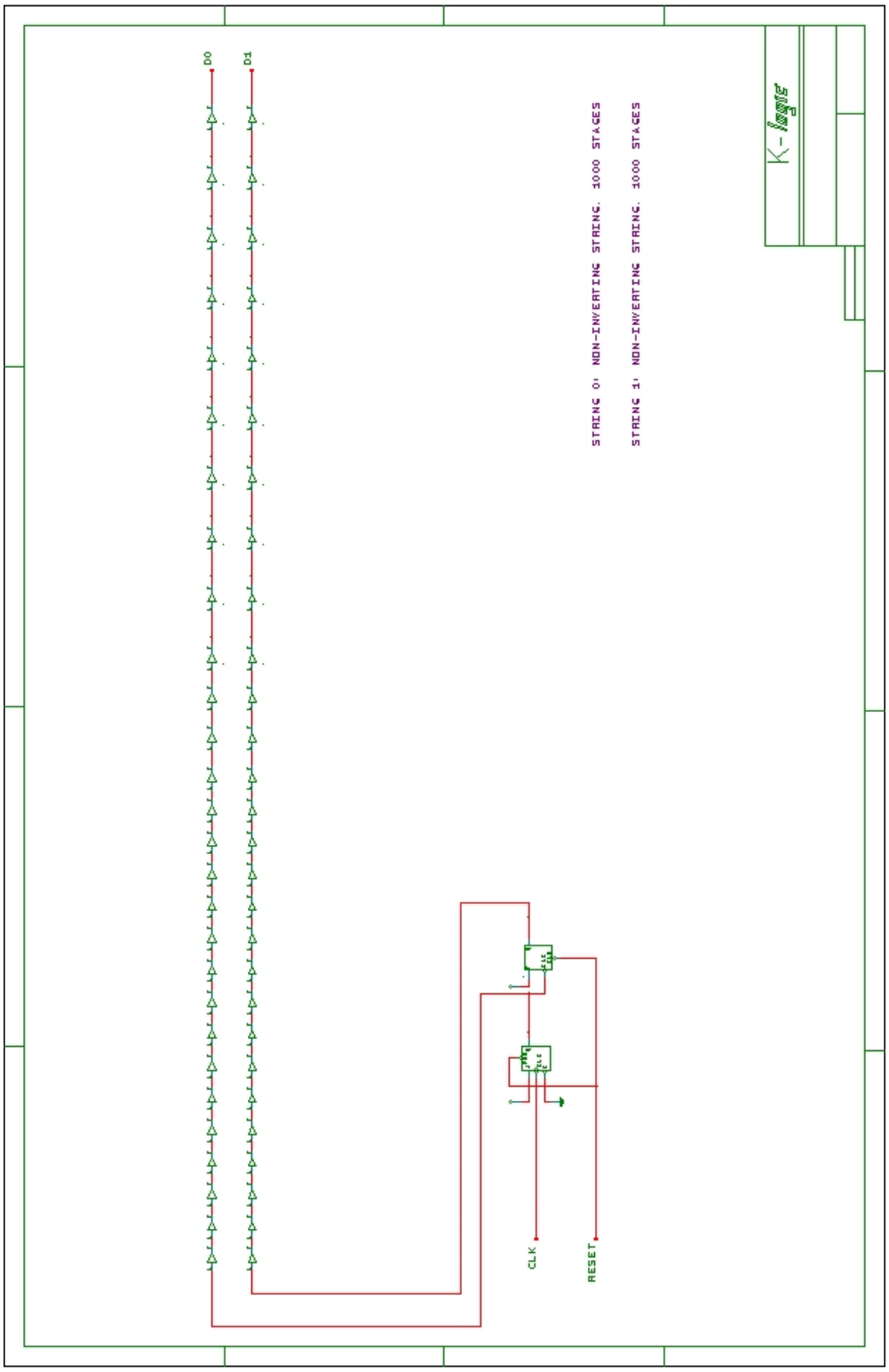


Figure A2 Power Supply, Ground, and Special Pins Bias During Irradiation

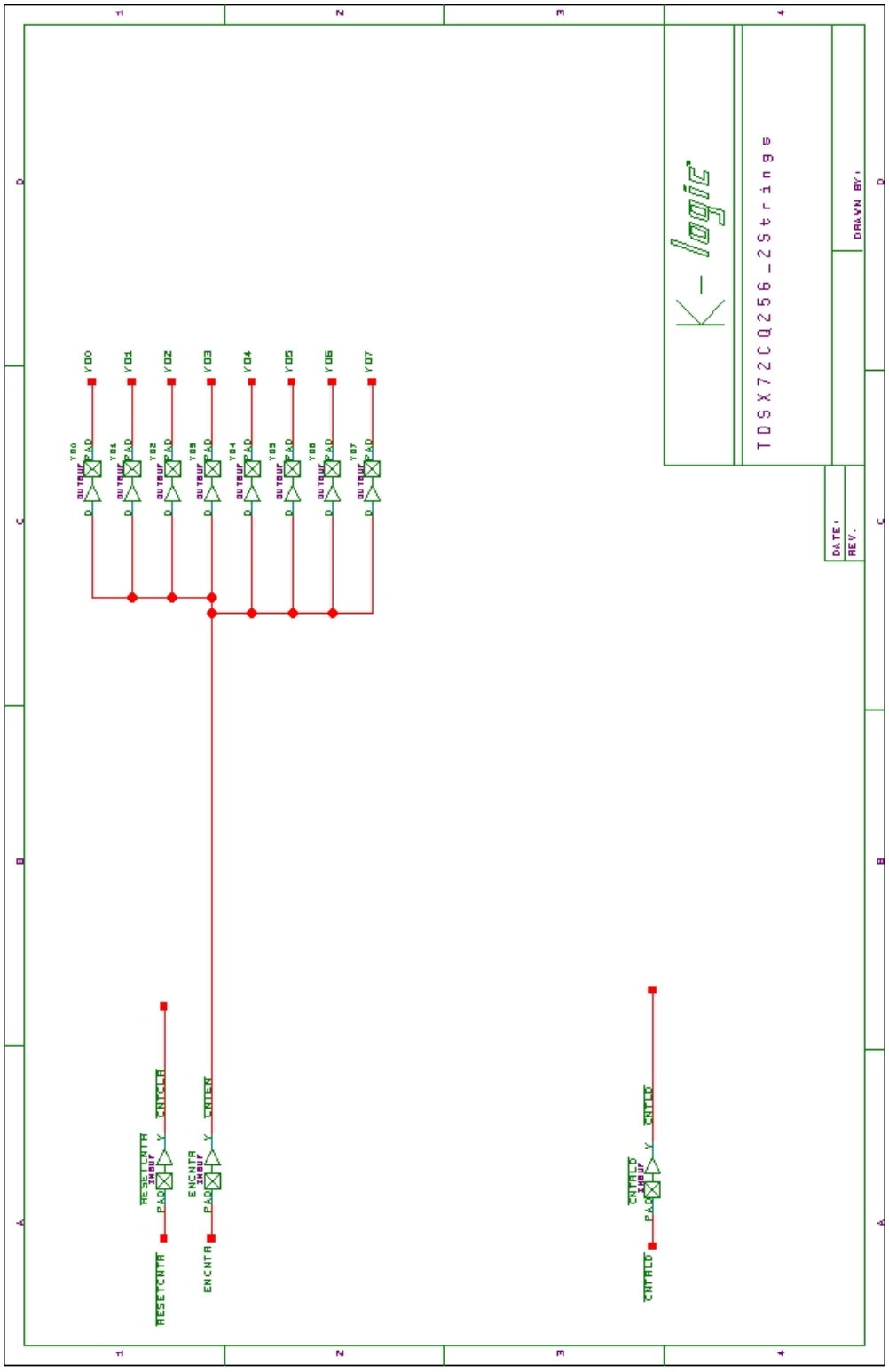
Appendix B: DUT Design Schematics

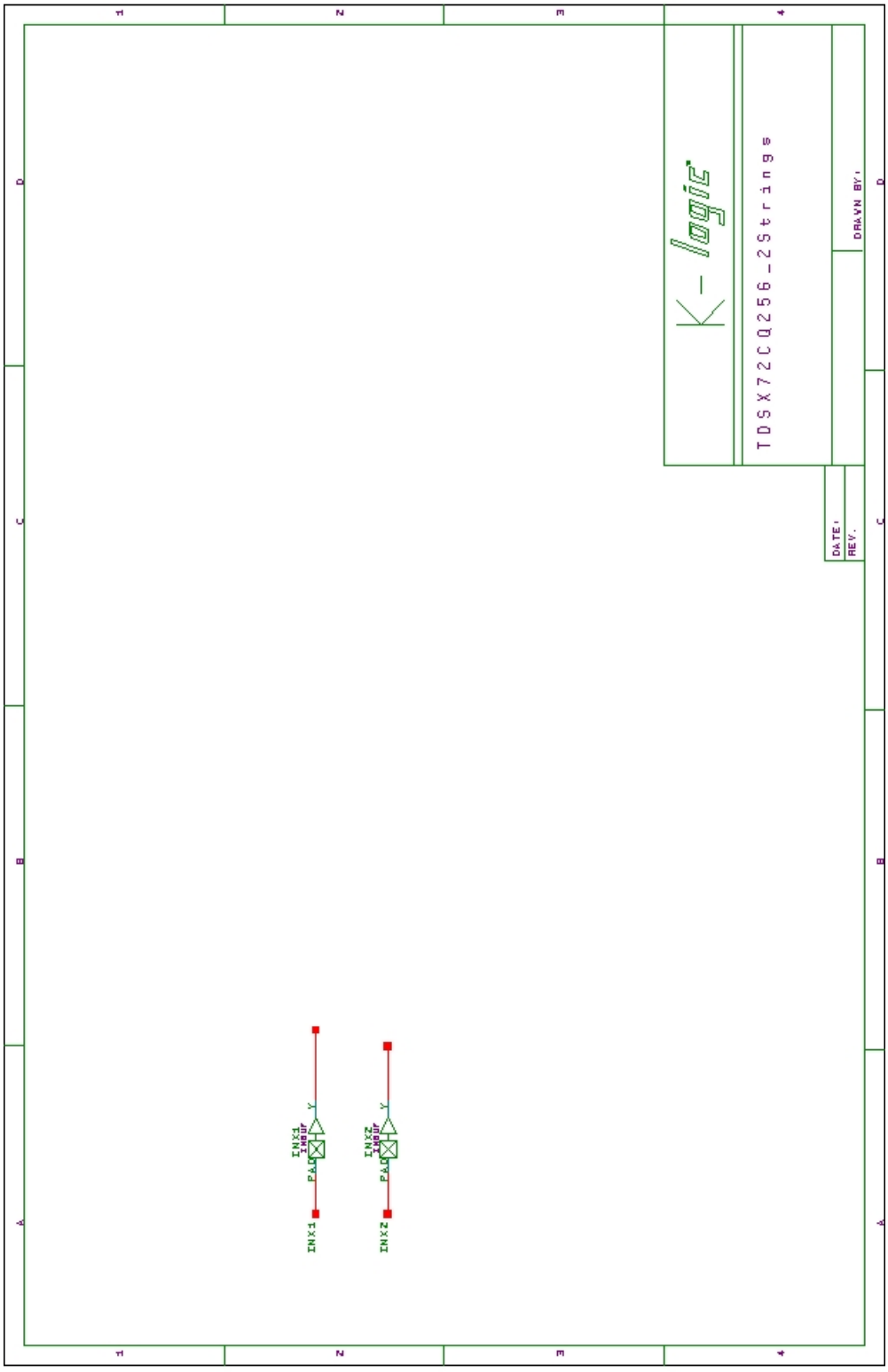


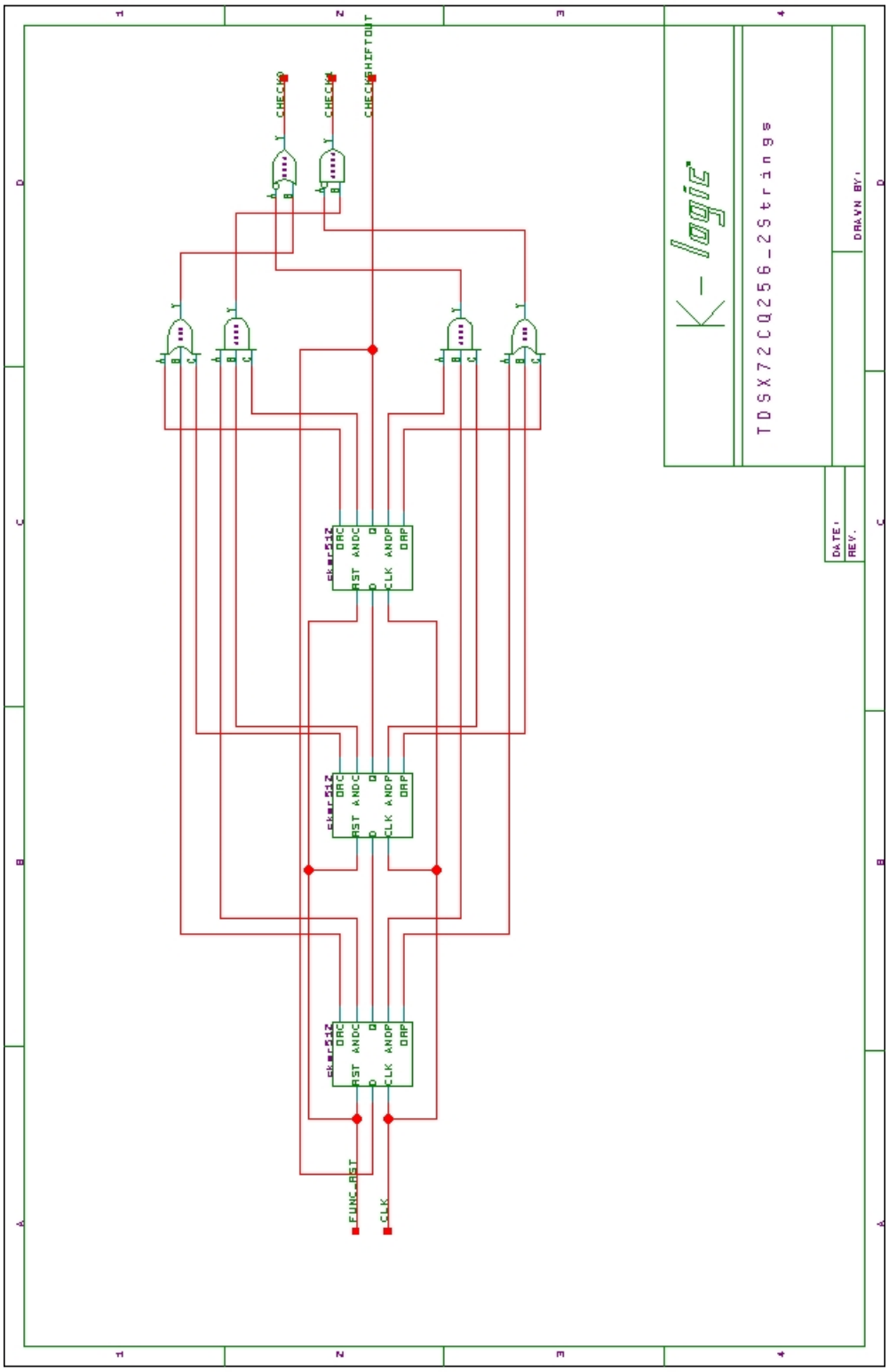

TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
RESET
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
ZStrings
CLK
D0
D1
RESET1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
DA
DA0
DA1
DA2
FFIN
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

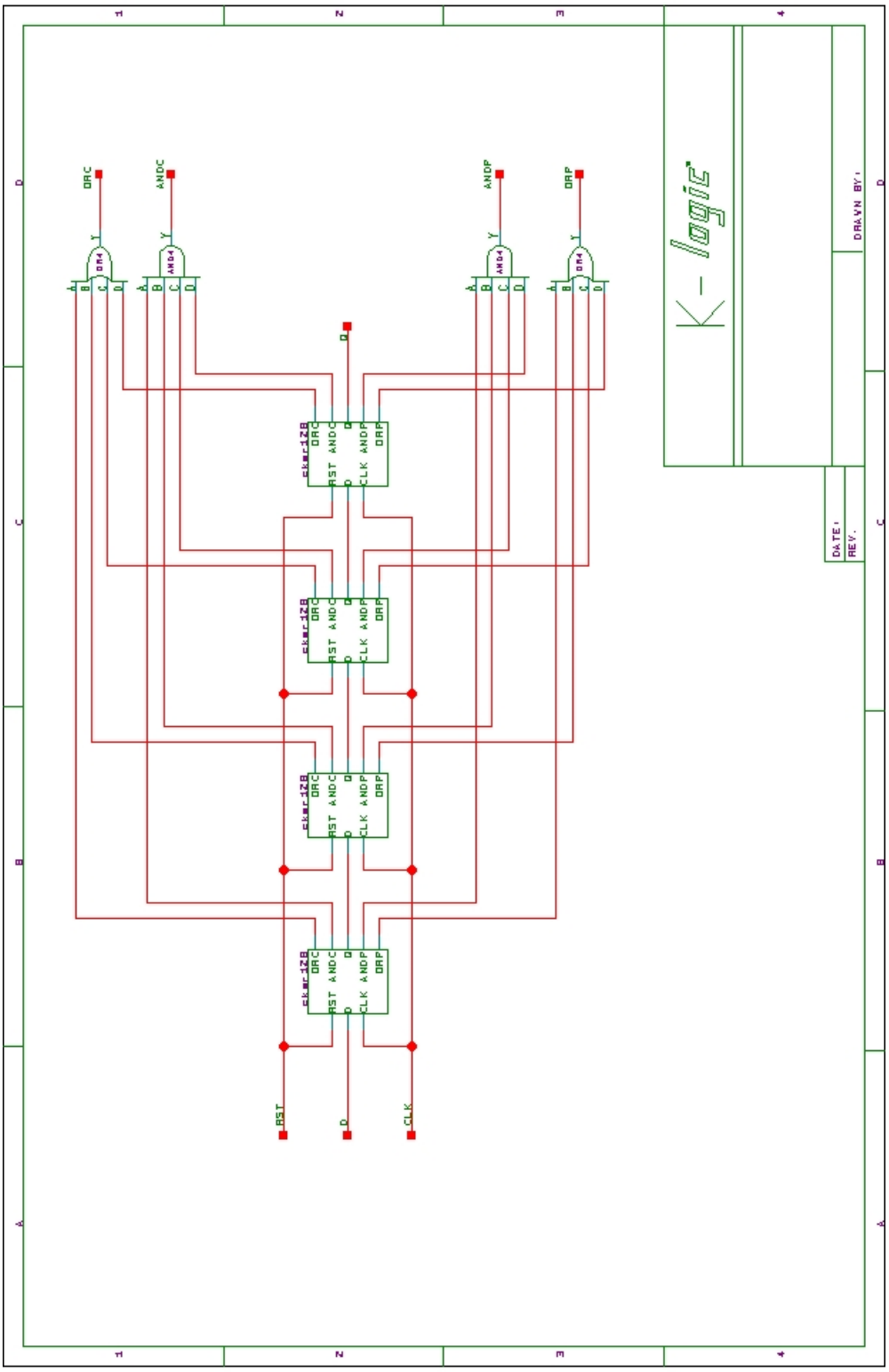

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-Logic
CLK
RESET

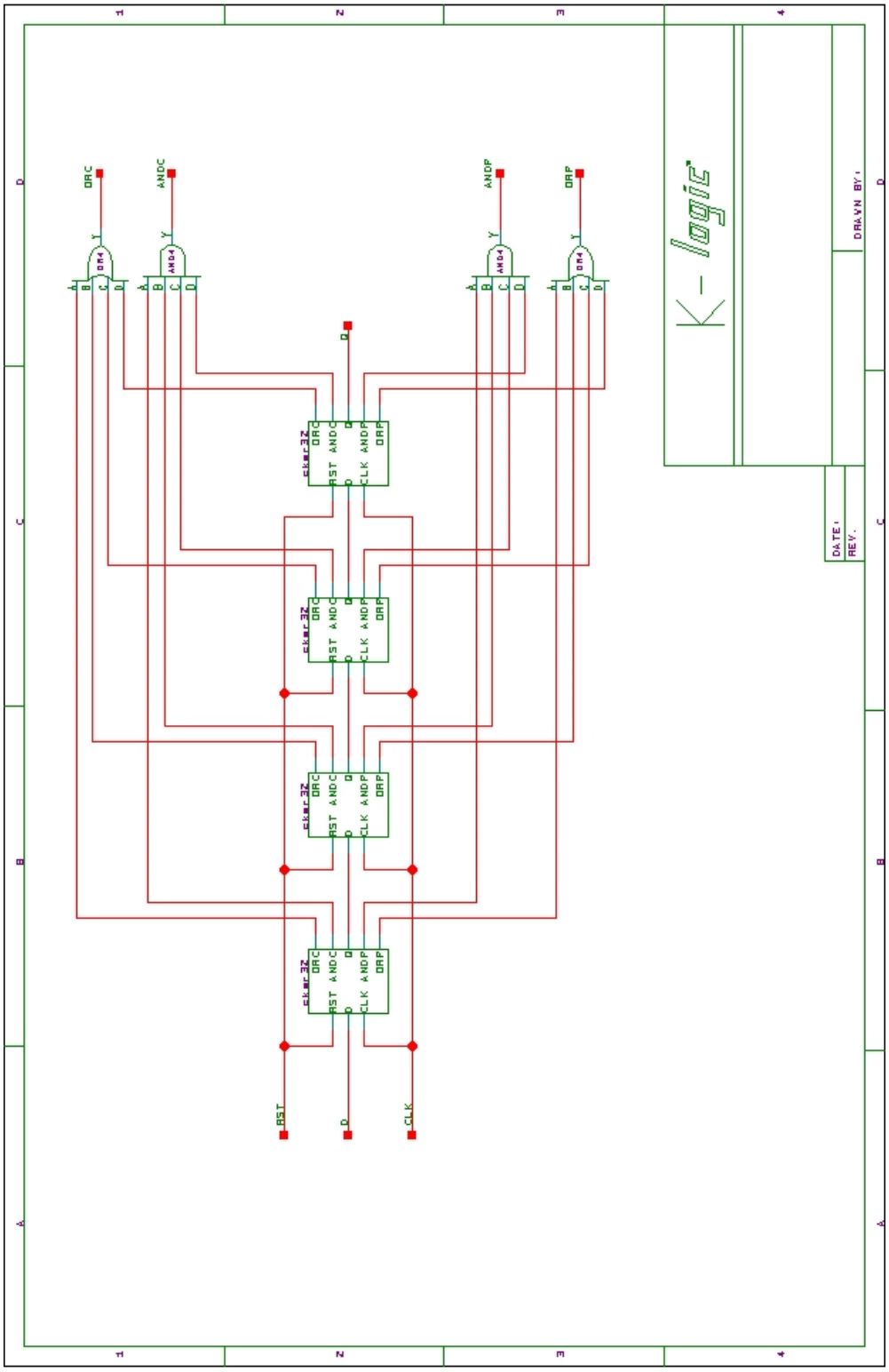

K- logic
T0ACT35XCQ\BUF50NINV
DRAWN BY: RBK
DATE:
REV.
PRESERVE

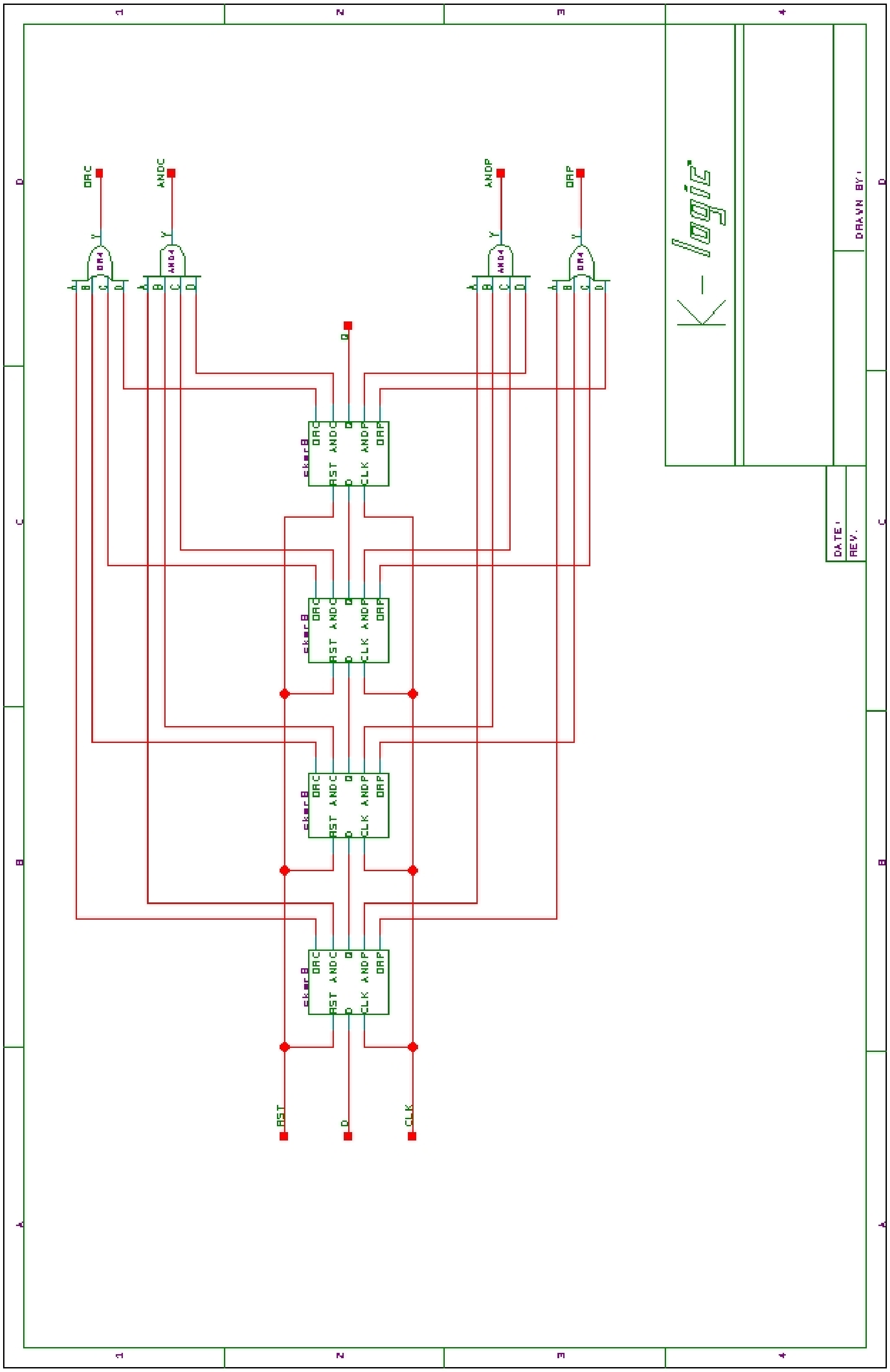

K-logic
TDSX72CQ256-25strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRCLR
CNTRCLD

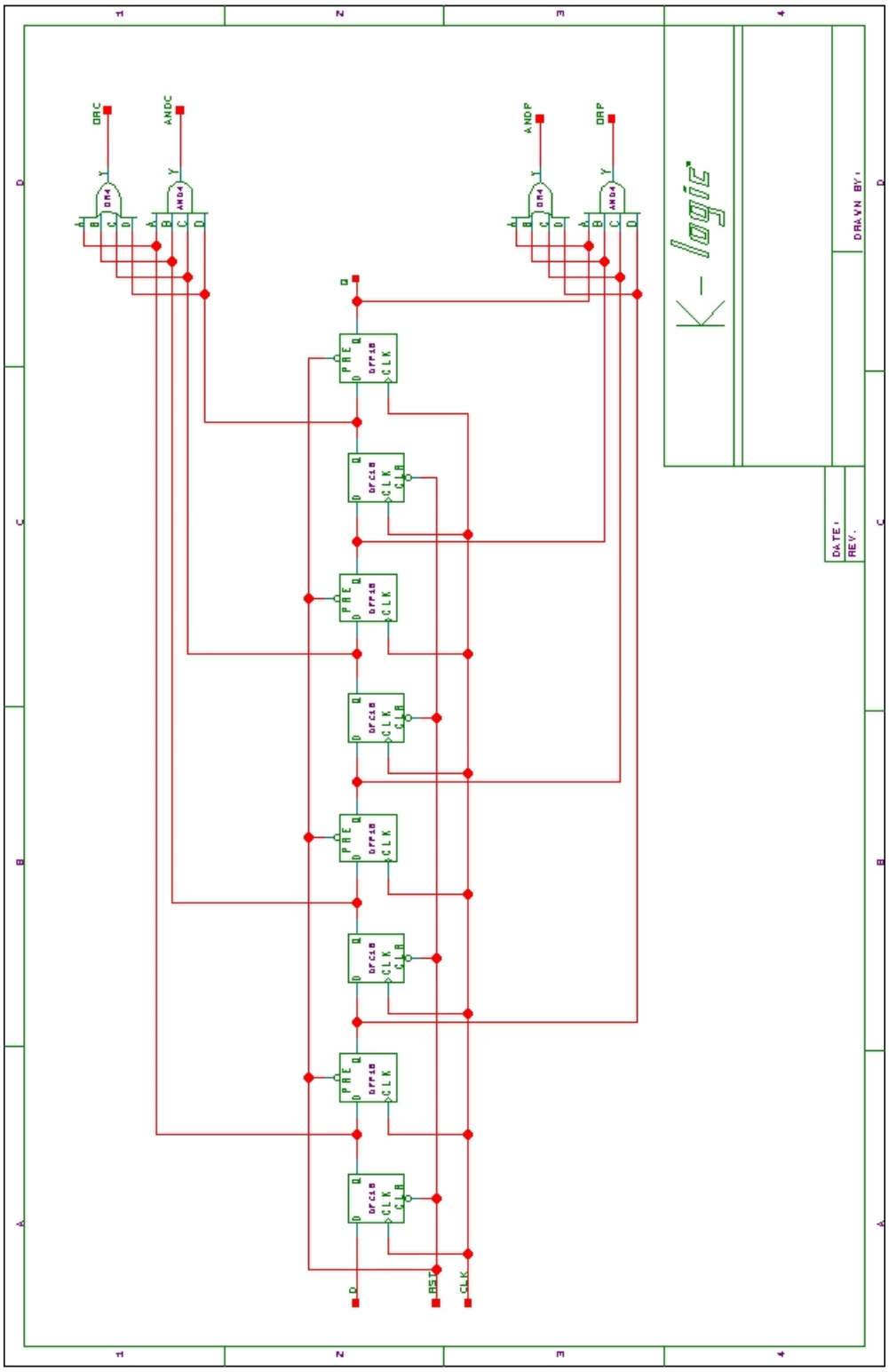

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

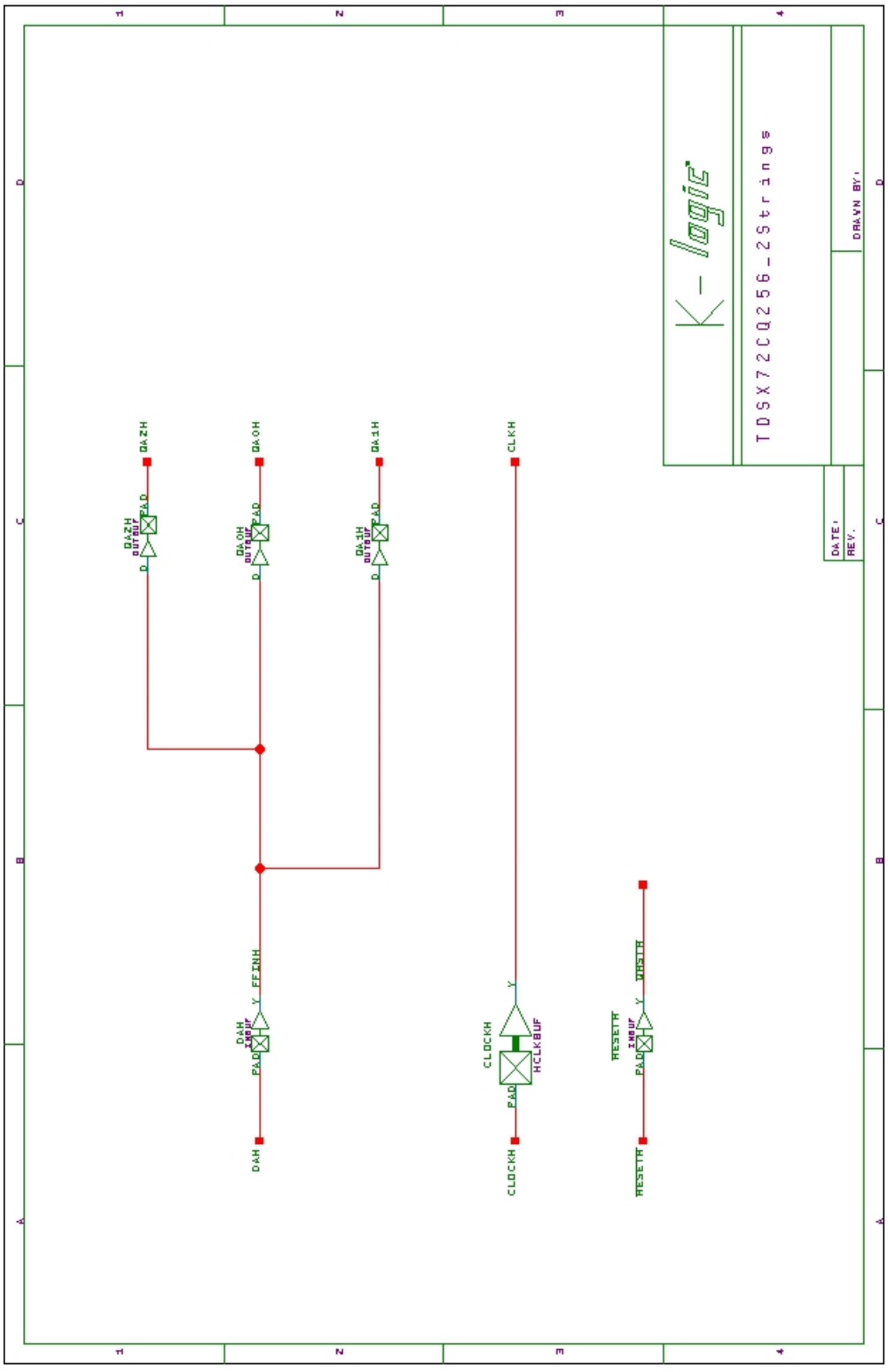

CHECK0
CHECK1
CHECKSHIFTOUT
TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
FUNC_RST
CLK

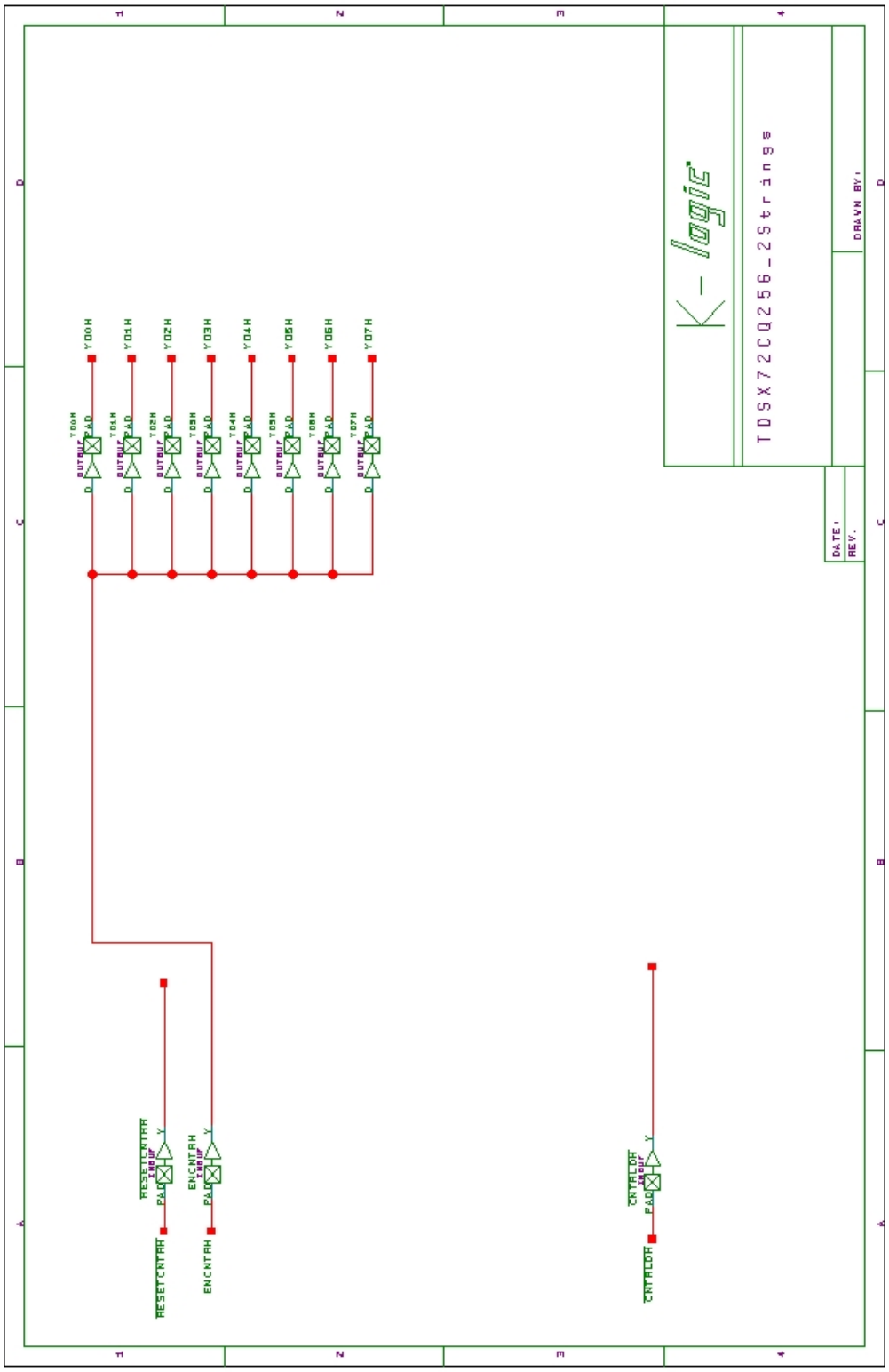

DRC
ANDC
ANDP
DRP
BST
D
CLK
DRAWN BY:
DATE:
REV.

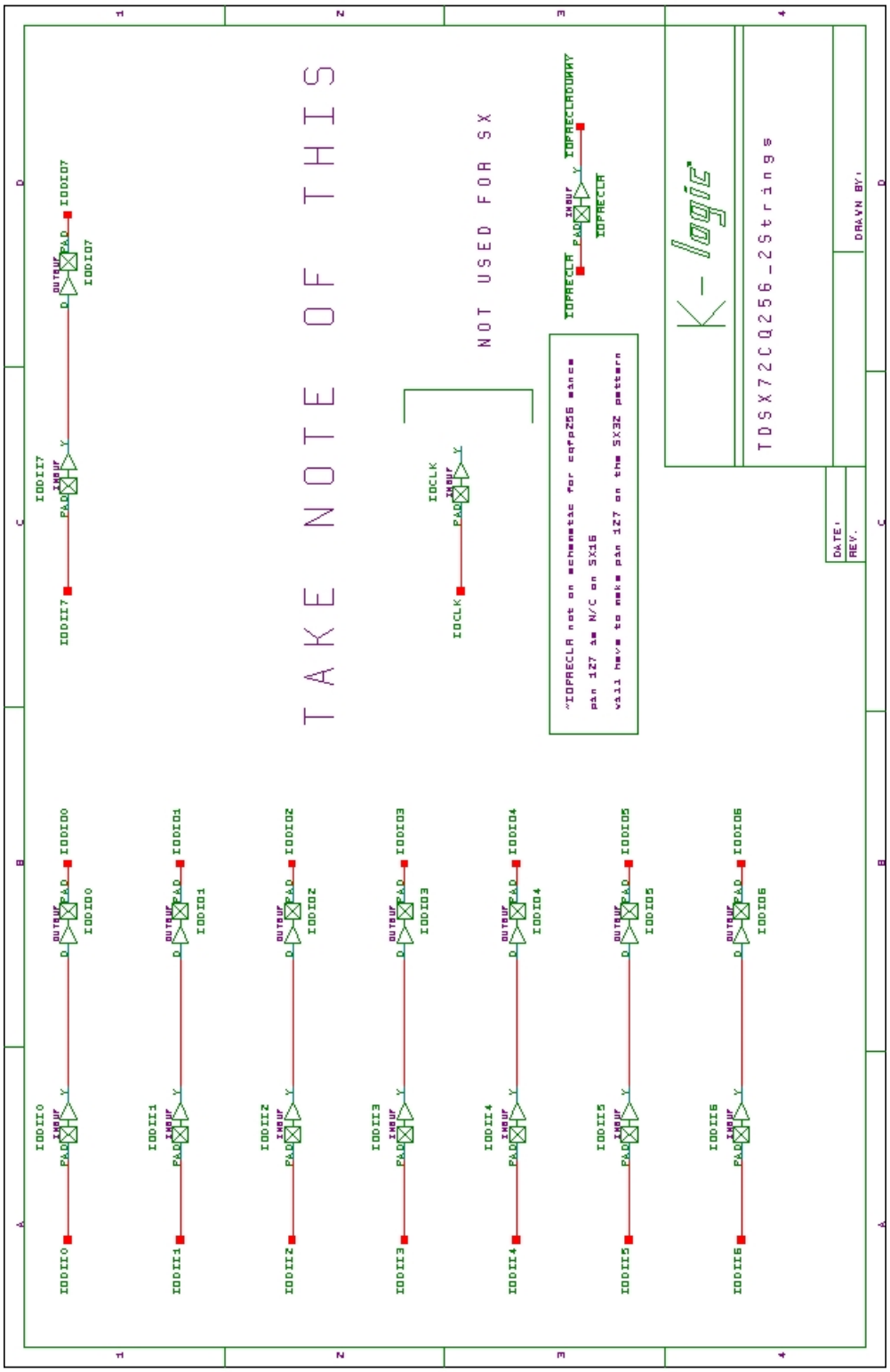

DRC
ANDC
ANDP
DRP
AND4
AND4
AND4
DFN4
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

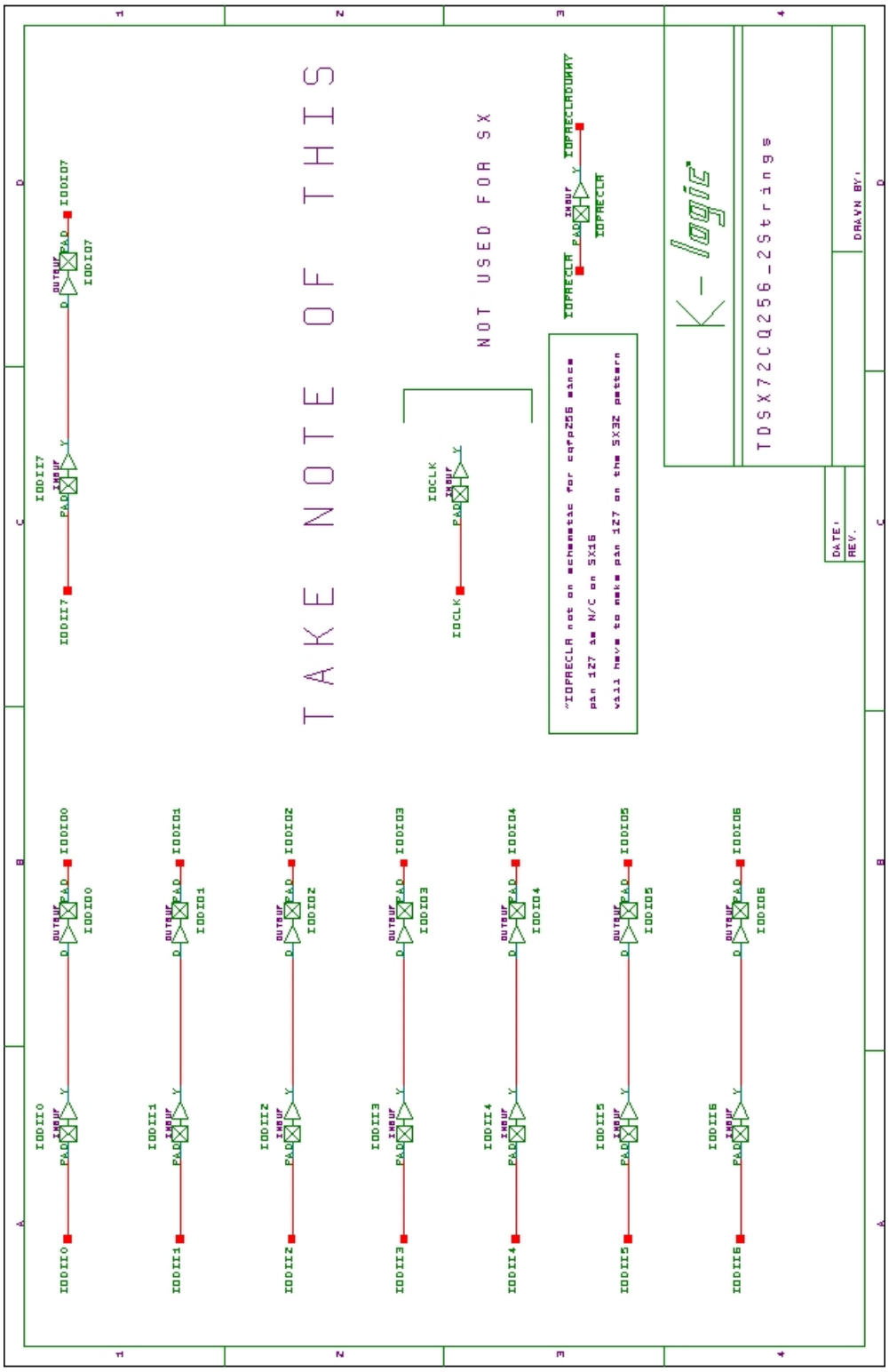

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DRAWN BY:
DATE:
REV.

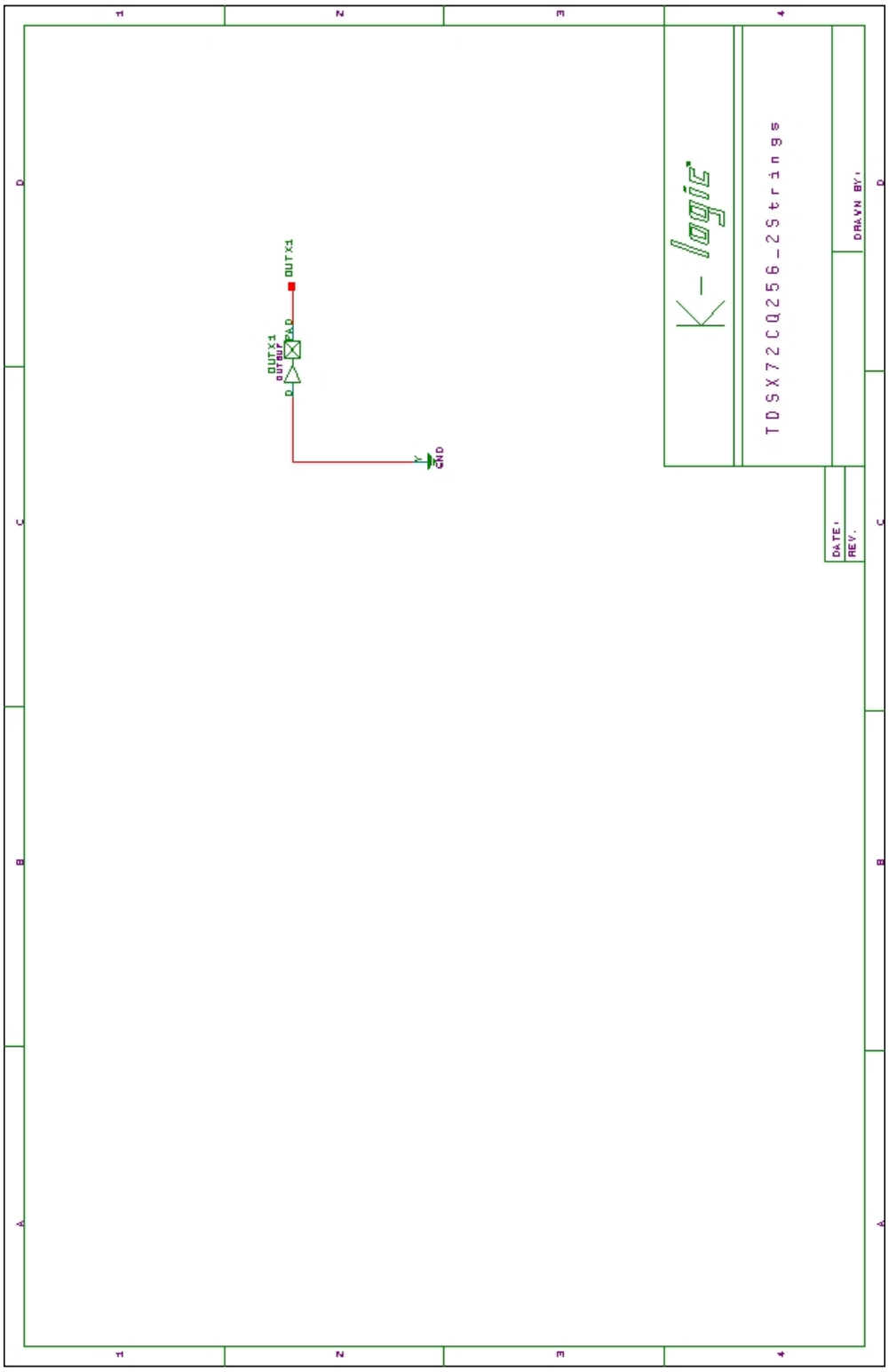

ORC
ANDC
ANDF
ORF
Q
D
RST
CLK
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DAH
RESETH
CLOCKH


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
IOPRECLR
IOPRECLRDUMMY
IOCLK
IOIO0
IOIO1
IOIO2
IOIO3
IOIO4
IOIO5
IOIO6
IOIO7
IOII0
IOII1
IOII2
IOII3
IOII4
IOII5
IOII6
IOII7


TAKE NOTE OF THIS
NOT USED FOR SX
IOCLK
IOPRECLR
IOPRECLRQUINKY
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
*IOPRECLR not on schematic for csfp256 sance
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


OUTX1
PAD
OUTX1
OUTPUT
GND
logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

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