DG0630
Demo Guide
RTG4 FPGA DSP FIR Filter

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 7.0

The following is a summary of the changes made in this revision.

- Updated the document for Libero SoC v2021.2.
- Updated Figure 5, page 7.
- Replaced Figure 26, page 29.
- Updated Table 7, page 29.

1.2 Revision 6.0

The following is a summary of the changes made in this revision.

- Added section Demo Design, page 3.
- Added Appendix 1: Programming the Device Using FlashPro Express, page 25.
- Added Appendix 2: Running the TCL Script, page 28.
- Removed the references to Libero version numbers.

1.3 Revision 5.0

Revision 5.0 of the document was updated to include features and enhancements introduced in the Libero SoC v11.9 SP1 release.

1.4 Revision 4.0

Revision 4.0 of the document was updated to include features and enhancements introduced in the Libero SoC v11.8 SP2 release.

1.5 Revision 3.0

Updated the document for Libero v11.7 software release (SAR 77670).

1.6 Revision 2.0

Updated the document for Libero v11.6 software release (SAR 72815).

1.7 Revision 1.0

Revision 1.0 was the first publication of this document.

2 RTG4 FPGA - DSP FIR Filter Demo

The RTG4™ FPGA devices integrate a fourth generation flash-based FPGA fabric architecture, which includes embedded Mathblocks optimized for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

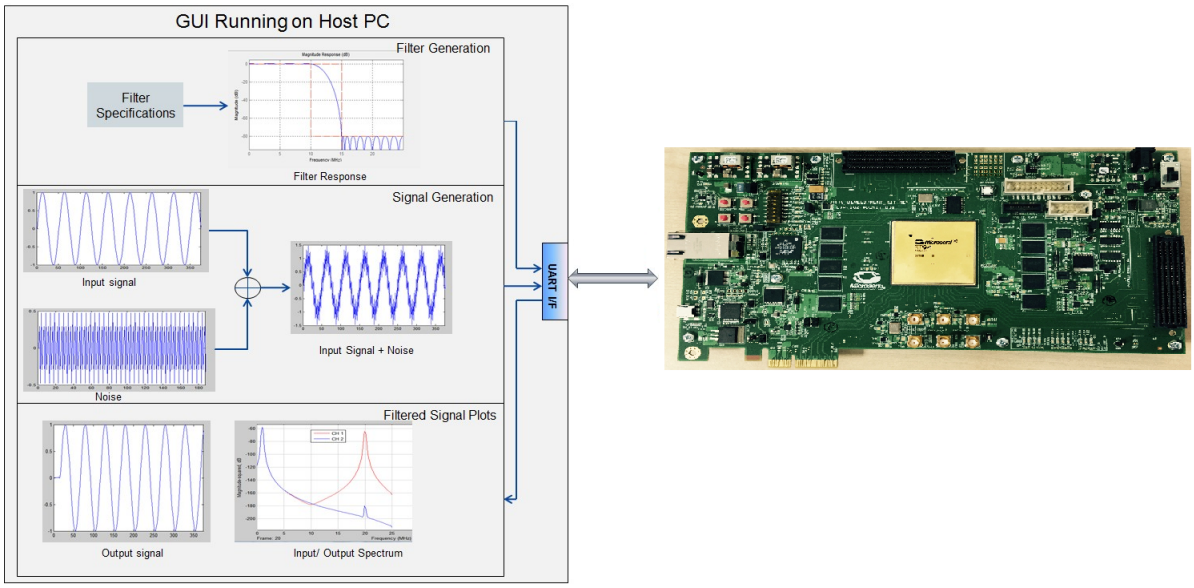
The demo design features:

- CoreFIR filter IP – Low-pass, High-pass, Band-pass, and Band-reject operations.
- CoreFFT FFT IP – to generate the output spectrum of the filtered signal.
- A GUI interface from host PC to generate filter coefficients, input signals (Pass-band frequency and Stop-band frequency), and also plots the input/output waveforms, and the required spectrum.

Microsemi CoreFIR filter IP is used to suppress the unwanted frequency components, and CoreFFT IP is used to generate the output spectrum to verify the filtering operation.

The following figure shows top-level diagram for the DSP FIR filter demo.

Figure 1 • **Top-Level Diagram of DSP FIR Filter Demo**



2.1 Design Requirements

The following table lists the hardware and software requirements for the demo.

Table 1 • **Design Requirements**

Requirement	Version
Hardware	
RTG4 Development Kit • USB A to Mini-B cable	Rev B or later
Host PC or Laptop	64-bit Windows 7 and 10
Software	
Libero® System-on-Chip (SoC)	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this reference design.
FlashPro Express	
Host PC Drivers	*USB to UART drivers*
Framework	*Microsoft.NET Framework 4 Client for launching demo GUI*

Note: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

2.2 Prerequisites

Before you start:

1. Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location: *https://www.microsemi.com/product-directory/design-resources/1750-libero-soc*
2. Before you start demo, download the design files from the following path: *http://soc.microsemi.com/download/rsc/?f=rtg4_dg0630_df*
3. If the USB to UART bridge drivers are not installed, download and install the drivers from *www.microsemi.com//documents/CDM_2.08.24_WHQL_Certified.zip*.

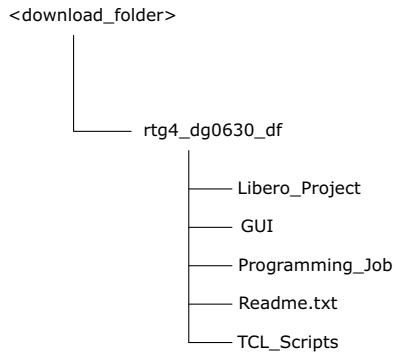
2.3 Demo Design

The design files include:

- Design Files
- GUI
- Programming Files
- TCL_Scripts
- Readme.txt file

The following figure shows the top-level structure of the design files. Refer to the `Readme.txt` file provided in the demo design folder for the complete directory structure.

Figure 2 • **Demo Design Files Top-Level Structure**



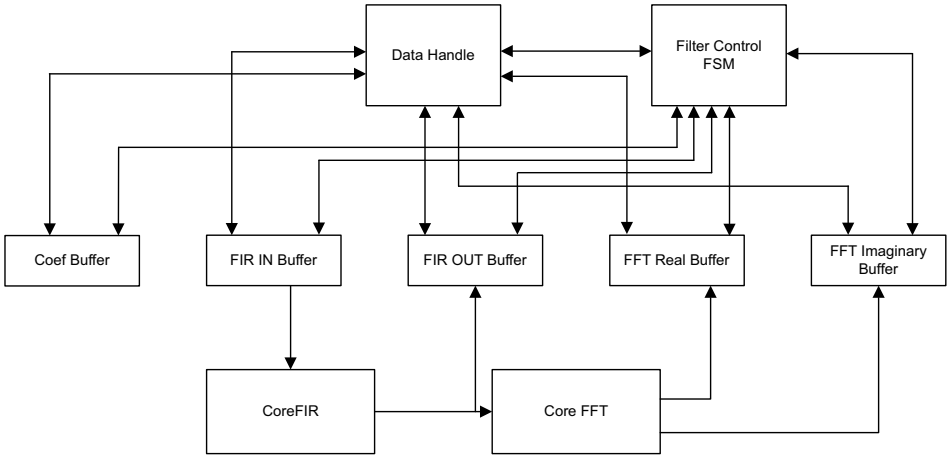
2.4 Design Description

This demo design uses the following blocks:

- Data Handle, page 4 (user RTL)
- Filter Control FSM, page 4 (user RTL)
- TPSRAM IP, page 5 (IP core)
- CoreUART, page 5 (IP core)
- CoreFIR, page 5 (IP core)
- CoreFFT, page 5 (IP core)
- SYSRESET, page 5 (IP core)
- OSC, page 6 (IP core)
- RTG4FCCCECALIB_C0, page 6 (IP core)

The following figure shows the illustrated block diagram of the demo design.

Figure 3 • **DSP FIR Filter Demo Design Block Diagram**



2.4.1 Data Handle

Data handle consists of the **CoreUART** IP and the UART interface finite state machine handling the control operations between the host PC (GUI interface) and the fabric logic. Control operations include the loading of filter coefficients, filter input data to the corresponding input data buffer, coefficient buffers, and send and receive data from the host PC GUI.

2.4.2 Filter Control FSM

Filter Control controls the FIR filter and the FFT operations. It loads the filtered data to the corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

2.4.3 TPSRAM IP

TPSRAM IP uses the following configurations:

- Filter coefficient buffer
- Input signal data buffer
- Output signal buffer
- Output signal FFT real data buffer
- Output signal FFT imaginary data buffer

Table 2 • **TPSRAM Configuration for Data Buffers**

Buffer	Write Port		Read Port	
	Depth	Width	Depth	Width
Filter Coefficients	256	8	128	16
FIR Input Signal	2048	8	1024	16
FIR Output Signal	1024	16	1024	16
FFT Output Real Signal	256	16	256	16
FFT Output Imaginary Signal	256	16	256	16

2.4.4 CoreUART

The **CoreUART IP** is used to transfer the data between the host PC (GUI) and RTG4. The **CoreUART** configuration is as follows:

- TxFIFO: Disable TxFIFO
- RxFIFO: Disable RxFIFO
- RxLegacyMode: Disable
- Baud rate: 115200
- Number of bits: 8
- Stop bits: 1
- Parity: None

2.4.5 CoreFIR

The **CoreFIR** IP is used in the re-loadable coefficient mode to support Low-pass, High-pass, Band-pass, and Band-reject filters. The **CoreFIR** IP configuration is as follows:

- Filter Type: Single rate fully enumerated
- Number of Taps: 127
- Coefficients Type: Reloadable
- Coefficients Bit Width: 16 (signed)
- Data Bit Width: 16 (signed)
- Filter Structure: Transposed with symmetry

2.4.6 CoreFFT

The **CoreFFT** IP is used for generating the frequency spectrum of the filtered data. **CoreFFT** IP Configuration is as follows:

- FFT Architecture: In place
- FFT Type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

2.4.7 SYSRESET

The **SYSRESET** IP provides the power on reset signal.

2.4.8 OSC

The **OSC** IP is configured as an RC oscillator to provide the 50 MHz signal to the clock conditioning circuit (CCC).

2.4.9 RTG4FCCCECALIB_C0

The RTG4FCCCECALIB_C0 IP is configured to provide a 100 MHz clock signal. For detailed smart design implementation and resource usage summary, refer to Appendix 3: SmartDesign Implementation, page 29 Demo Flow.

2.5 Resource Usage Summary

The following table shows usage summary of DSP FIR filter design resource utilization.

Table 3 • **DSP FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
4LUT	5497	151824	3.62
DFF	8621	151824	5.68
RAM64x18	0	210	0
RAM1Kx18	12	209	5.74
MACC	68	462	14.72

The following table shows usage summary of MACC blocks.

Table 4 • **MACC Blocks Usage Summary**

CoreFIR	CoreFFT	Total
64	04	68

The following table shows usage summary of RAM1Kx18 blocks.

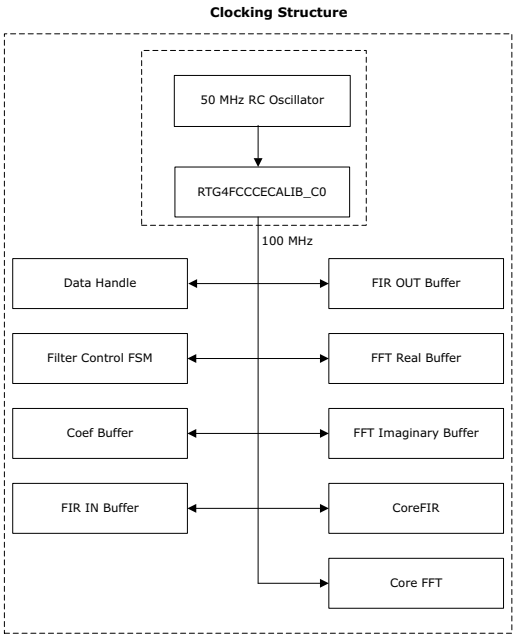
Table 5 • **RAM 1Kx18 Blocks Usage Summary**

CoreFIR	CoreFFT	Fabric Buffers	Total
0	7	5	12

2.6 Clocking Structure

In this demo design, there is only one clock domain. 50 MHz RC oscillator is connected to the RTG4FCCCECALIB block, which generates a 100 MHz clock.

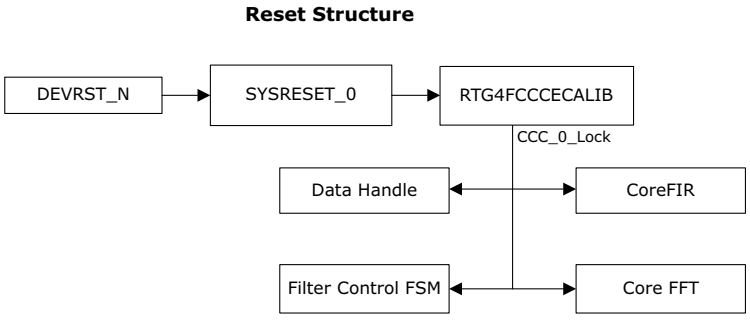
Figure 4 • **Clocking Structure**



2.7 Reset Structure

In this demo design, the reset signal is generated using a SYSRESET module, which is then synchronized using the RTG4FCCCECALIB block.

Figure 5 • **Reset Structure**



2.8 Setting Up the Demo Design

2.8.1 Setting Up the Hardware

The following steps describe how to set up the hardware demo:

1. Ensure that the board is powered **OFF** using the **SW6** switch.
2. Connect the jumpers on the RTG4 Development Kit board, as shown in the following table.

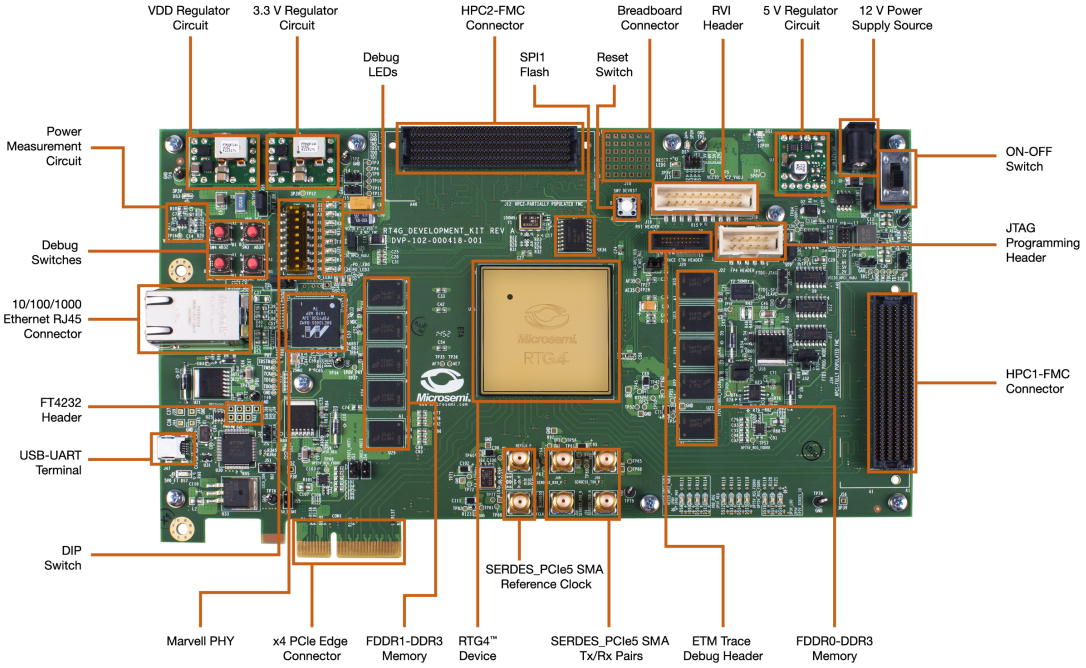
Table 6 • **RTG4 Development Kit Jumper Settings**

Jumper	Location	Purpose	Setting
J16	Above **SW3**	Select VDD core voltage	2-3 installed
J17	Below **J9** AC connector	Select either **SW6** input or signal **ENABLE_FT4232** from **FT4232H** chip	1-2 installed
J19	Below **J9** AC connector		1-2 installed
J21	To the right of the dip switch bank	Bank 7 supply voltage	1-2 installed
J23	To the right of the FlashPro4 programming header		1-2 installed
J26	Below ETM Trace header	Bank 2 supply voltage	1-2 installed
J28	Below the dip switch bank		1-2 installed
J32	To the left of the FMC connector (HPC1)	Enable FlashPro5 for programming	2-3 installed
J33	Below FlashPro4 programming header		1-2 installed 3-4 installed

3. Connect the Power supply to the **J9** connector, switch on the power supply switch, **SW6**.
4. Connect the host PC USB port to the **J47** USB connector on the RTG4 Development Kit board using the USB Mini-B cable.

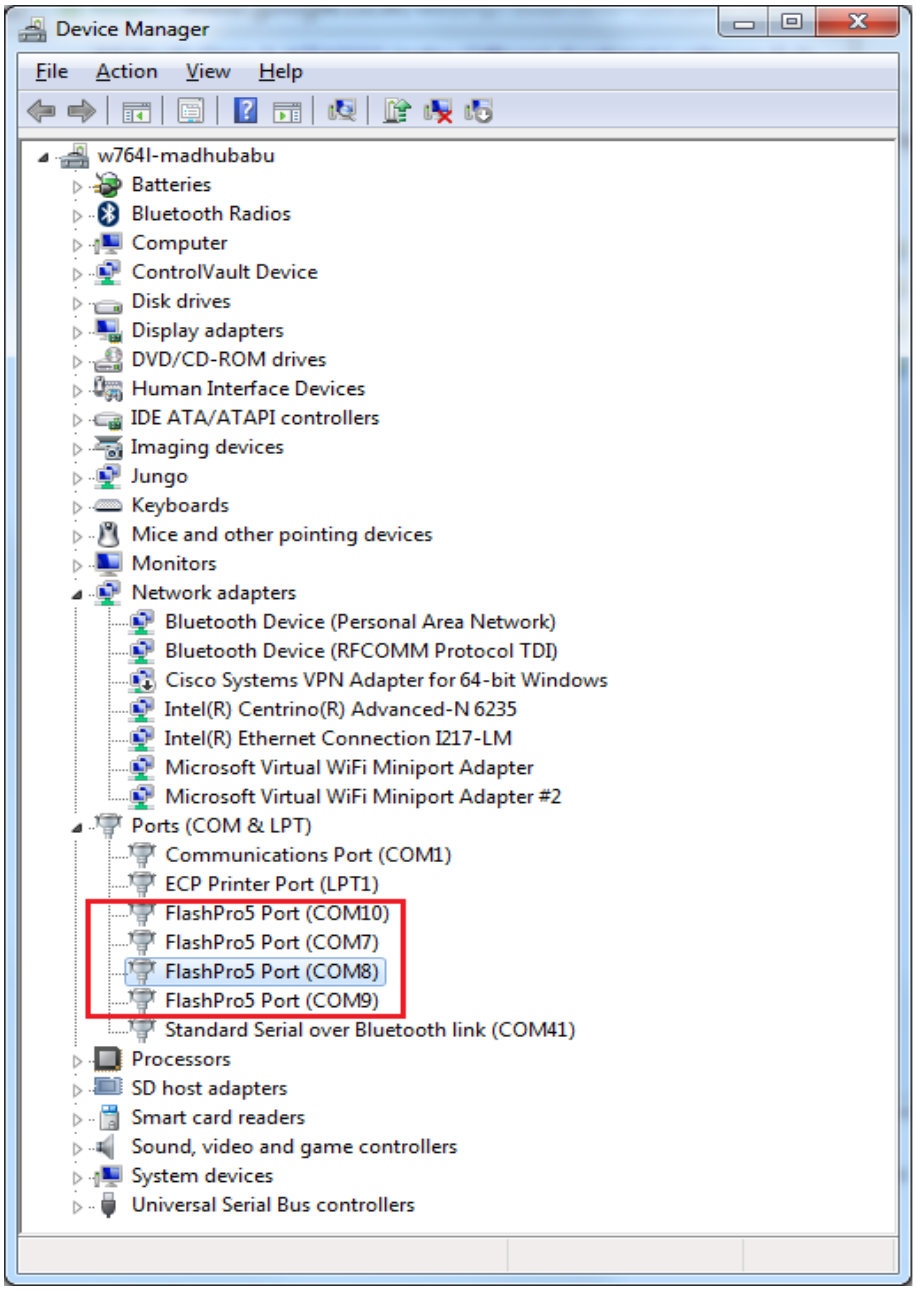
The following figure shows the board setup for running the DSP FIR Filter demo on the RTG4 Development Kit.

Figure 6 • **RTG4 Development Kit DSP FIR Filter Demo Setup**



5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the host PC. The following figure shows the USB 2.0 Serial port properties and the connected **COM6** and **USB Serial Converter C**.

Figure 7 • **USB to UART Bridge Drivers**



6. If the USB to UART bridge drivers are not installed, download and install the drivers from *www.microsemi.com//documents/CDM_2.08.24_WHQL_Certified.zip*.

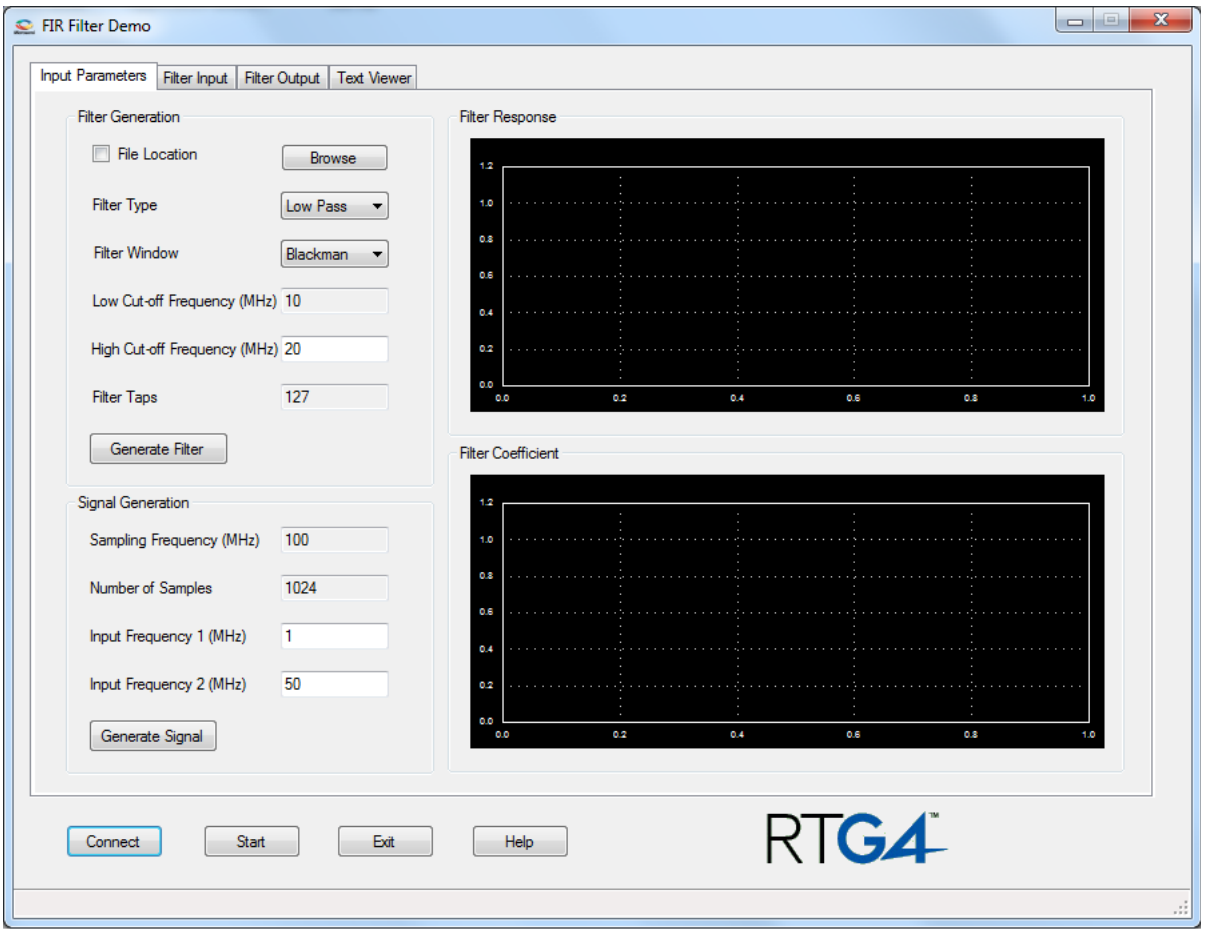
2.8.2 Programming the Device

To program the RTG4 Development Kit with the job file provided as part of the design files using FlashPro Express software, refer to Appendix 1: Programming the Device Using FlashPro Express, page 25.

2.8.3 DSP FIR Demo GUI

The DSP FIR demo is provided with a user-friendly GUI that runs on the host PC which communicates with the RTG4 Development Kit. The UART is used as the communication protocol between the host PC and RTG4 Development Kit. The following figure shows the DSP FIR demo GUI.

Figure 8 • **DSP FIR Demo Window**



The DSP FIR demo window consists of the following tabs:

- **Input Parameters:** Filter generation and signal generation
- **Filter Input:** Plots the input signal and its frequency spectrum
- **Filter Output**: Plots the output signal and its frequency spectrum
- **Text Viewer:** Shows the coefficients, input signal, output signal, and FFT data values

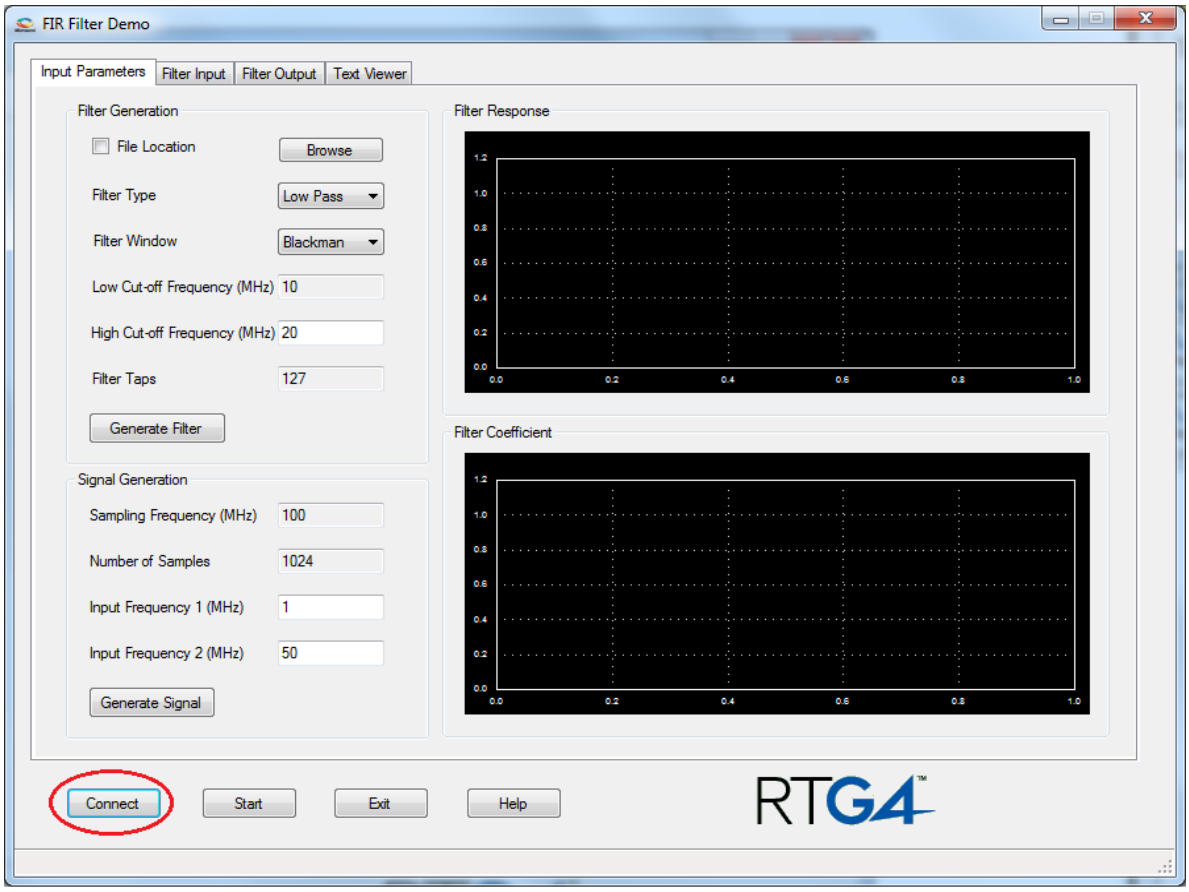
2.9 Running the Demo Design

The following steps describe how to run the demo design:

To run the demo:

1. Launch the DSP FIR Demo GUI executable file available in the design files. (`\rtg4_dg0630_df\GUI\RTG4_FIR_Filter.exe`).
2. The FIR Filter Demo window is displayed, as shown in the following figure.

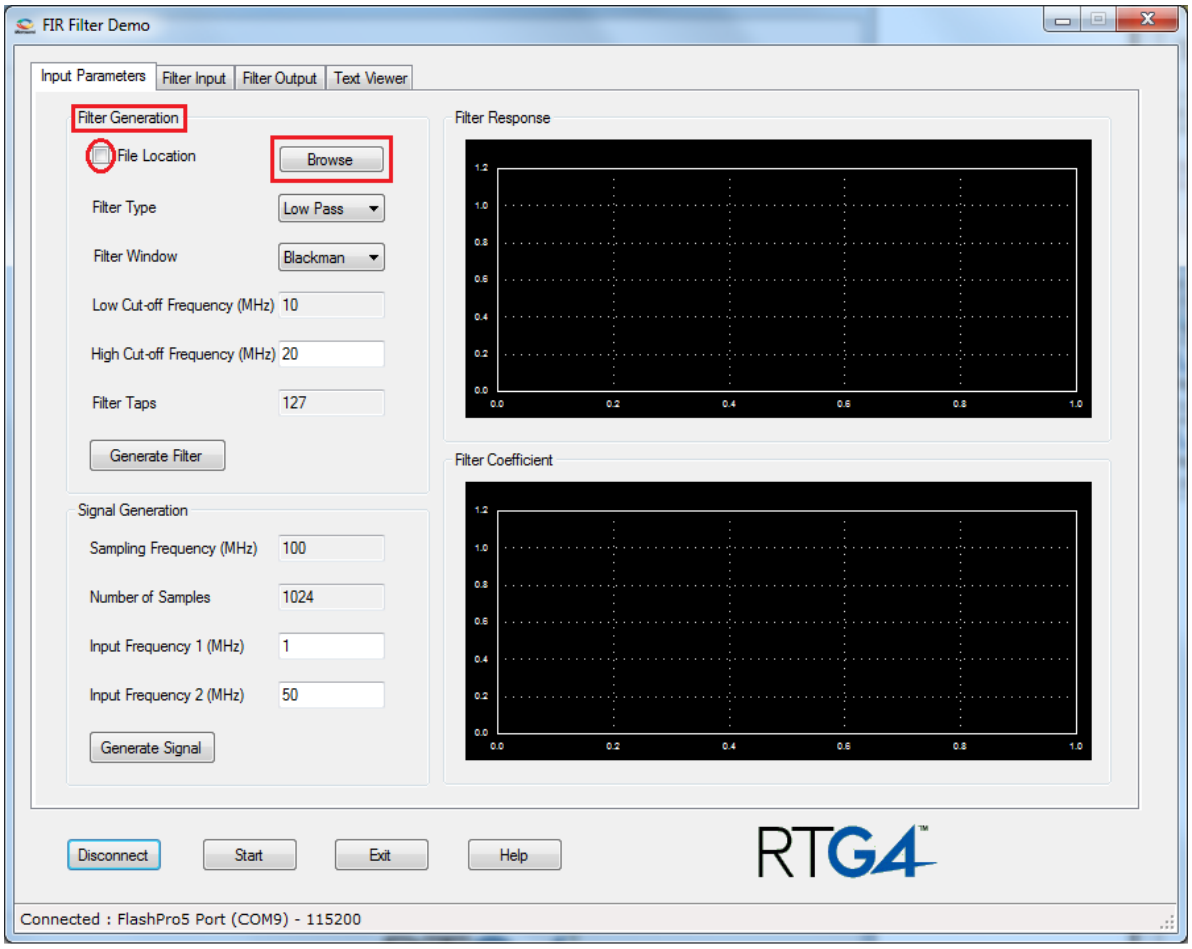
Figure 9 • **Serial Port Configuration**



3. **Serial Port Configuration**: Click **Connect**, the COM port number is automatically detected and the baud rate is fixed at 115200 as shown in the preceding figure.

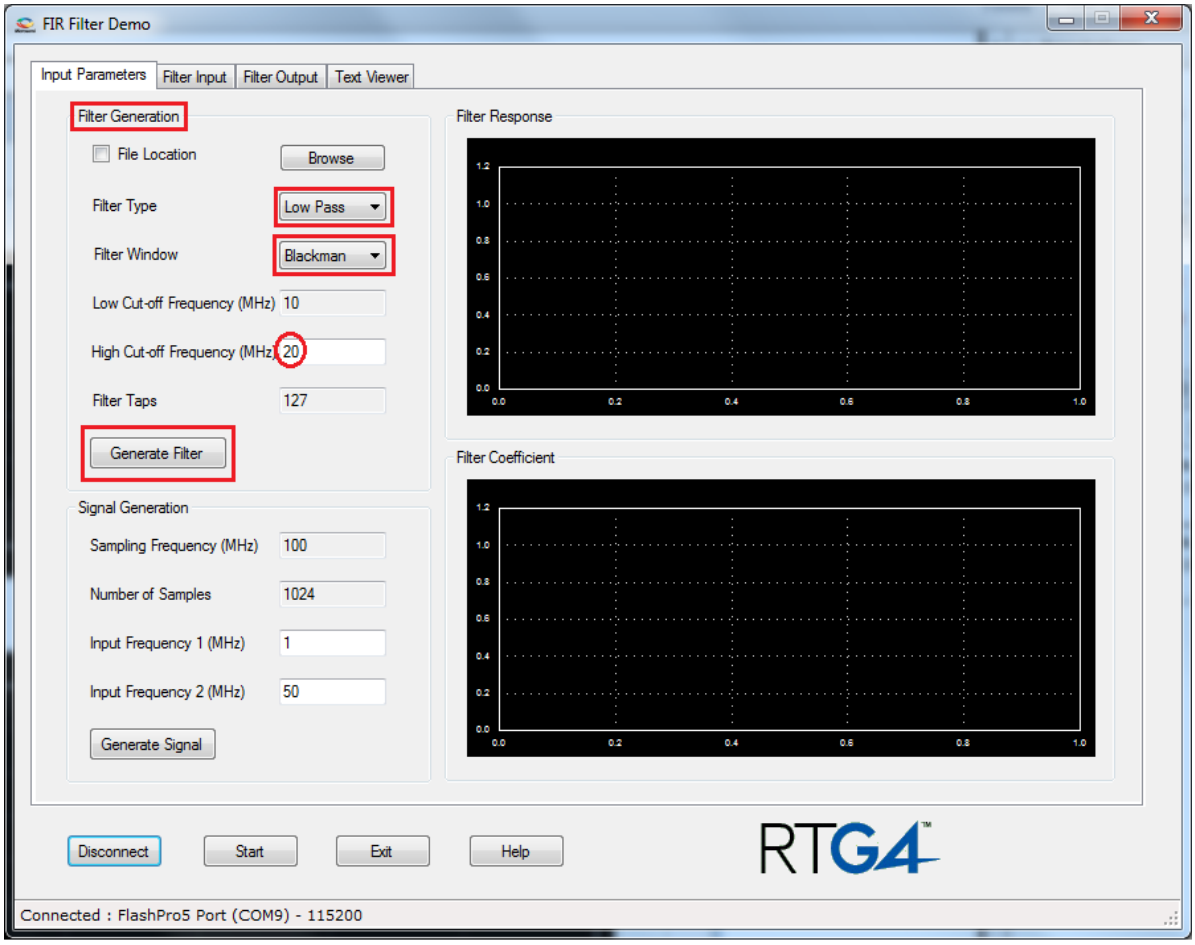
4. **Filter Generation:** Two options are provided for generating the filter coefficients:
   - Generate the coefficients using MATLAB or any similar tool and save it as a text file. Refer to Appendix 4: Coefficient Text File Format, page 30 for the format of the text file. The GUI can be used to browse and load this file as shown in the following figure.

Figure 10 • **Filter Generation - 1**



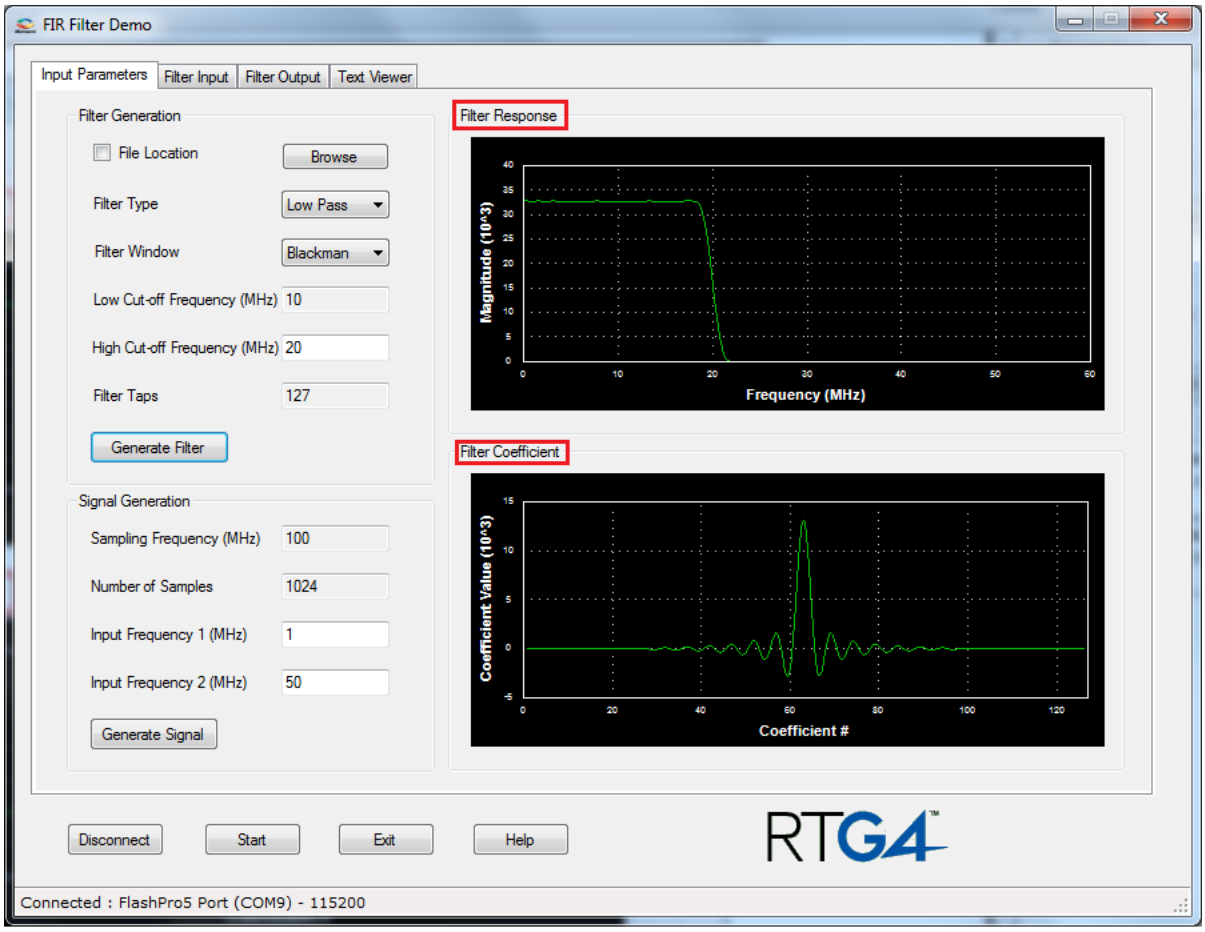
- Generate the Filter coefficients using the GUI as given below:
  The following parameters are required to generate filter coefficients as shown in the following figure.
  - **Filter type:** Low-pass(Low-pass/High-pass/Band-pass/Band-reject filter)
  - **Filter Window:** Blackman (Blackman/Hamming window)
  - **Low Cut-off Frequency:** Disabled for Low-pass filter required (High cut-off frequency is disabled for High-pass filter)
  - **High Cut-off Frequency:** 20 MHz
  - **Filter Taps:** 127 (Fixed)
    Click **Generate Filter** to generate the filter coefficients.

Figure 11 • **Filter Generation - 2**



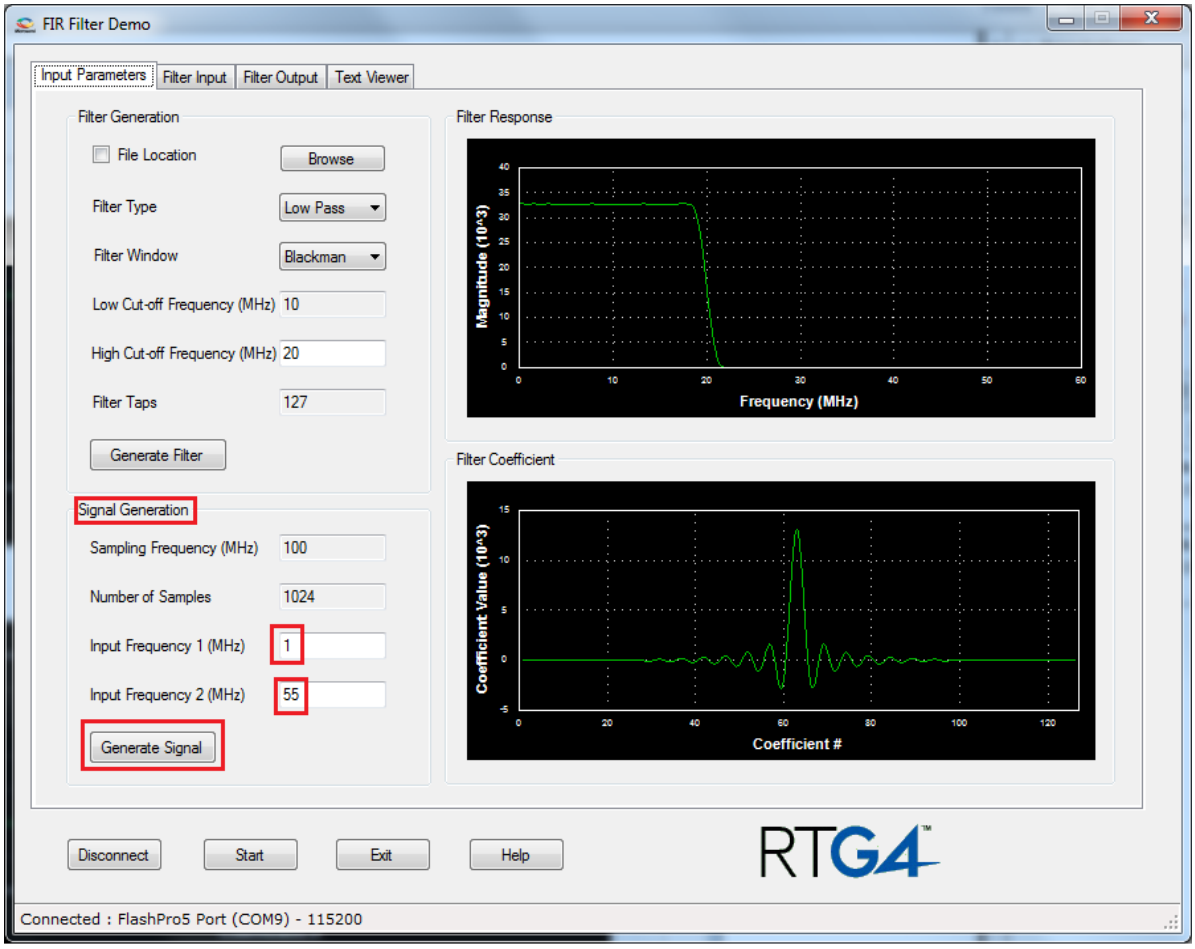
The successful after generation graphs of the filter coefficients, filter response, and the filter coefficient plots are displayed in the following figure.

Figure 12 • **Filter Response and Filter Coefficient Plot**



5. **Signal Generation**:
   - **Sampling Frequency**: 100 MHz (Fixed)
   - **Number of Samples**: 1024 (Fixed)
   - **Input Frequency 1**: Enter the signal frequency in the Pass-band region. For example, 1 MHz is set to High cut-off frequency
   - **Input Frequency 2**: Enter the signal frequency in the Stop-band region. For example, High cut-off frequency is set to Sampling frequency/2
   - Click **Generate Signal** as shown in the following figure.

Figure 13 • **Signal Generation**

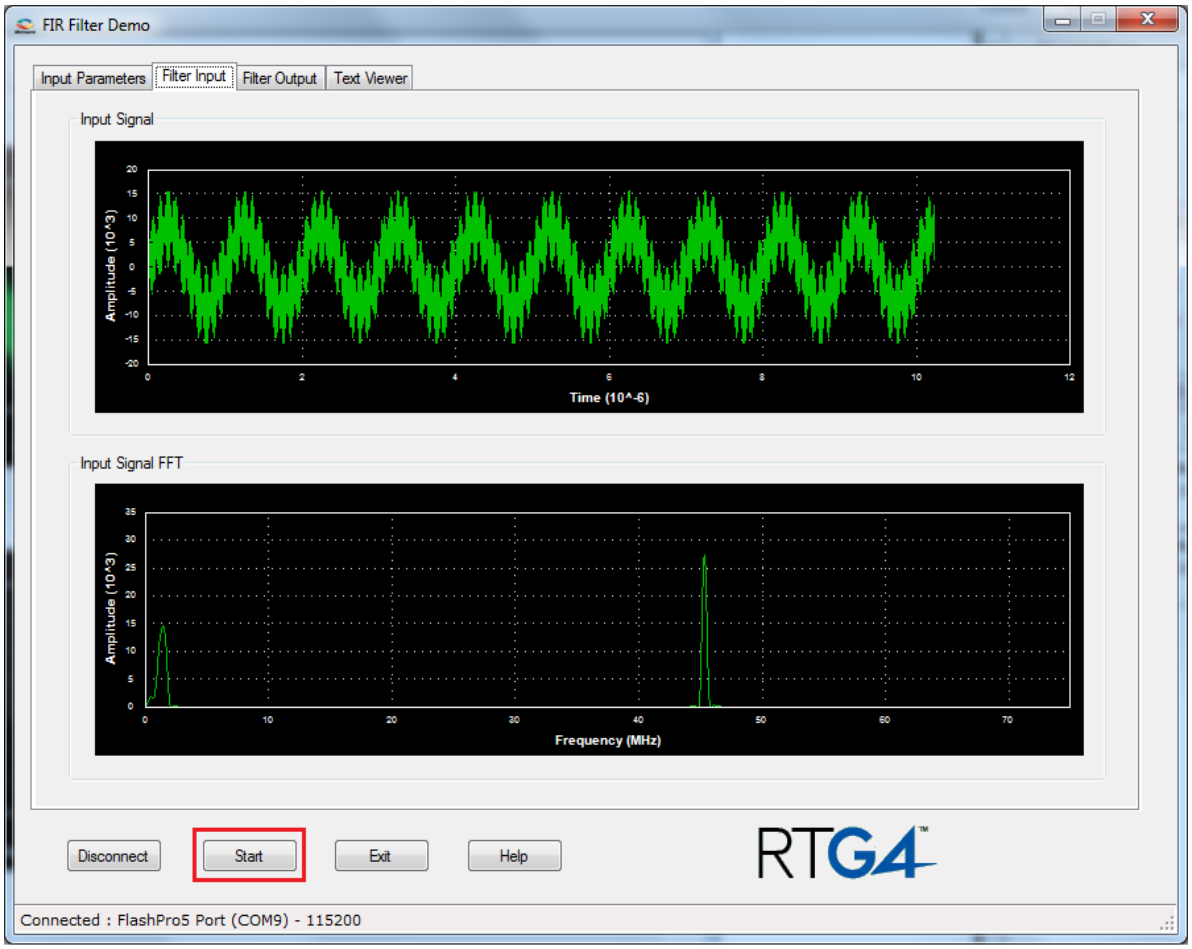


Input signal and frequency spectrum of the specified signal is displayed, as shown in the following figure.

Figure 14 • **Input Signal and Input Signal FFT Plot**

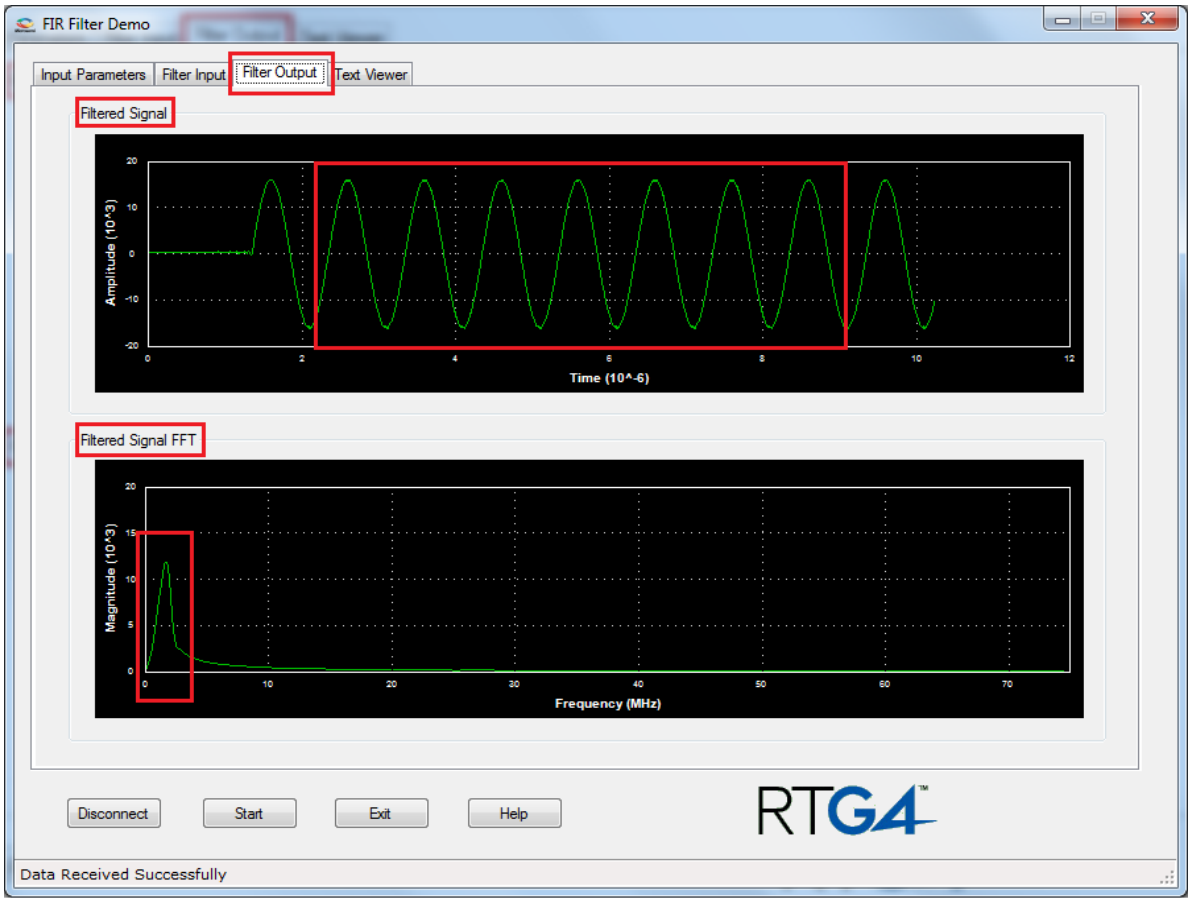
6. To configure the input frequencies and coefficients, click **Start**, as shown in the following figure. It sends the input data (1 K samples) and filter coefficients to the RTG4 device for processing the filtering operation.

Figure 15 • **DSP FIR Filter Demo - Start**



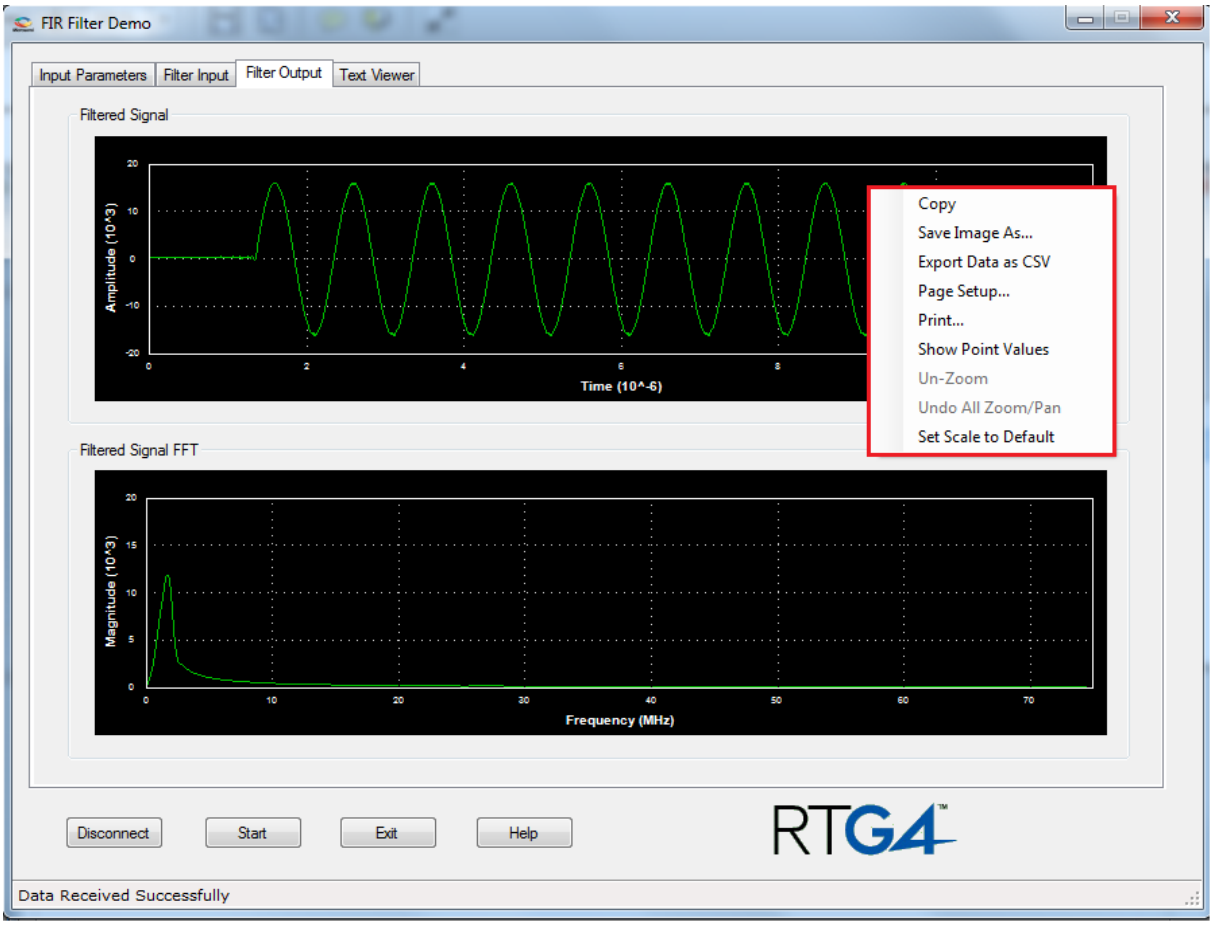
After completing the filter operation by the RTG4 device, the GUI plots the filtered data and the FFT data on the filter output window as shown in the following figure. Since the Low-pass filter option was selected, the High frequency component is suppressed while the Low frequency signal is preserved. This can be observed in the frequency spectrum of the output signal.

Figure 16 • **Filtered Signal: Time and Frequency Plot**



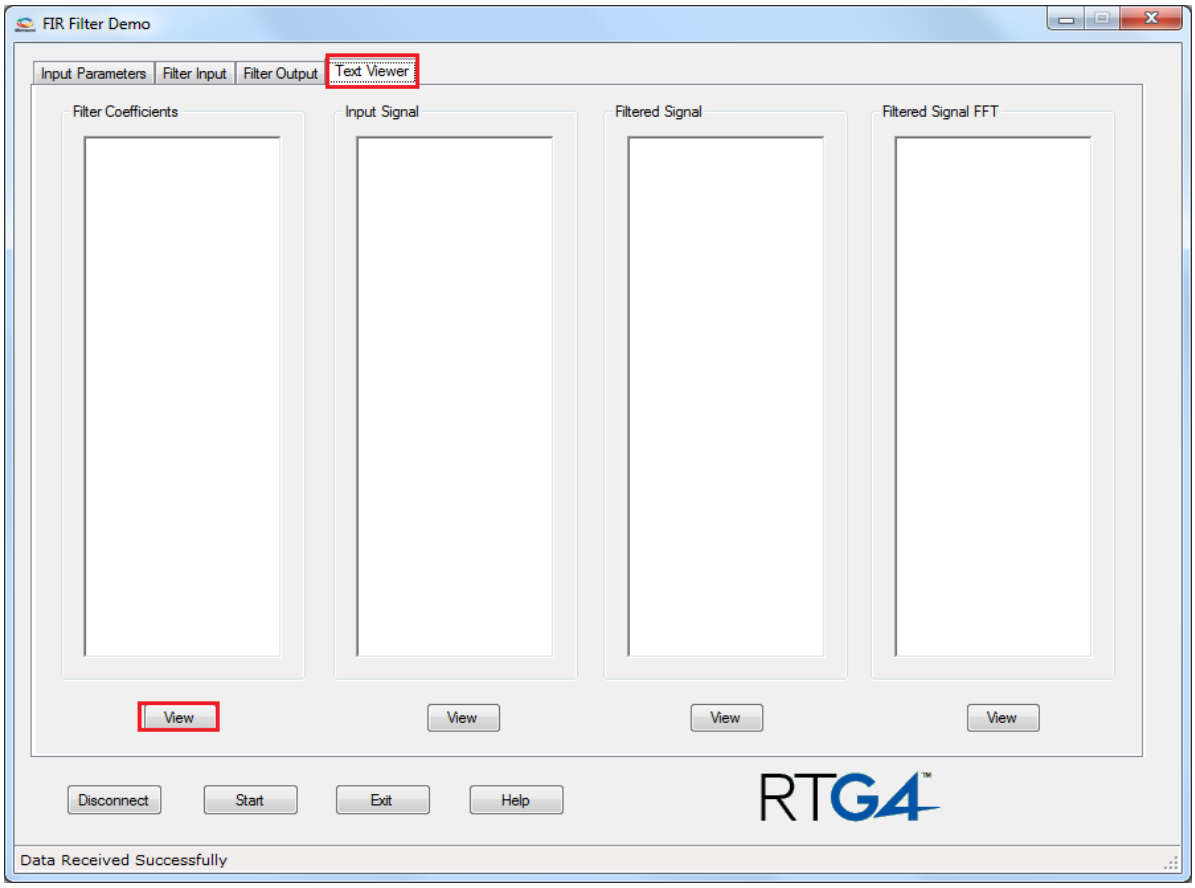
7. Right-click on the window, it shows different options as shown in the following figure. The data can be copied, saved, and exported to the CSV plot for analysis purpose. Page setup, print, show point values, zoom, and set scale are set to default.

Figure 17 • **Filtered Signal: GUI Options**



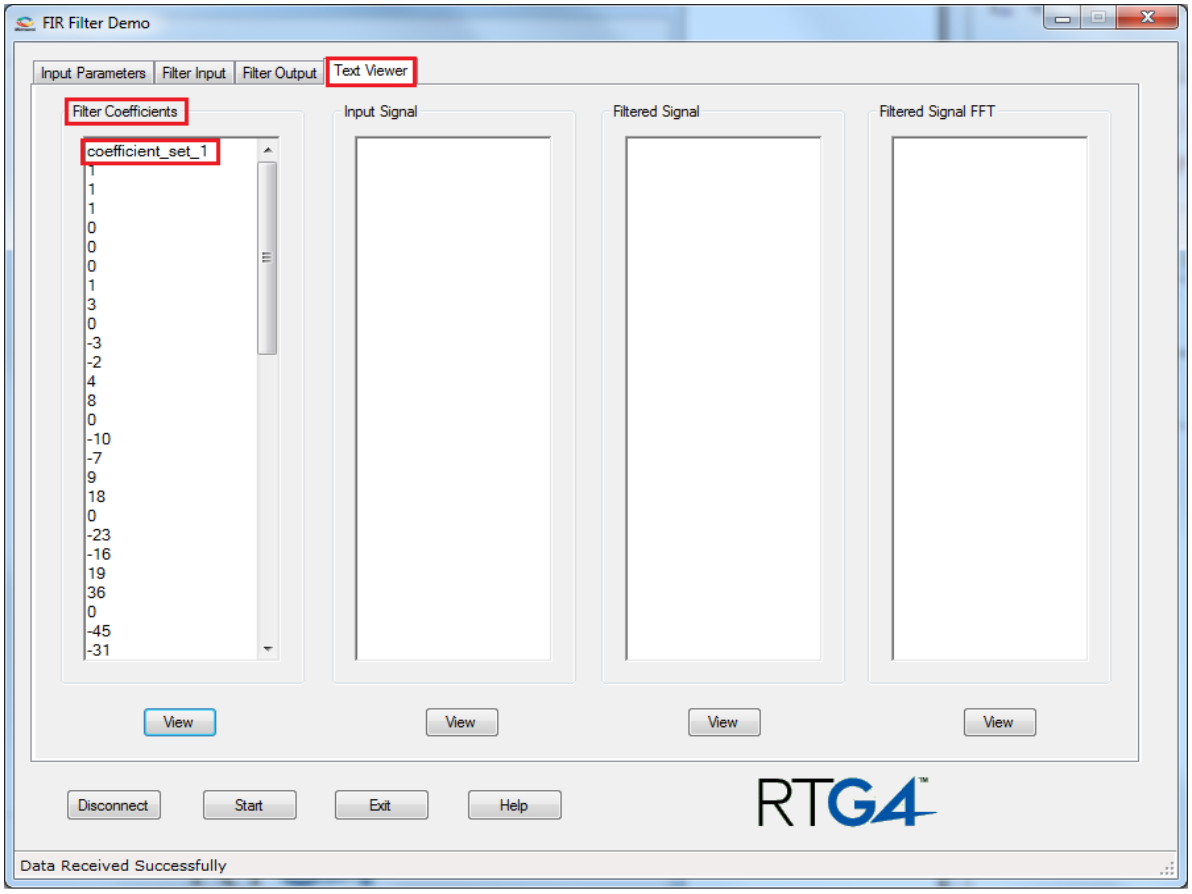
8. The filter coefficients, input signal, output signal, and FFT output data values can be viewed in the **Text viewer**.
9. Click **Text Viewer** and click the corresponding **View**, as shown in the following figure.

Figure 18 • **Text Viewer**



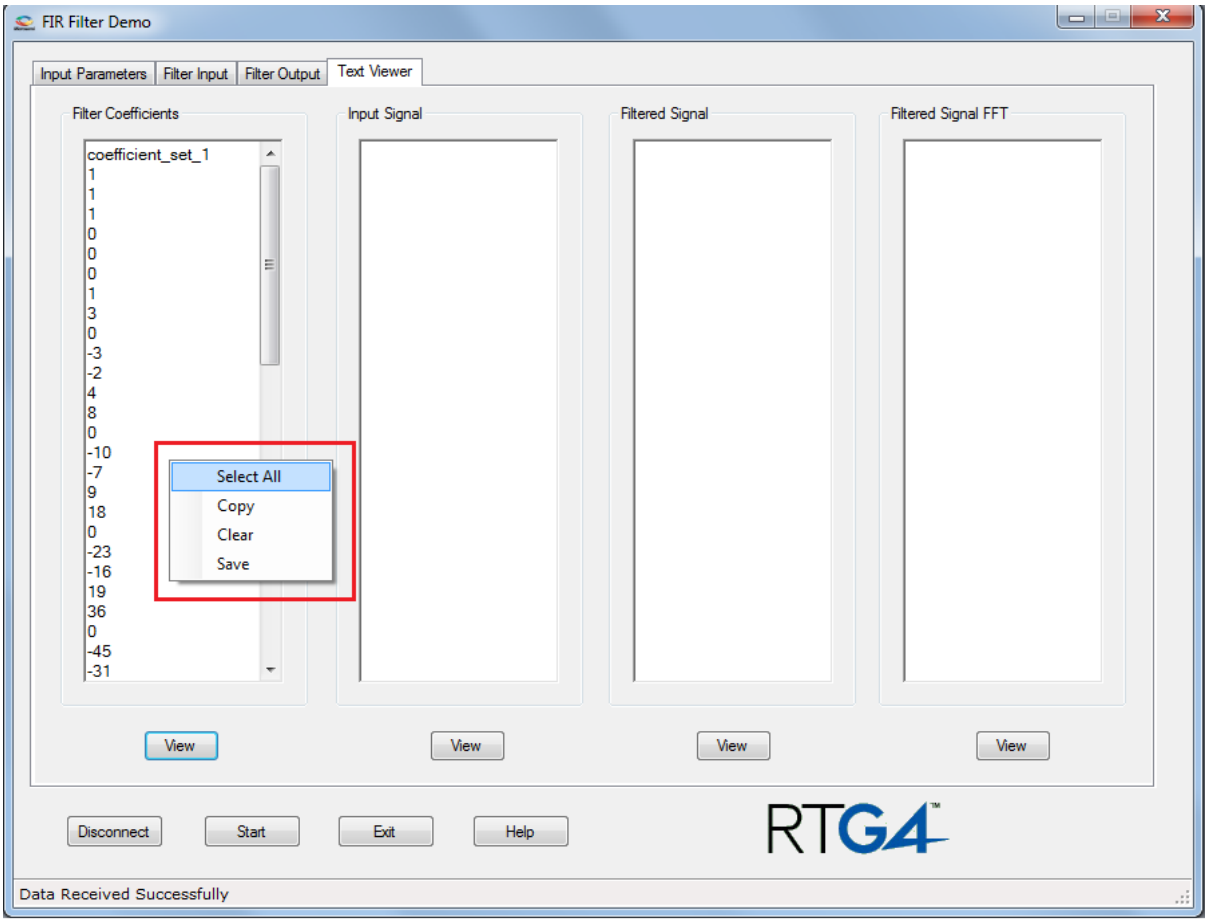
The values can be observed, as shown in the following figure.

Figure 19 • **Text Viewer: Filter Coefficient Values**



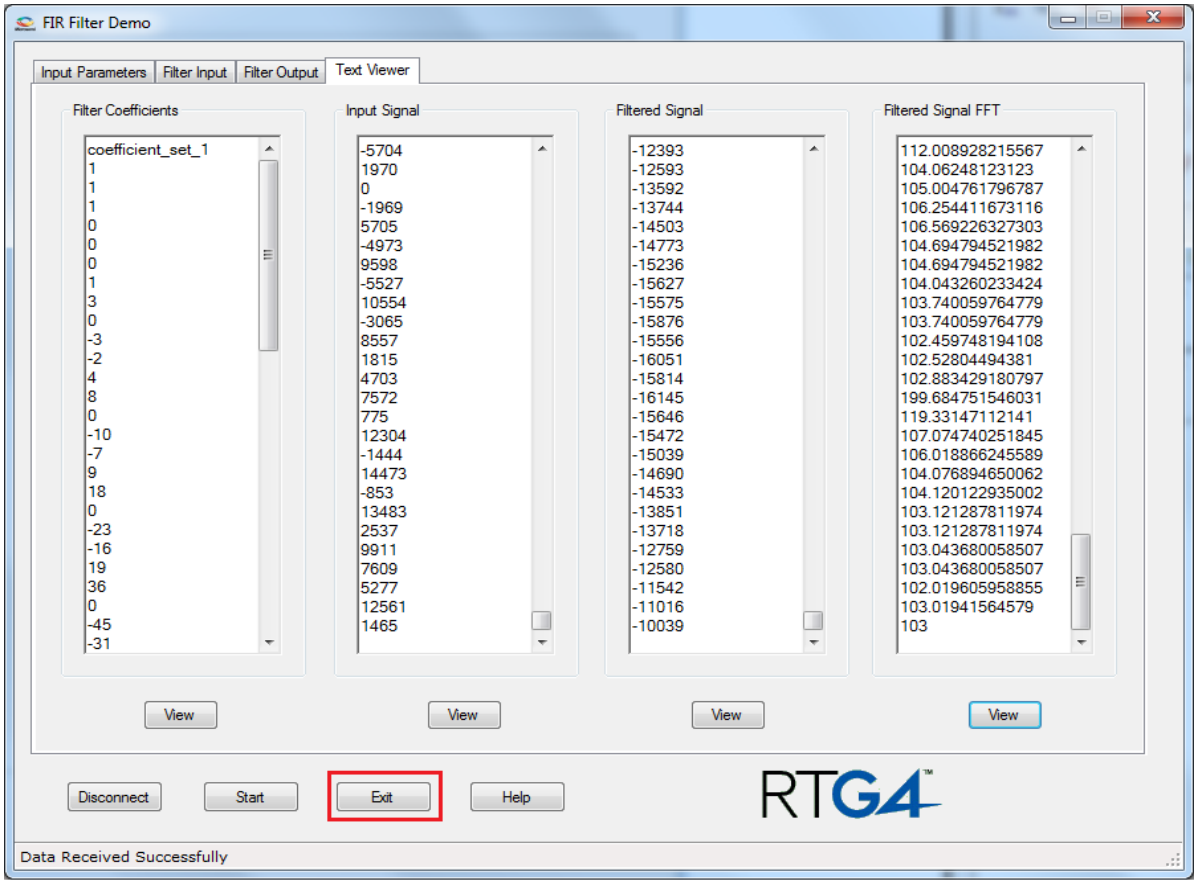
10. To save the coefficients as a text file, right-click the **Filter Coefficients** window, it shows different options, as shown in the following figure.
11. Click **Save**. Select **OK** to save the text file.

Figure 20 • **Text Viewer: Coefficients Save Options**



12. Click **Exit** to stop the demo as shown in the following figure.

Figure 21 • **FIR Filter Demo: Exit**



2.10 Conclusion

This demo shows the features of the RTG4 device including Mathblocks, and LSRAMS for DSP specific applications and provides information on how to use the Microsemi DSP IP cores (CoreFIR and CoreFFT). This FIR filter GUI-based demo is very easy to use and provides several options to understand and implement the DSP filters on the RTG4 device.

3 Appendix 1: Programming the Device Using FlashPro Express

This section describes how to program the RTG4 device with the programming job file using FlashPro Express.

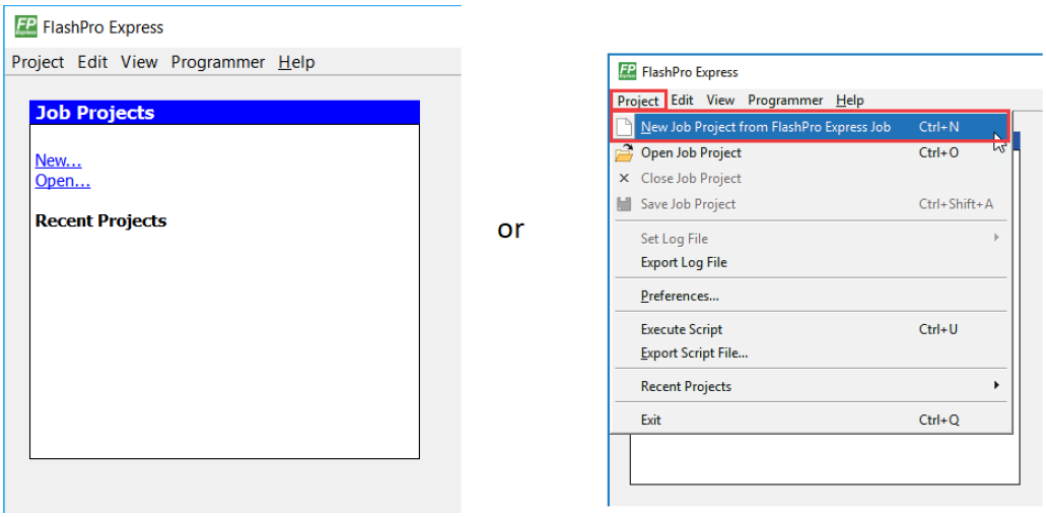
To program the device, perform the following steps:

1. Ensure that the jumper settings on the board are the same as those listed in *Table 3 of UG0617: RTG4 Development Kit User Guide*.
2. Optionally, jumper **J32** can be set to connect pins 2-3 when using an external FlashPro4, FlashPro5, or FlashPro6 programmer instead of the default jumper setting to use the embedded FlashPro5.

Note: The power supply switch, **SW6** must be switched **OFF** while making the jumper connections.

3. Connect the power supply cable to the **J9** connector on the board.
4. Power **ON** the power supply switch **SW6**.
5. If using the embedded FlashPro5, connect the USB cable to connector **J47** and the host PC. Alternatively, if using an external programmer, connect the ribbon cable to the JTAG header **J22** and connect the programmer to the host PC.
6. On the host PC, launch the **FlashPro Express** software.
7. Click **New** or select **New Job Project from FlashPro Express Job** from **Project** menu to create a new job project, as shown in the following figure.

Figure 22 • **FlashPro Express Job Project**



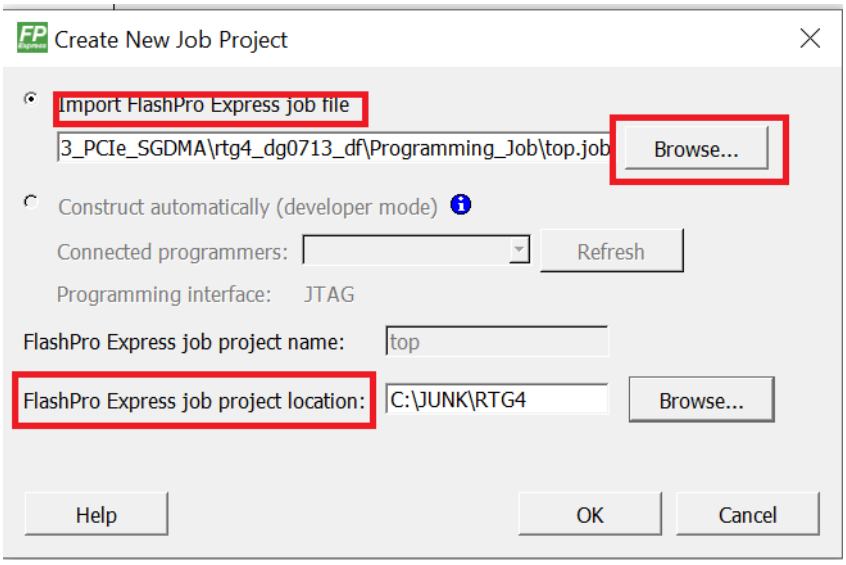
8. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:

- **Programming job file:** Click **Browse**, and navigate to the location where the .job file is located and select the file. The default location is:

  `<download_folder>\rtg4_dg0630_df\Programming_Job`

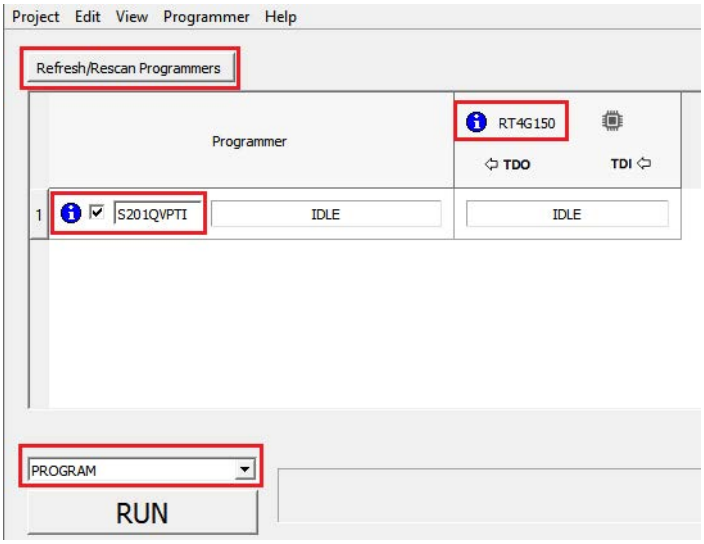
- **FlashPro Express job project location:** Click **Browse** and navigate to the desired FlashPro Express project location.

Figure 23 • **New Job Project from FlashPro Express Job**



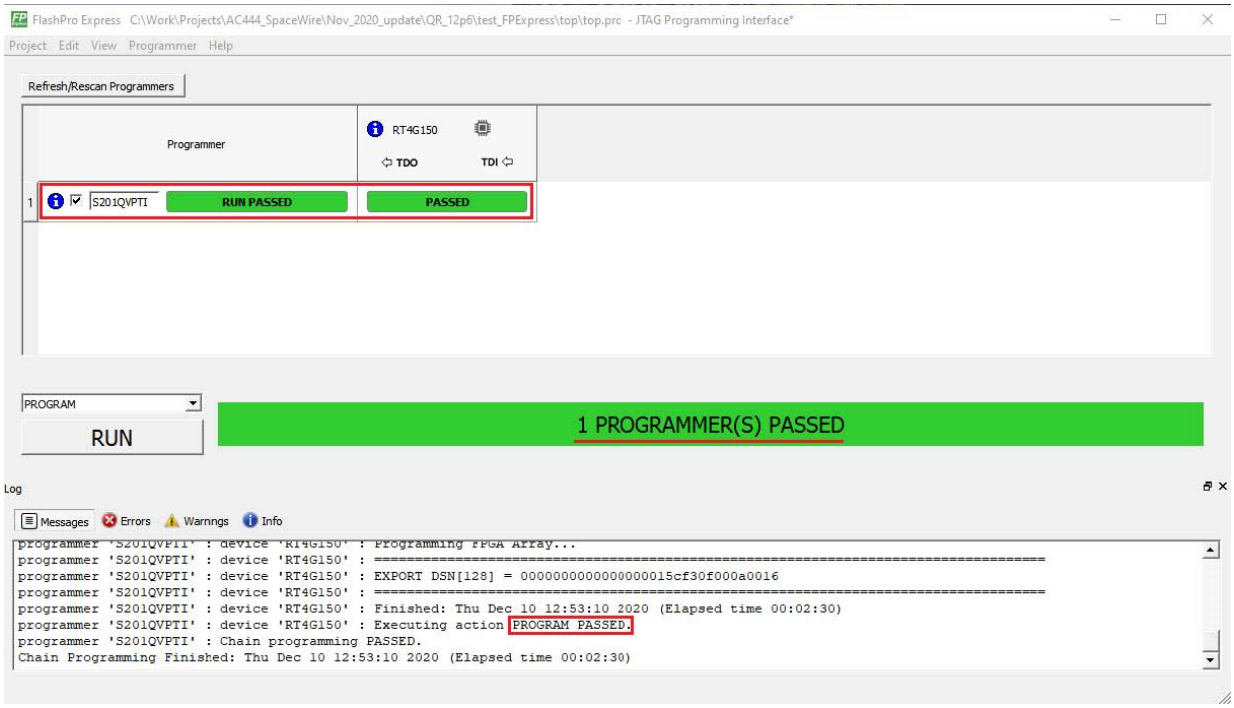
9. Click **OK**. The required programming file is selected and ready to be programmed in the device.
10. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan** Programmers.

Figure 24 • **Programming the Device**



11. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

Figure 25 • **FlashPro Express—RUN PASSED**



12. Close **FlashPro Express** or click **Exit** in the Project tab.

4 Appendix 2: Running the TCL Script

TCL scripts are provided in the design files folder under directory TCL_Scripts. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, follow the steps below:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click Browse and select `script.tcl` from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within TCL_Scripts directory.

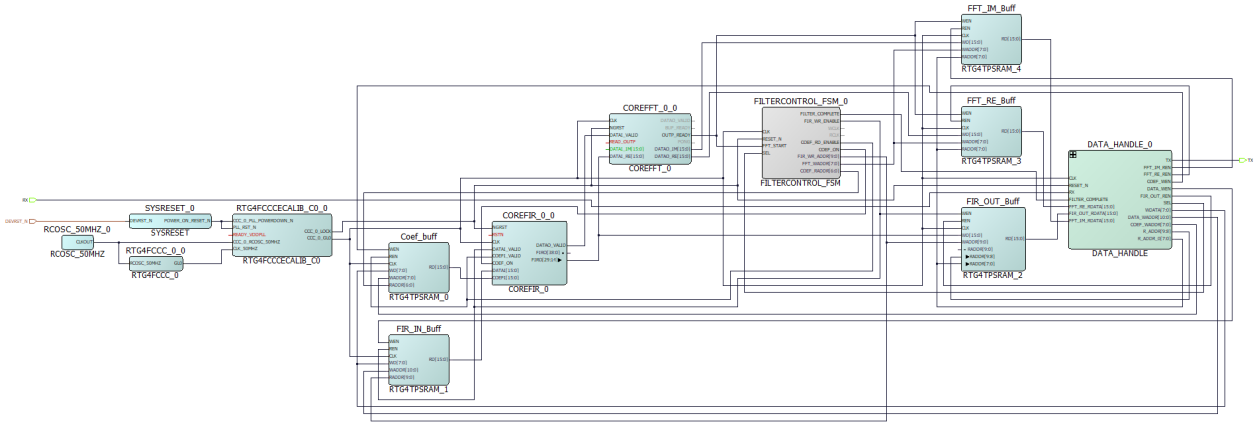
For more information about TCL scripts, refer to **rtg4_dg0630_df/TCL_Scripts/readme.txt.**

Refer to *Libero® SoC TCL Command Reference Guide* for more details on TCL commands. Contact Technical Support for any queries encountered when running the TCL script.

5 Appendix 3: SmartDesign Implementation

The following figure shows DSP FIR filter SmartDesign.

Figure 26 • **DSP FIR Filter SmartDesign**



The following figure shows SmartDesign blocks in DSP FIR Filter.

Table 7 • **DSP FIR Filter Demo SmartDesign Blocks and Description**

S.No	Block Name	Description
1	DATA_HANDLE_0	Handles the communication between the host PC and the RTG4 Development Kit board
2	FILTERCONTROL_FSM_0	Control logic to generate the control signals for the FIR and FFT operations
3	Coef_Buff IP	IP for the filter coefficient buffer
4	FIR_IN_Buff	IP for the FIR input signal data buffer
	FIR_OUT_Buff	IP for the FIR output signal data buffer
	FFT_Re_Buff	IP for the FIR output real data buffer
	FFT_Im_Buff	IP for the FIR output imaginary data buffer
5	COREFIR_0	COREFIR IP
6	COREFFT_0	COREFFT IP
7	SYSRESET_0	Reset IP
8	OSC_0	Oscillator IP
9	RTG4FCCCECALIB_C0	Clock Conditioning circuit IP

6 Appendix 4: Coefficient Text File Format

The FIR filter coefficients can be loaded from an ASCII text file (*.txt). Create the coefficient file using a text editor. The format of the text file should be as shown in the following figure. The coefficient values must be entered as integer numbers. For a symmetric or anti-symmetric filter, only half of the coefficients must be listed in the file (this applies to the Fully Enumerated type only). Only one coefficient value per line is permitted. An extra empty line must be placed after the last coefficient of the last set.

Figure 27 • **Coefficient File Example – 9 Taps, Decimal Values**