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Microsemi

# Building High Reliability into Microsemi Designs with Synplify FPGA Tools

Microsemi Space Forum 2015, Synopsys

Microsemi SPACE FORUM

# Agenda

- FPGA SEU mitigation industry trends and best practices
  - Market trends
  - What's needed and when
- Current solutions
  - Overview FPGA design tools
  - Hardware debug and operation visibility
  - DO-254 support
  - SEU mitigation circuitry creation and error monitors
- New best practices → What's next?
  - Local TMR best practices
  - Validating that TMR occurred and that it works
  - Error monitoring and access
  - Solutions for Microsemi RTG4

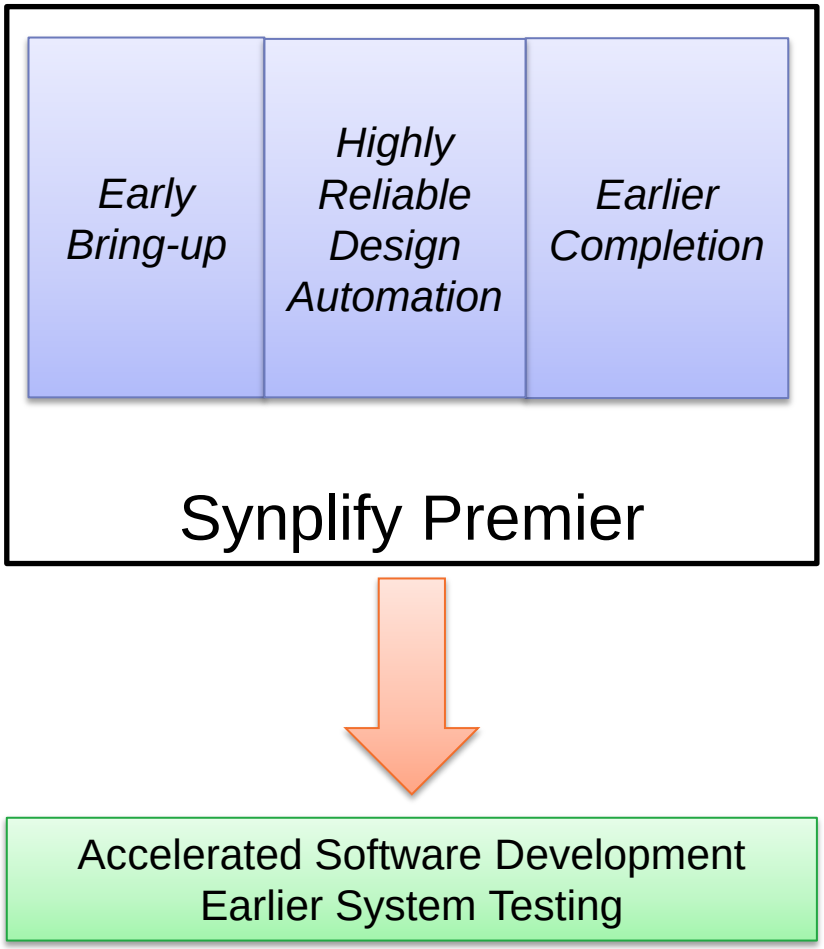


# FPGA Military/Aerospace Solutions

- Mil/Aero market trends for FPGA systems
  - Need highest datapath performance in smallest area
  - High reliability and SEU error mitigation
  - Strict processes for circuit creation and verification
  - Reliable operation in harsh and high radiation environments
  - Support for multiple FPGA vendor suppliers
- Synplify FPGA solutions provide
  - DO-254 support and process compliance
  - Debug operating design in RTL
  - Automation of high reliability design techniques
  - Highest system performance in smallest area
  - Support for Verilog, VHDL, VHDL-2008 and System Verilog

Synplify enables high reliability, fast runtimes and deep debug

# Synplify Premier offers 10x Faster Hardware Bring-up for Microsemi FPGAs

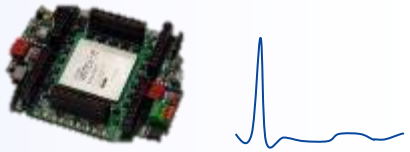



- Single-pass design debug
  - Upfront RTL and constraint checks
  - Finds all errors in a single compile
  - Diagnostic reporting
  - Fast synthesis (low QoR) mode
- Highly Reliable Automation
  - Hamming-3 error detection and correction design automation
- Quickly apply improvements
  - Hierarchical & incremental flows
  - Multi-machine synthesis

# Why is There a High Reliability Problem?

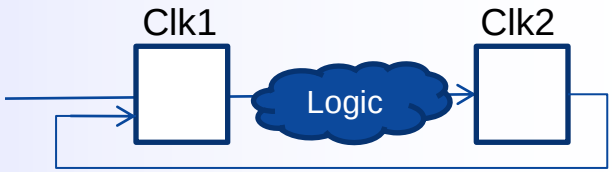
Radiation-induced circuit glitches
(SEUs, SETs)


Power rail glitch



Power supply glitch or brown-out

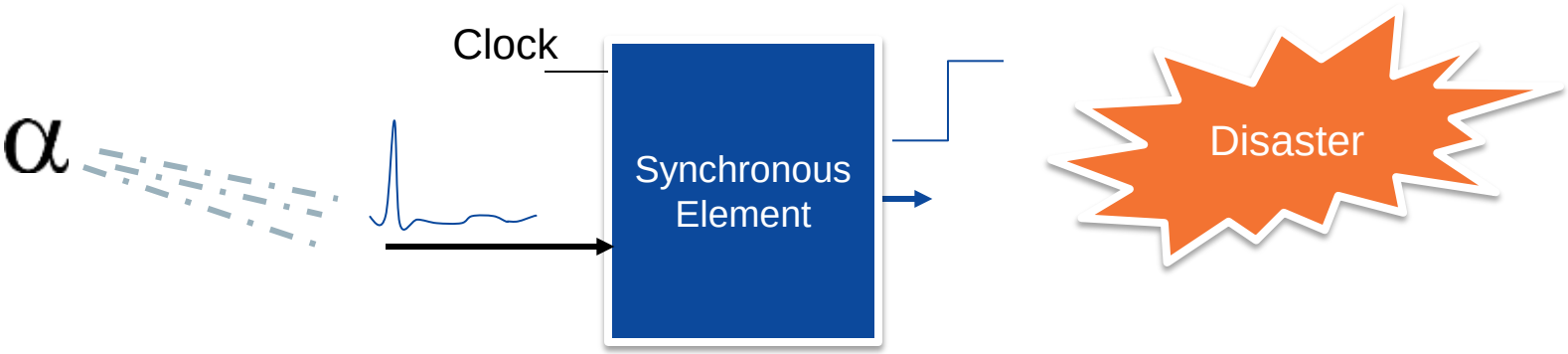
Meta-stability due to design flaws
(failure to synchronize the circuit)



# SETs and SEUs

*Glitches clocked into a synchronous element can cause operation errors and ultimately system failure*

- Impacts memories, registers, state machines




**SET** (Single Event Transient)

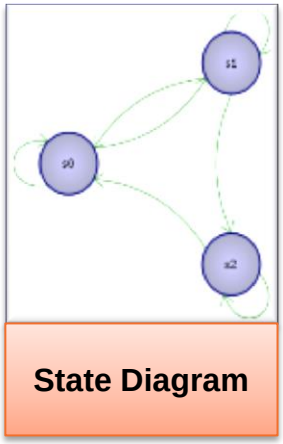
A current spike or "glitch" in a signal that occurs due to ionization or electromagnetic radiation

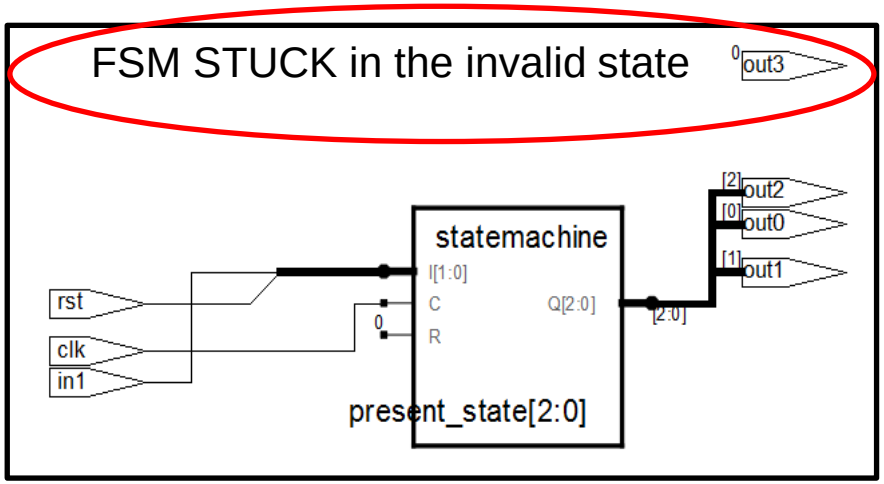
**SEU** (Single Event Upset)

Incorrect signal (SET) captured by a synchronous element that impacts its internal state and / or output

# SEUs Cause Incorrect Behavior or FSM Failure

A flip in a register bit within an FSM can cause what was assumed to be an “unreachable“ or “invalid” state to be reached




RTL others clause that would handle state transition behavior out of an unreachable state is optimized away by default by the synthesis tool

# Synplify Premier Automates Design for High Reliability

- **Monitor for Soft Errors "Bit flips"**
- **Restore Stable Operation**

Preserve Critical Circuitry

High Reliability Reporting

| | | | |
|---|---|---|---|
| Control Logic and FSMs | Safe FSMs w/ Hamming-3 | Local and Distributed TMR | |
| Memories | RAM TMR | ECC RAM Inference | Duplicate w/ Compare Triggers Scrubbing |
| User Logic, I/O's | Distributed TMR | I/O Replication and Error Monitoring | Duplicate with Compare |

*Not supported for Microsemi

# Radiation-Induced Error (SEU) Mitigation

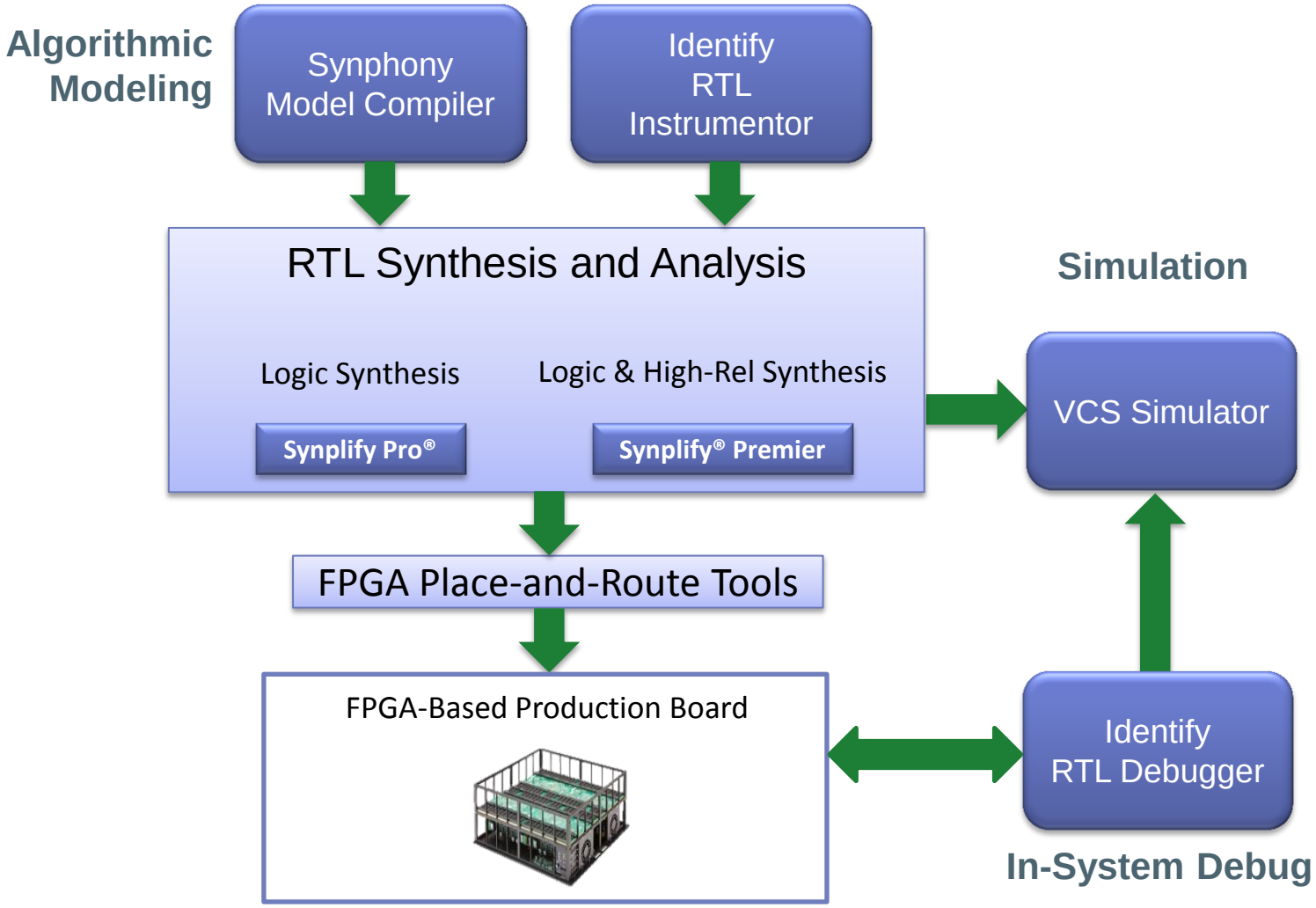
## Susceptibility to Particle Radiation Effects

| Device Type | RAD-HARD | Anti-Fuse/ Flash | SRAM |
|---|---|---|---|
| Register | Low | Moderate | Low |
| Block RAM | Very High unless Error Detection & Correction used | Very High unless Error Detection & Correction used | Very High |
| Logic Cells | None | None | High |
| Routing Matrix | None | None | High |

# Current Solutions

Overview FPGA design tools
Hardware debug and operation visibility
DO-254 support
SEU mitigation circuitry creation and error monitors

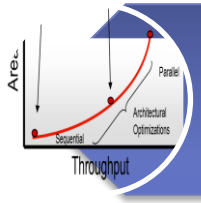
# Synopsys FPGA Design Suite



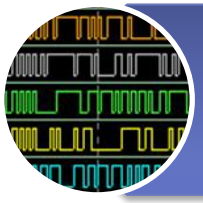
# Synphony Model Compiler Overview

Save Months in Design/Verification of Signal Processing Systems

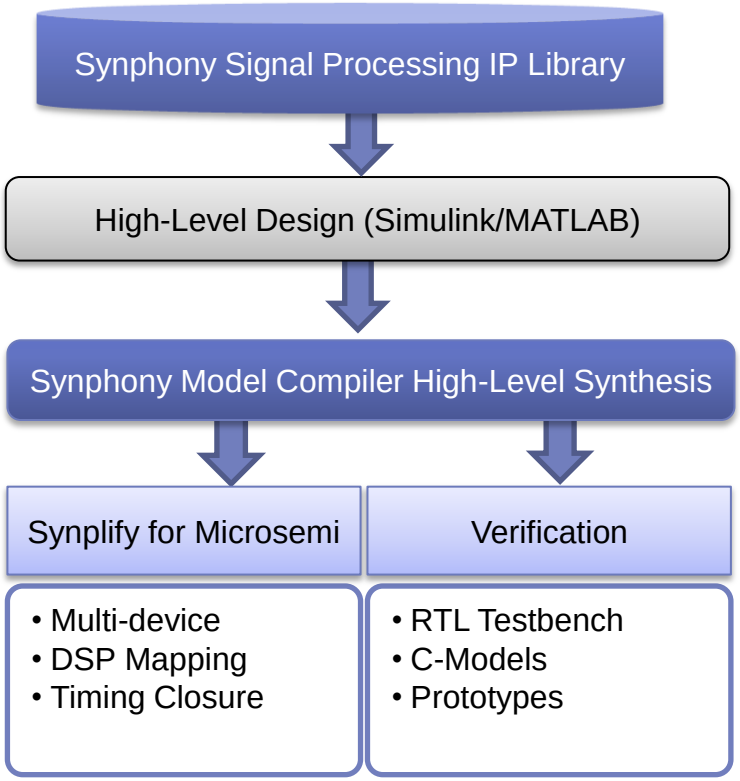
Signal Processing IP library




High-Level Design and Verification from Simulink/MATLAB

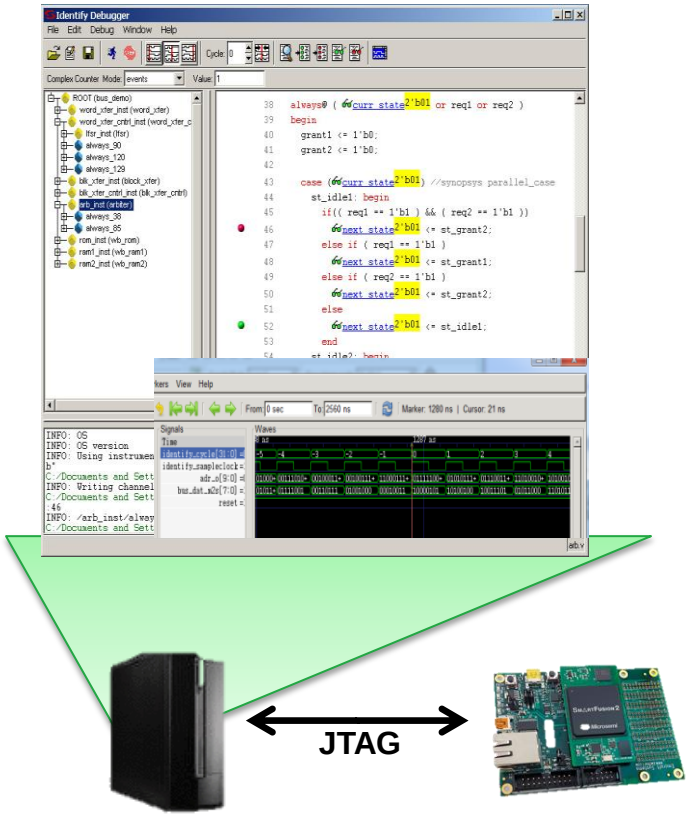


High-performance verification for RTL and C-model system simulation




- Microsemi provides “Synphony Model Compiler” software distribution for Microsemi FPGA devices
- Synopsys enables Synphony Model Compiler product enabling all FPGA devices

# Synplify Debug Provides Simulator-Like Visibility into FPGA Hardware Operation

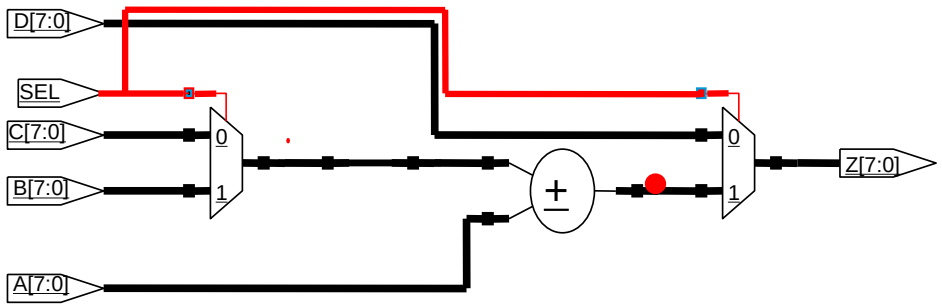



- Faster debug & higher design visibility
  - Traditional debug takes too long
  - Logic analyzers are insufficient
  - Debug at speed in system required
- Debug were you design
  - Instrument/debug directly in RTL
  - Quickly select signals for sampling/triggering
  - Capture signals at real-time speed
  - Powerful triggering for pinpointing a fault
  - Explore state spaces and conditions not easily reached by simulation
  - Integrated with Synplify Premier

- Microsemi provides “Identify” software distribution for Microsemi FPGA devices
- Synopsys enables Synplify Premier and Identify products enabling all FPGA devices

# Identify Enables Requirements Traceability after Synthesis Optimizations

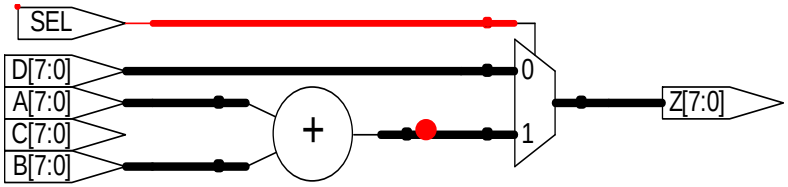
## RTL representation




**Synthesis**

- *RTL Enumerated TYPES appear as 1's and 0's in netlist*
- *RAM, DSP inferencing and sequential optimization optimize node in RED away*

## Optimized Gate Level Netlist




Synthesis performs optimizations

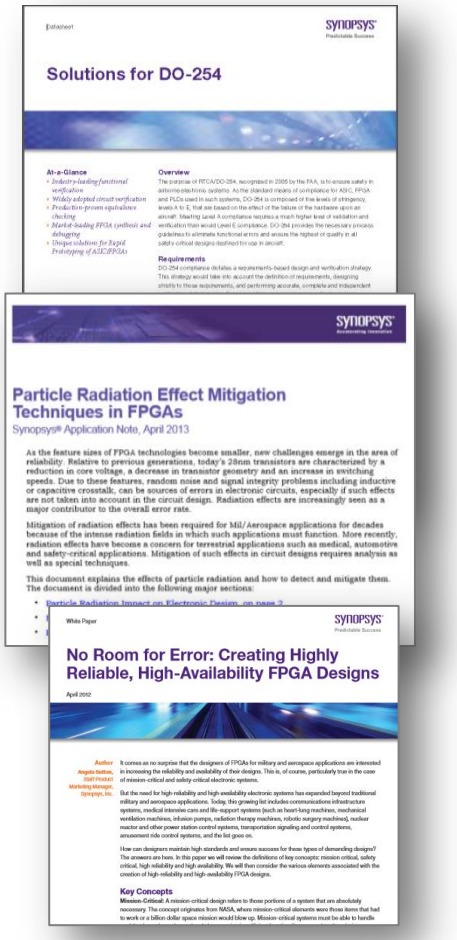
- Can cause debug node being absorbed or transformed
- No longer able to trace or probe these nodes
- Cannot relate their behavior in system back to your RTL

Instrument with Identify

- Nodes of interest preserved
- Relate behavior on board at nodes back to the RTL

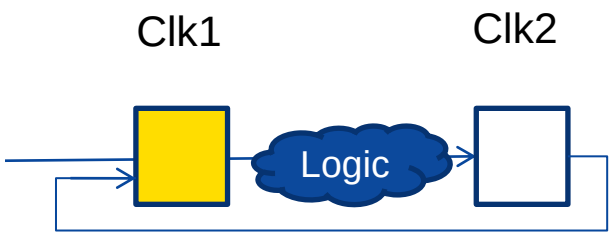
# Synplify Enables DO-254 Compliant Process

| | |
|---|---|
| **Traceability** | Schematics for Documentation<br>Timing Reports and Log files<br>Safe FSM and TMR Reports |
| **Repeatability** | Reproducible synthesis results<br>Lock down pre-verified blocks<br>Best Practices Safety-critical design |
| **Equivalence** | Simulator Integration<br>Node preservation control for equivalence assurance & requirements trace |



# SEU Mitigation Practices – Synplify Pro & Premier

- Clock Domain Synchronization Assurance
  - Report alerts you to meta-stability problems due to design flaws such as failure to synchronize the circuit
- Preservation of Debug Circuitry and of Custom Error Detection and Mitigation Circuitry
  - Implementation during synthesis of RTL “others” clause that specifies your custom error mitigation circuitry
  - Attributes to designate “preserve during synthesis nodes needed for probing and debug, or for equivalence proving purposes”




```
always @ (in1,present_state)
   case (present_state)
      s0 :……..
      s1 : ……..
      s2 : ……
      s3 : …… //no transition into S3
      default : next_state <= s3;
endcase
```

***Attributes***

**syn_keep syn_preserve syn_hier syn_noprune syn_probe**

# Single Event Upset Mitigation Practices

- Antifuse/flash device registers can be moderately susceptible to SEUs
- FSMs contain registers

| Resource | Recommended solution | Synplify Version |
|---|---|---|
| Registers | Local TMR | Synplify Pro |
| FSMs | Hamming-3 Automatic Error Correction<br><br>Specify how to return FSM from “unreachable state” to safe state by specifying and preserving the RTL “others” clause | Synplify Premier |

**TIP:** *Be sure to instruct the synthesis software to preserve error-mitigation circuitry*

# New Best Practices … What's Next?

Local TMR Best Practices
Validating that TMR occurred and that it works
Error monitoring and access
Solutions for MicroSemi RTG4

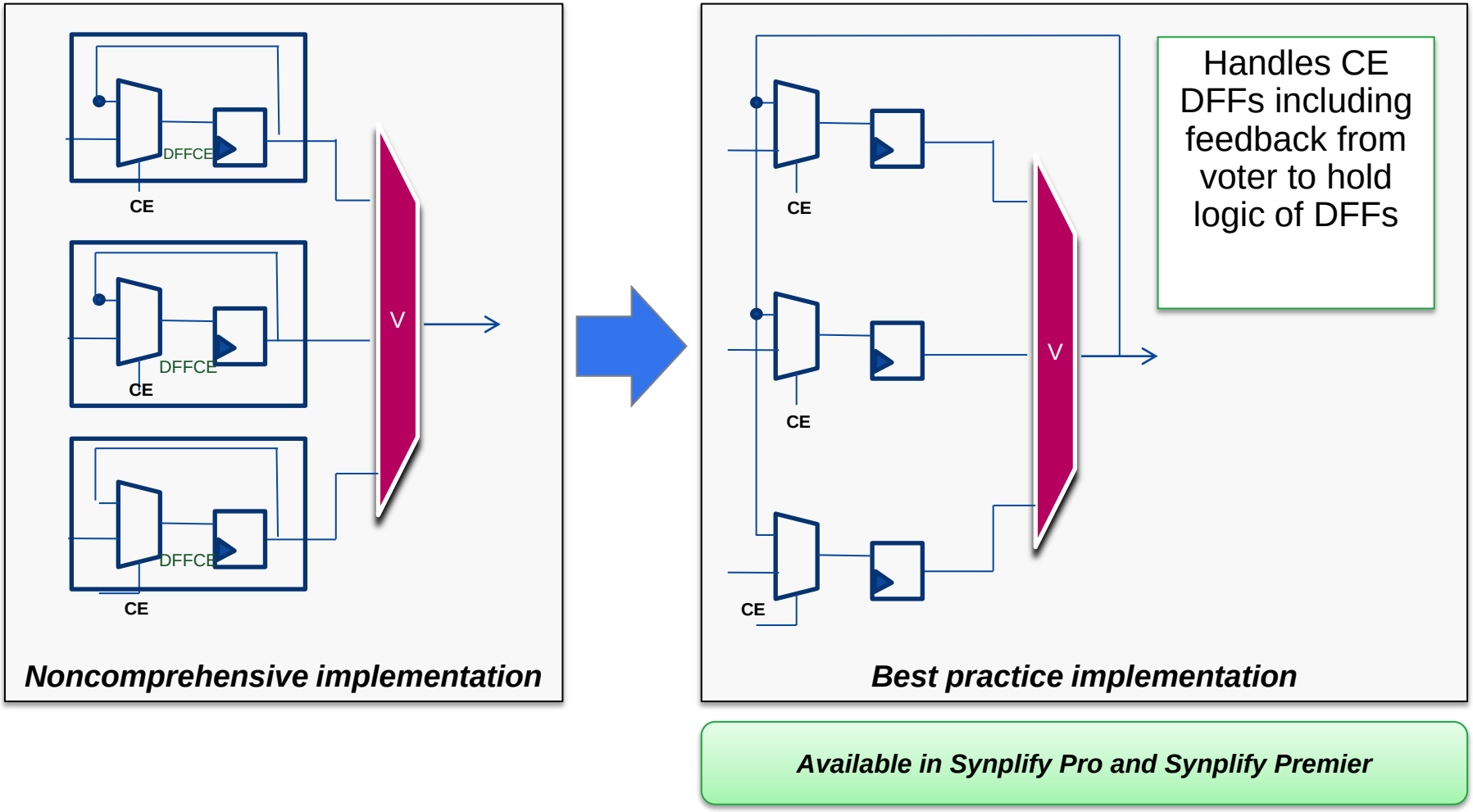
# New Industry Trends and Best Practices

- TMR clock enable feedback loop in Local TMR & Distributed TMR circuitry
- Ways to determine “what best to TMR”
- Validation that TMR occurred
- Physical Separation of Triplicates

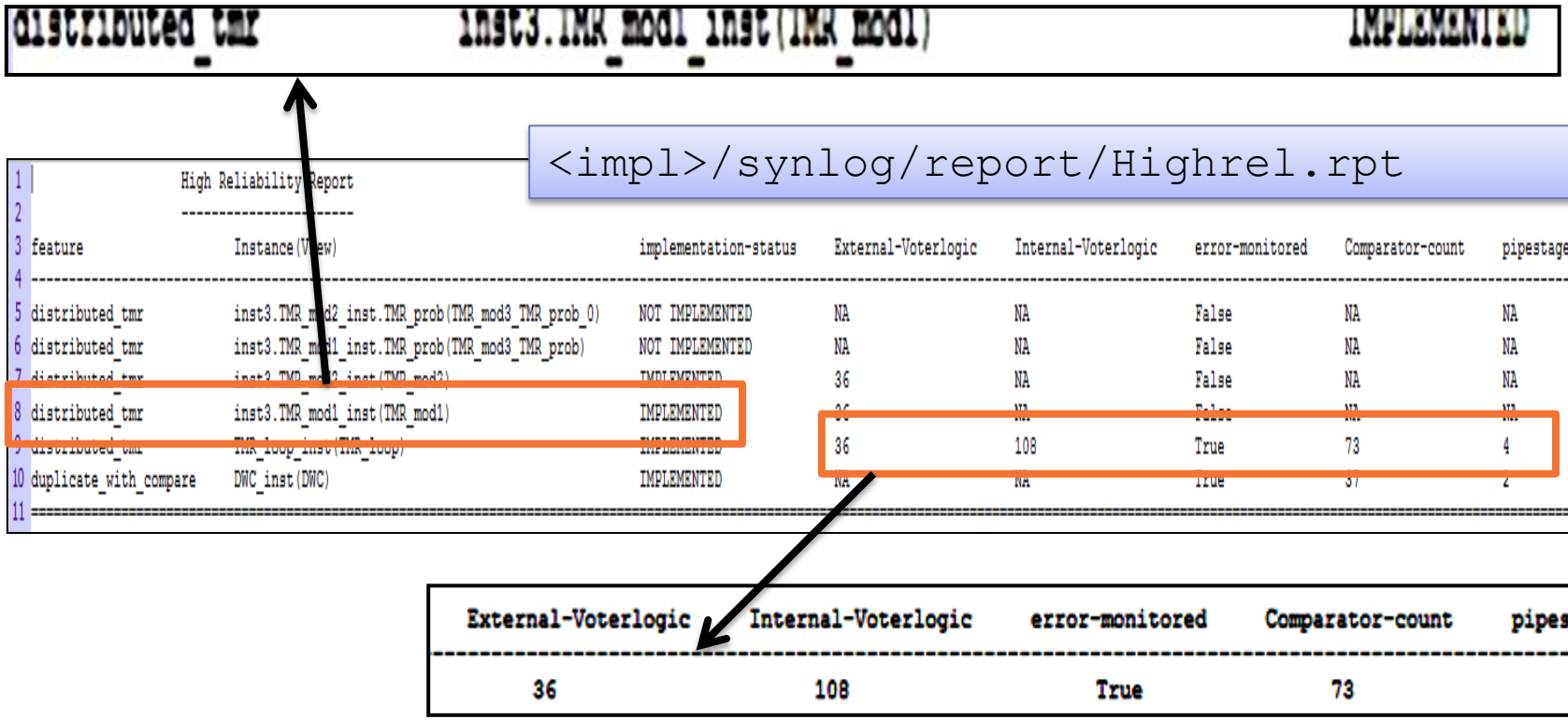
Synopsys is refining these solutions within Synplify Premier

# Local TMR Best Practice

Enhances Local TMR implementation to include feedback from voter



# Validating that TMR Occurred



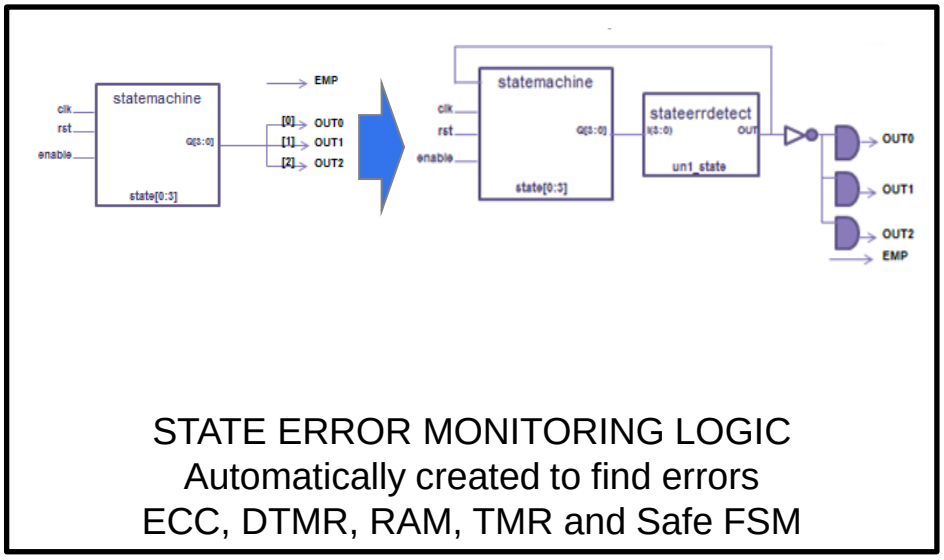

Synplify Premier reports and confirms where SEU mitigation circuitry implemented

- For Local TMR and Distributed TMR, Safe FSM
- Voter logic, sequential loops, error monitoring, comparator gates, pipestage resources

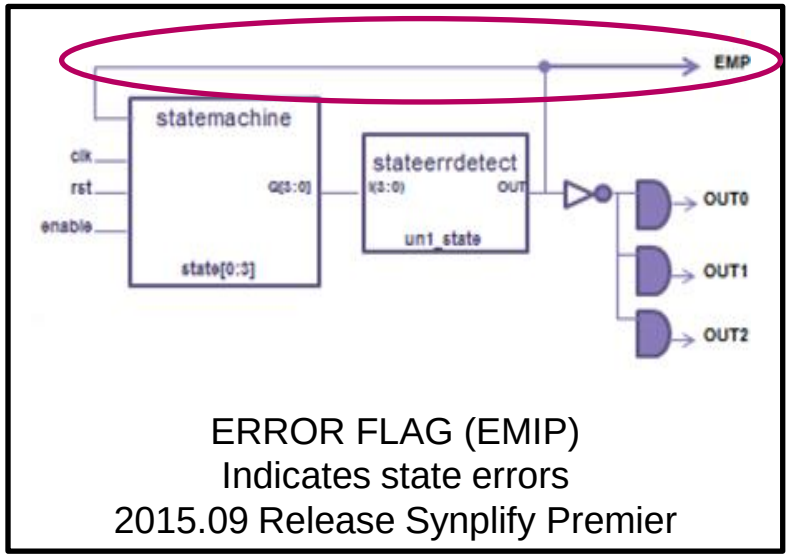
# Error Monitoring & Access – FSM Example

- Synthesis Attributes specify Error Nets to be monitored
- Synthesis creates error-monitoring logic and makes Error flag signal accessible
  - set_option –safe_case 1

```
syn_create_err_net {-name {error_flag} -inst {i:state[1:3]}}
syn_connect -from {{n:error_flag} -to {t:EMIP.err_port}}
```



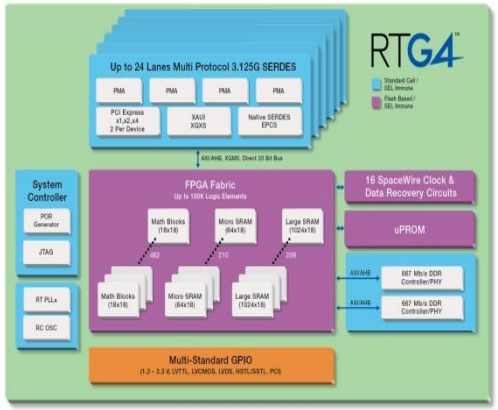

STATE ERROR MONITORING LOGIC
Automatically created to find errors
ECC, DTMR, RAM, TMR and Safe FSM

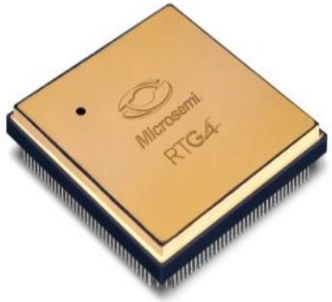



ERROR FLAG (EMIP)
Indicates state errors
2015.09 Release Synplify Premier

# Synplify Premier MicroSemi RTG4 Solution

- Safe FSM
  - syn_encoding = safe
  - Using preserve & decode unreachable states logic
- Sequential logic and FSMs – Hamming 3 error detection and correction (EDAC)
- Support for Block RAMs
  - Inference of ECC block RAMs
  - Access to error bits similar to duplicate and compare.
- Local TMR for registers not required

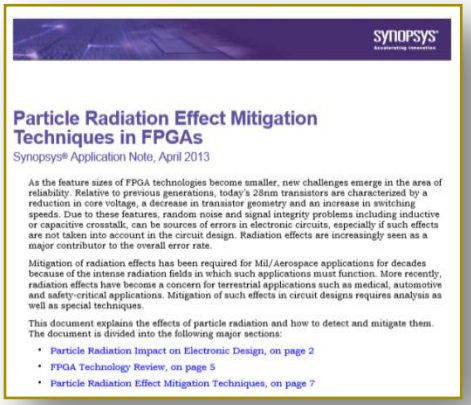



RTG4 design solution available in 2015.09 Synplify Premier release

# More Information on Design for High Reliability

**White Paper**



Particle Radiation Effect Mitigation Techniques in FPGAs

Synopsys® Application Note, April 2013

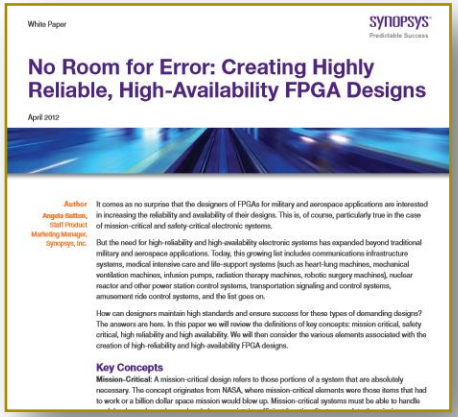
As the feature sizes of FPGA technologies become smaller, new challenges emerge in the area of reliability. Relative to previous generations, today's 28nm transistors are characterized by a reduction in core voltage, a decrease in transistor geometry and an increase in switching speeds. Due to these features, random noise and signal integrity problems including inductive or capacitive crosstalk, can be sources of errors in electronic circuits, especially if such effects are not taken into account in the circuit design. Radiation effects are increasingly seen as a major contributor to the overall error rate.

Mitigation of radiation effects has been required for Mil/Aerospace applications for decades because of the intense radiation fields in which such applications must function. More recently, radiation effects have become a concern for terrestrial applications such as medical, automotive and safety-critical applications. Mitigation of such effects in circuit designs requires analysis as well as special techniques.

This document explains the effects of particle radiation and how to detect and mitigate them. The document is divided into the following major sections:

- Particle Radiation Impact on Electronic Design, on page 2
- FPGA Technology Review, on page 5
- Particle Radiation Effect Mitigation Techniques, on page 7

**App Note**



White Paper

No Room for Error: Creating Highly Reliable, High-Availability FPGA Designs

April 2012

It comes as no surprise that the designers of FPGAs for military and aerospace applications are interested in increasing the reliability and availability of their designs. This is, of course, particularly true in the case of mission-critical and safety-critical electronic systems.

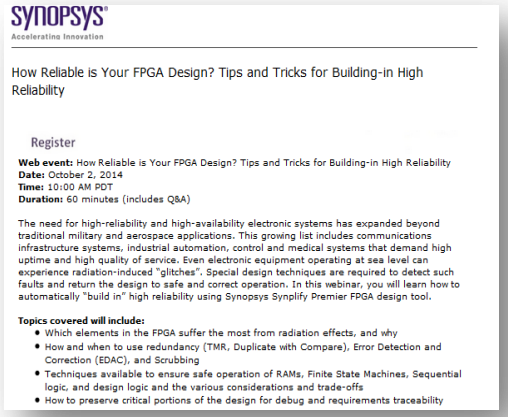
But the need for high-reliability and high-availability electronic systems has expanded beyond traditional military and aerospace applications. Today, this growing list includes communications infrastructure systems, medical intensive care and life-support systems (such as heart-lung machines, mechanical ventilation machines, infusion pumps, radiation therapy machines, robotic surgery machines), nuclear reactor and other power station control systems, transportation signaling and control systems, amusement ride control systems, and the list goes on.

How can designers maintain high standards and ensure success for these types of demanding designs? The answers are here. In this paper we will review the definitions of key concepts: mission critical, safety critical, high reliability and high availability. We will then consider the various elements associated with the creation of high-reliability and high-availability FPGA designs.

Key Concepts

**Mission-Critical:** A mission-critical design refers to those portions of a system that are absolutely necessary. The concept originates from NASA, where mission-critical elements were those items that had to work or a billion dollar space mission would blow up. Mission-critical systems must be able to handle

**High Rel Webinar**



How Reliable is Your FPGA Design? Tips and Tricks for Building-in High Reliability

Register

**Web event:** How Reliable is Your FPGA Design? Tips and Tricks for Building-in High Reliability
**Date:** October 2, 2014
**Time:** 10:00 AM PDT
**Duration:** 60 minutes (includes Q&A)

The need for high-reliability and high-availability electronic systems has expanded beyond traditional military and aerospace applications. This growing list includes communications infrastructure systems, industrial automation, control and medical systems that demand high uptime and high quality of service. Even electronic equipment operating at sea level can experience radiation-induced "glitches". Special design techniques are required to detect such faults and return the design to safe and correct operation. In this webinar, you will learn how to automatically "build in" high reliability using Synopsys Synplify Premier FPGA design tool.

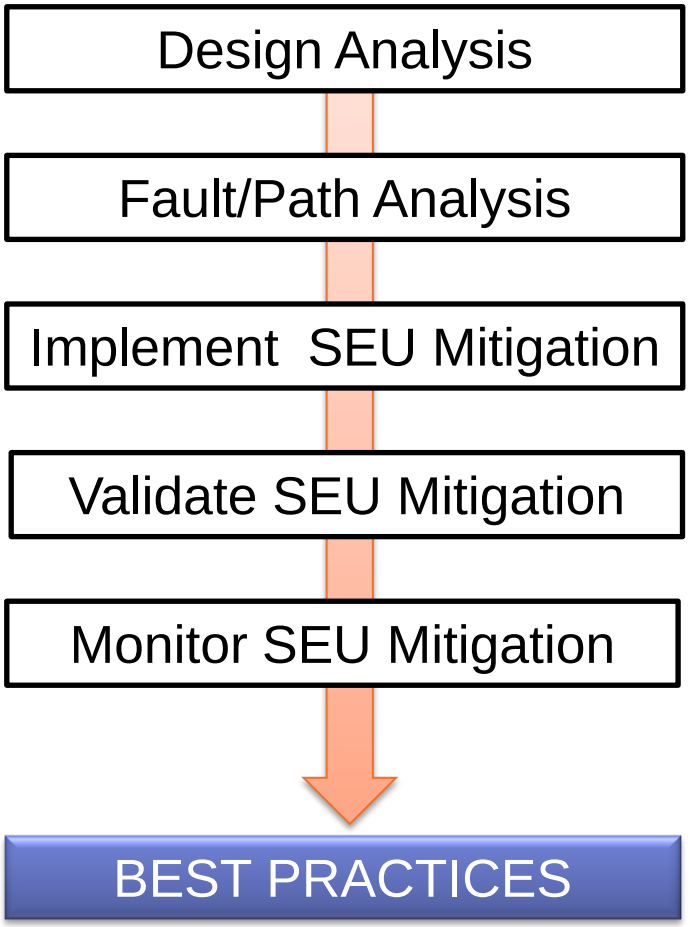
**Topics covered will include:**

- Which elements in the FPGA suffer the most from radiation effects, and why
- How and when to use redundancy (TMR, Duplicate with Compare), Error Detection and Correction (EDAC), and Scrubbing
- Techniques available to ensure safe operation of RAMs, Finite State Machines, Sequential logic, and design logic and the various considerations and trade-offs
- How to preserve critical portions of the design for debug and requirements traceability

*http://www.synopsys.com/fpga*

*And visit us at our booth*

# Synplify Enables SEU Mitigation Methodologies




- Enhanced Local TMR and Distributed TMR for CE DFF
- TMR Reporting Trade-off Analysis and Control
- TMR and Safe FSM reporting and/or visualization
- Fault injection for Safe FSM and TMR (future technology)
- Ease of validation of error recovery
- Error Flag implementation

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# Thank You

Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at www.microsemi.com.

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