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SmartFusion2 and IGLOO2 Neutron Single Event Effects (SEE)

TR0020 Test Report

April 1, 2020

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I. Summary

The SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices—M2S050T, M2S090T, M2S150T—were beam tested for single event effects (SEE) at Los Alamos National Laboratory. Single-event-upset (SEU) and single event latch-up (SEL) measurements were completed at High Temperature of 85°-95° C.

SEL events were not detected with total exposure of more than 1.1 x 10^{12} neutrons/cm^2, which is equivalent to approximately 20,000 years of exposure to atmospheric neutrons at 40,000' over New York City.

SEU measurements were also taken and FIT rates for flip-flops and memory structures were calculated. Flip-flop SEU rates were computed to be between 240 and 360 FIT per million flip-flops, at sea level New York City. SRAM SEU rates were computed to be between 250 and 350 FIT per million bits for LSRAM, and between 160 and 180 FIT per million bits for uSRAM, at sea level New York City.

The results presented here were obtained using SmartFusion2 devices. However, these results are also applicable to the IGLOO®2 FPGA family devices, as IGLOO2 and SmartFusion2 use the same 65 nm Flash process and have common design structures.

II. Neutron Beam Test

A Test Conditions

Los Alamos National Laboratory TA-53 LANSCE facility provided the neutron irradiation. Table 1 shows DUT and test conditions.

Table 1: DUT and Test Conditions

Device	Functional SEU Test	Design	DUT#	Freq (MHz)	Temp (C)	Bias (V)
M2S050	No	SEL Static Non Func	M2S050-896_398	0	85°-95° C	Maximum Spec (VDD = 1.26, VDDI = 2.625 and 3.465, VPP = 3.465)
			M2S050-896_403	0		
			M2S050-896_409	0		
			M2S050-896_410	0		
			M2S050-896_411	0		
			M2S050-896_412	0		
			M2S050-896_413	0		
			M2S050-896_414	0		
			M2S050-896_425	0		
			M2S050-896_426	0		
			M2S050-896_428	0		
			M2S050-896_49	0		
	Yes	200FFx4_uLRAM_TTag	M2S050-896_402	1		
			M2S050-896_404	1		
			M2S050-896_405	1		
			M2S050-896_406	1		
			M2S050-896_427	1		
			M2S050-896_430	1		
M2S090	No	SEL Static Non Func	M2S090-484_133	0		

Device	Functional SEU Test	Design	DUT#	Freq (MHz)	Temp (C)	Bias (V)
			M2S090-484_134	0		
			M2S090-484_135	0		
			M2S090-484_141	0		
			M2S090-484_142	0		
			M2S090-484_143	0		
			M2S090-484_144	0		
			M2S090-484_145	0		
			M2S090-484_146	0		
			M2S090-484_147	0		
			M2S090-484_149	0		
			M2S090-484_150	0		
	Yes	FF_PLL_HS	M2S090-484_136	10		
			M2S090-484_137	120		
			M2S090-484_138	120		
			M2S090-484_139	120		
			M2S090-484_151	10		
			M2S090-484_159	120		
M2S150	No	SEL Static Non Func	M2S150-1152_38	0		
			M2S150-1152_46	0		
			M2S150-1152_51	0		
			M2S150-1152_41	0		
			M2S150-1152_42	0		
	Yes	2000FFx9_uLRAM_TTag	M2S150-1152_43	1		
			M2S150-1152_44	10		
			M2S150-1152_45	10		
			M2S150-1152_47	10		
			M2S150-1152_48	10		
			M2S150-1152_49	10		

Table 2 shows DUT and tested sum of the fluence.

Table 2: Fluence Tested

Device	DUT#	Sum of Fluence
M2S050	M2S050-896_398	4.35E+10
	M2S050-896_402	2.97E+10
	M2S050-896_403	2.29E+10
	M2S050-896_404	2.41E+10
	M2S050-896_405	3.23E+10
	M2S050-896_406	2.35E+10
	M2S050-896_409	2.81E+10
	M2S050-896_410	2.80E+10
	M2S050-896_411	2.28E+10
	M2S050-896_412	3.07E+10
	M2S050-896_413	3.05E+10
	M2S050-896_414	4.37E+10
	M2S050-896_425	1.29E+10
	M2S050-896_426	1.28E+10
	M2S050-896_427	1.36E+10
	M2S050-896_428	1.37E+10
	M2S050-896_430	1.44E+10
	M2S050-896_49	1.36E+10
M2S050 Total		4.41E+11
M2S090	M2S090-484_133	2.85E+10
	M2S090-484_134	2.83E+10
	M2S090-484_135	2.32E+10
	M2S090-484_136	2.95E+10
	M2S090-484_137	2.39E+10
	M2S090-484_138	3.21E+10
	M2S090-484_139	2.34E+10
	M2S090-484_141	2.31E+10
	M2S090-484_142	3.11E+10
	M2S090-484_143	3.09E+10
	M2S090-484_144	4.43E+10
	M2S090-484_145	4.40E+10
	M2S090-484_146	1.31E+10
	M2S090-484_147	1.30E+10
	M2S090-484_149	1.38E+10
	M2S090-484_150	1.39E+10
	M2S090-484_151	1.43E+10

Device	DUT#	Sum of Fluence
	M2S090-484_159	1.35E+10
M2S090 Total		4.44E+11
M2S150	M2S150-1152_38	4.32E+10
	M2S150-1152_41	2.78E+10
	M2S150-1152_42	2.26E+10
	M2S150-1152_43	2.92E+10
	M2S150-1152_44	2.38E+10
	M2S150-1152_45	3.19E+10
	M2S150-1152_46	3.03E+10
	M2S150-1152_47	1.12E+10
	M2S150-1152_48	1.34E+10
	M2S150-1152_49	1.42E+10
	M2S150-1152_51	2.63E+10
M2S150 Total		2.74E+11
Grand Total		1.16E+12

B Test Procedure

SEL Testing Procedure

SEL and SEU tests were conducted simultaneously on several DUTs marked as **Functional SEU Test** in Table 1. To collect further SEL statistics, several DUTs in beam are biased and monitored for power fluctuations. However, no SEU statistics were collected from DUTs marked as **SEL Static Non Func** design in Table 1.

The power supplies were monitored and observed for current jumps. For a current jump of <20 mA, current was measured again after approximately one minute to see if the current returned to normal levels. If the current did not drop down, or if the current jump is >20 mA, the voltage was ramped downwards below the holding voltage and then back up again to determine if the jump was due to SEL or contention.

Figure 1 shows SEL test procedure in detail.

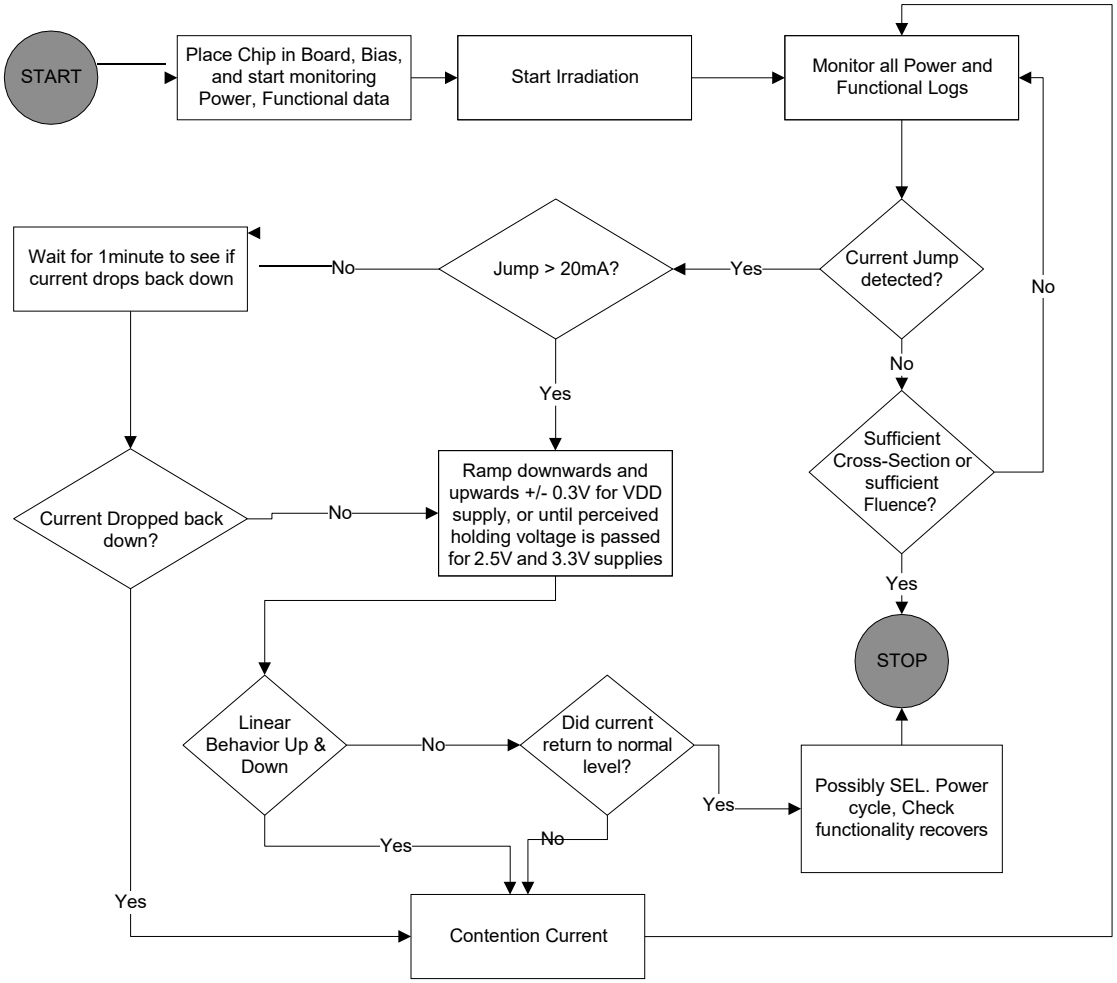

Figure 1: SEL Testing Procedure

SEU Procedure

Flip-Flop and Globals

The Master Controller compares the output flip-flop data with the expected golden model cycle for cycle to ensure that every flip-flop error is captured. Burst errors, such as a phase shift can be caught to help identify global upsets. The design was manually placed to identify burst signatures for Global upsets including row global buffers (RGB), global buffers (GB), and logic cluster (CL) upsets. Figure 2 shows how a cycle for cycle comparison between the DUT and Global model. Similarly, other blocks also follow the same approach.

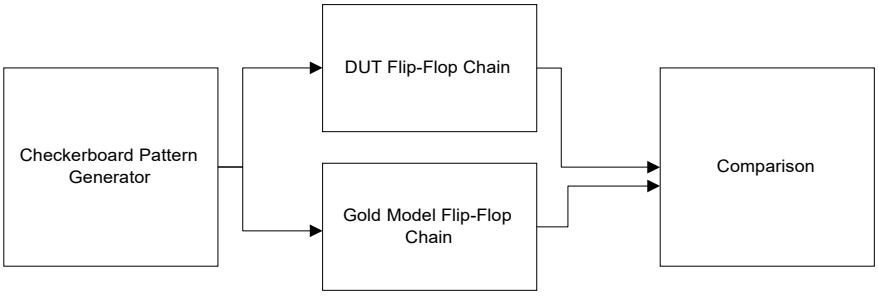

Figure 2: Golden Model vs. DUT Data Capture

uSRAM/LSRAM

The LSRAM and uSRAM blocks are configured with 18-bit words (LSRAM = 18 x 1024 address x 69 blocks; uSRAM = 18 x 64 address x 72 blocks) and read one 18-bit word at a time. All Addresses in each RAM block and every block on the chip are read sequentially. If any upset is detected, the cycles are tracked to find in which cycle the error occurred. The error sequence is reconstructed to determine if any upsets occurred in the same block (or word) in the same read cycle.

Observations:

- All upsets are Time-Tagged with the time each error occurred
- Keep track of the location of each upset (Address, Block, Ram Type)
- Keep track of the cycles, if upsets occur in the same read cycle
- Write back and clear errors after the entire RAM is read completely

PLL

The M2S090 DUT design incorporates one Fabric PLL in the testing design. The PLL clock source is the same oscillator as the controller design for synchronization purposes. The output of the PLL is connected to a clock network on the M2S090 FPGA. The clock network drives several chains of flip-flops.

Observations:

1. Monitored the PLL lock signal to identify if the PLL goes out of lock
2. Monitored the flip-flops to help identify if the PLL output stopped functioning even if the lock signal is not lost. This will appear as a burst error and help to identify the number of cycles for recovery.

III. DUT Design

A Test Device

The test devices contain the following:

- Flip-flops
  - M2S050T-FGG896 – Four Chains of 2000 flip-flops per chain (Manually placed, 400 flip-flops per RGB)
  - M2S090T-FGG484 – Seven Chains of 200 flip-flops per chain (Manually placed, 200 flip-flops per RGB)
  - M2S150T-FGG1152 – Nine Chains of 2000 flip-flops per chain (Manually placed, 400 flip-flops per RGB)
- LSRAM
  - M2S050-FGG896 –69 LSRAM blocks instantiated (18-bit word size x 1024 address)
  - M2S150-FGG1152 –69 LSRAM blocks instantiated (18-bit word size x 1024 address)
- uSRAM
  - M2S050-FGG896 –72 uSRAM blocks instantiated (18-bit word size x 64 address)
  - M2S150-FGG1152 – 72 uSRAM blocks instantiated (18-bit word size x 64 address)
- PLL
  - M2S090T-FGG484 – PLL configured as 9 MHz input, 10 MHz, and 120 MHz output driving internal global clock. The PLL lock signal is monitored.

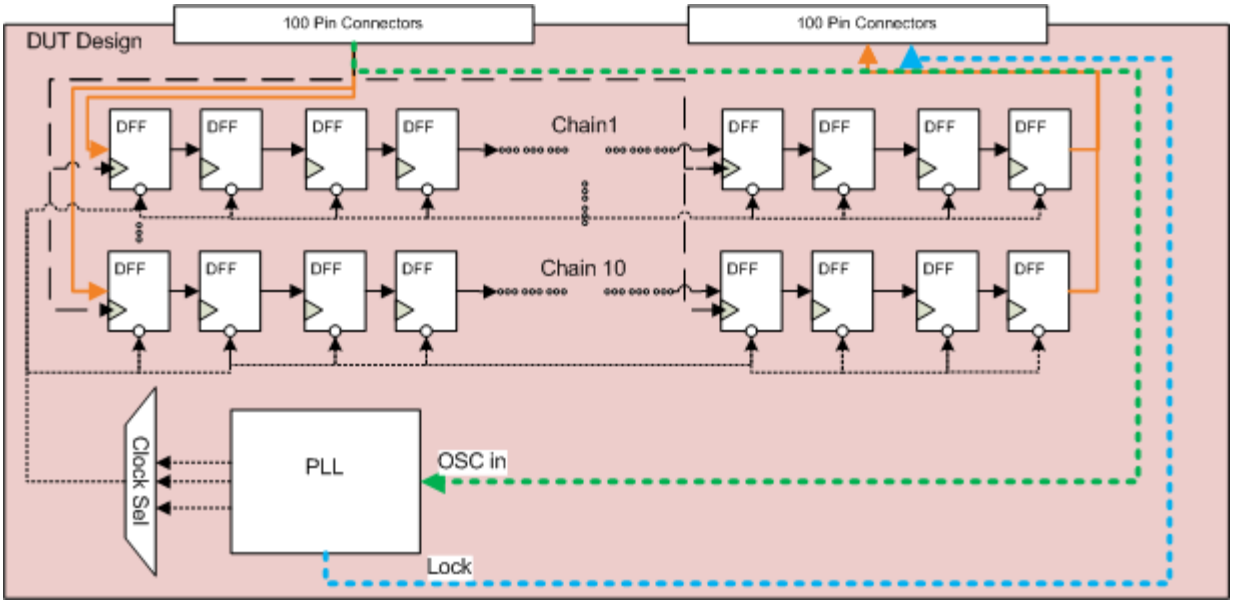

Figure 3: Block Diagram of M2S090 Test Design

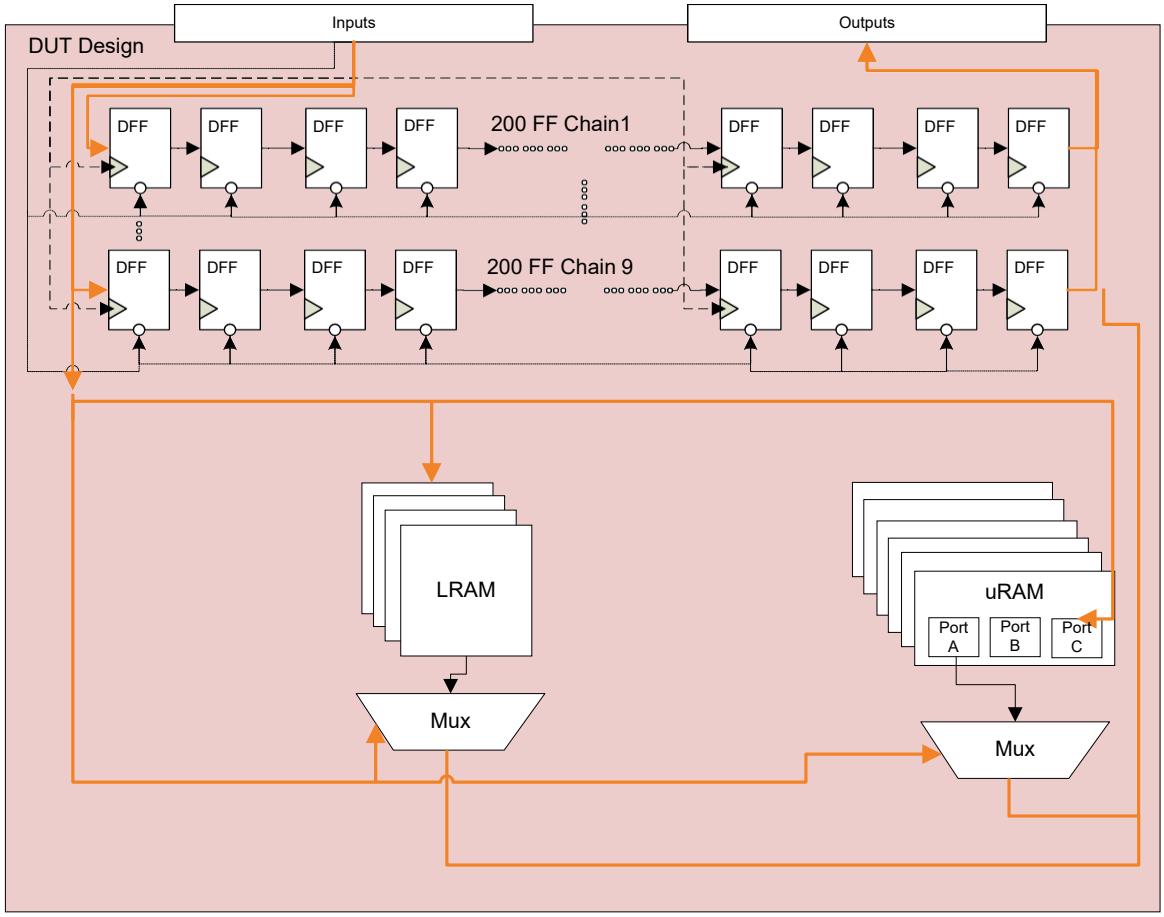

Figure 4: Block Diagram of M2S050 and M2S150 Test Designs

B Setup

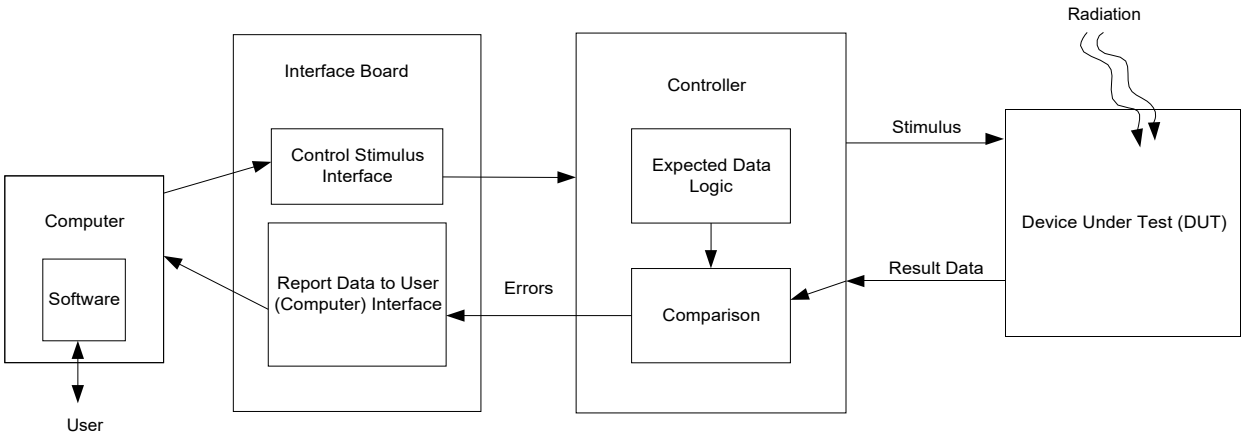

Figure 5: High-Level Setup for Controller and DUT

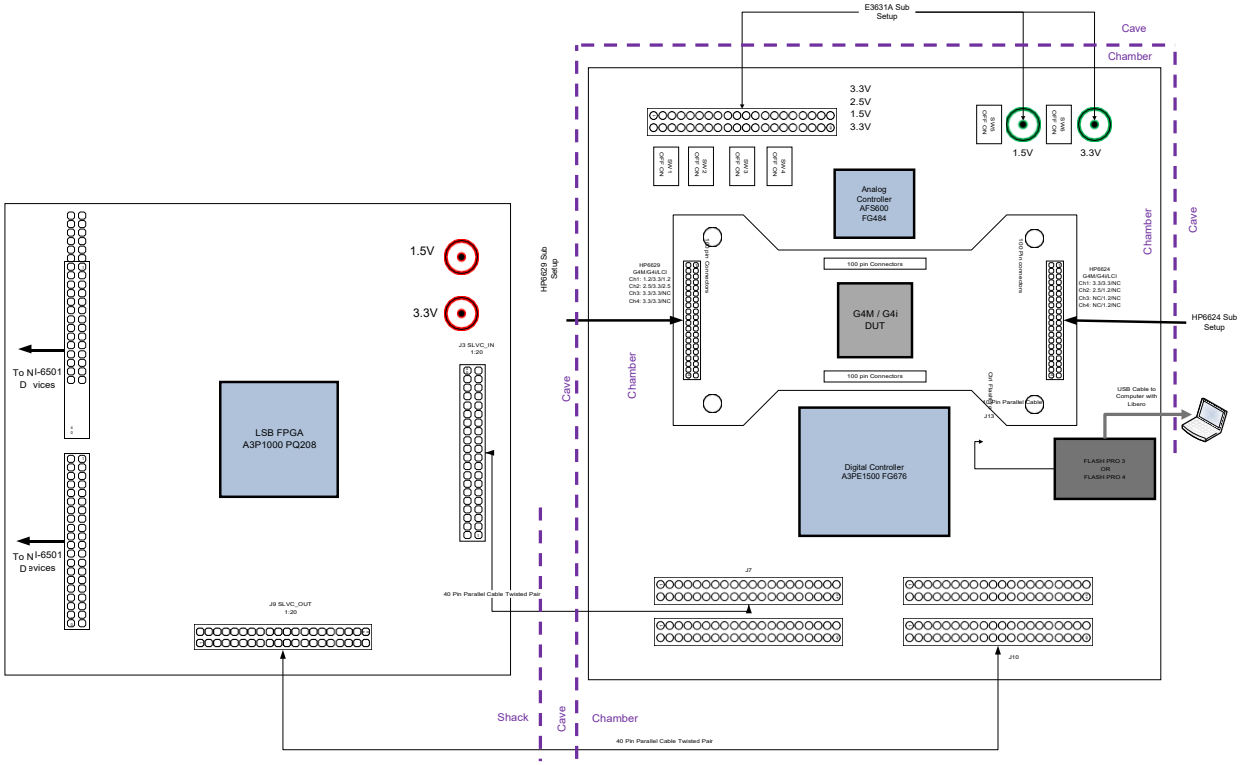

Figure 6: Boards Setup

IV. Test Results

Table 3 through Table 15 shows the test results.

Table 3: Test Results – Run 1

DUT#	M2S050-896_402	M2S090-484_136	M2S150-1152_43	M2S090-484_133	M2S090-484_134	M2S050-896_409	M2S050-896_410	M2S150-1152_41
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	IOCheck
Fluence	2.02E+10	2.00E+10	1.98E+10	1.94E+10	1.92E+10	1.91E+10	1.90E+10	1.89E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	617		#N/A					
LSRAM BIT	617		#N/A					
LSRAM MBU	0		#N/A					
uSRAM WRD	24		#N/A					
uSRAM BIT	24		#N/A					
uSRAM MBU	0		#N/A					
FF1'	1	0	0					
FF2'	1	0	0					
FF3'	0	0	3					
FF4'	0	0	0					
FF5'		0	1					
FF6'		0	1					
FF7'		0	2					
FF8'			1					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			1					
Cluster9			0					

Table 12: Test Results – Run 8

DUT#	M2S050-896_402	M2S090-484_136	M2S150-1152_43	M2S090-484_133	M2S090-484_134	M2S050-896_409	M2S050-896_410	M2S150-1152_41
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	IOCheck
Fluence	9.50E+09	9.43E+09	9.37E+09	9.14E+09	9.08E+09	9.02E+09	8.97E+09	8.91E+09
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	304		#N/A					
LSRAM BIT	304		#N/A					
LSRAM MBU	0		#N/A					
uSRAM WRD	8		#N/A					
uSRAM BIT	8		#N/A					
uSRAM MBU	0		#N/A					
FF1'	0	0	0					
FF2'	1	0	0					
FF3'	0	0	0					
FF4'	2	0	0					
FF5'		0	0					
FF6'		0	1					
FF7'		0	0					
FF8'			2					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 13: Test Results – Run 9

DUT#	M2S050-896_404	M2S090-484_137	M2S150-1152_44	M2S090-484_135	M2S090-484_141	M2S050-896_403	M2S050-896_411	M2S150-1152_42
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	IOCheck
Fluence	2.92E+09	2.90E+09	2.88E+09	2.81E+09	2.79E+09	2.78E+09	2.76E+09	2.74E+09
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	0		#N/A					
LSRAM BIT	0		#N/A					
LSRAM MBU	0		#N/A					
uSRAM WRD	0		#N/A					
uSRAM BIT	0		#N/A					
uSRAM MBU	0		#N/A					
FF1'	0	0	0					
FF2'	0	0	0					
FF3'	0	0	0					
FF4'	0	0	0					
FF5'		0	0					
FF6'		0	0					
FF7'		0	0					
FF8'			0					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 14: Test Results – Run 8

DUT#	M2S050-896_404	M2S090-484_137	M2S150-1152_44	M2S090-484_135	M2S090-484_141	M2S050-896_403	M2S050-896_411	M2S150-1152_42
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	IOCheck
Fluence	2.41E+10	2.39E+10	2.38E+10	2.32E+10	2.31E+10	2.29E+10	2.28E+10	2.26E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	826		559					
LSRAM BIT	826		559					
LSRAM MBU	0		0					
uSRAM WRD	29		42					
uSRAM BIT	29		42					
uSRAM MBU	0		0					
FF1'	1	0	0					
FF2'	1	0	1					
FF3'	1	0	1					
FF4'	0	2	2					
FF5'		0	0					
FF6'		0	9					
FF7'		1	0					
FF8'			1					
FF9'			1					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 15: Test Results – Run 9

DUT#	M2S050-896_405	M2S090-484_138	M2S150-1152_45	M2S090-484_142	M2S090-484_143	M2S050-896_412	M2S050-896_413	M2S150-1152_46
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	1.63E+10	1.62E+10	1.61E+10	1.57E+10	1.56E+10	1.55E+10	1.54E+10	1.53E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		1						
LSRAM WRD	555		356					
LSRAM BIT	555		356					
LSRAM MBU	0		0					
uSRAM WRD	23		11					
uSRAM BIT	23		11					
uSRAM MBU	0		0					
FF1'	1	0	0					
FF2'	1	0	0					
FF3'	2	0	1					
FF4'	1	0	0	SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
FF5'		0	0					
FF6'		0	0					
FF7'		0	1					
FF8'			2					
FF9'			1					
Cluster1	0	0	0					
Cluster2	1	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 16: Test Results – Run 8

DUT#	M2S050-896_405	M2S090-484_138	M2S150-1152_45	M2S090-484_142	M2S090-484_143	M2S050-896_412	M2S050-896_413	M2S150-1152_46
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	1.60E+10	1.59E+10	1.58E+10	1.54E+10	1.53E+10	1.52E+10	1.51E+10	1.50E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	523		389					
LSRAM BIT	523		389					
LSRAM MBU	0		0					
uSRAM WRD	15		14					
uSRAM BIT	15		14					
uSRAM MBU	0		0					
FF1'	0	0	0					
FF2'	1	1	0					
FF3'	0	0	0					
FF4'	2	0	1					
FF5'		0	2					
FF6'		0	1					
FF7'		0	0					
FF8'			2					
FF9'			1					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 17: Test Results – Run 9

DUT#	M2S050-896_406	M2S090-484_139	M2S150-1152_47	M2S090-484_144	M2S090-484_145	M2S050-896_414	M2S050-896_398	M2S150-1152_38
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0						
LSRAM WRD	0		0					
LSRAM BIT	0		0					
LSRAM MBU	0		0					
uSRAM WRD	0		0					
uSRAM BIT	0		0					
uSRAM MBU	0		0					
FF1'	0	0	0					
FF2'	0	0	0					
FF3'	0	0	0					
FF4'	0	0	0	SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
FF5'		0	0					
FF6'		0	0					
FF7'		0	0					
FF8'			0					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 18: Test Results – Run 8

DUT#	M2S050-896_406	M2S090-484_139	M2S150-1152_47	M2S090-484_144	M2S090-484_145	M2S050-896_414	M2S050-896_398	M2S150-1152_38
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	1.22E+10	1.21E+10	1.20E+10	1.17E+10	1.17E+10	1.16E+10	1.15E+10	1.14E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	394		N/A					
LSRAM BIT	394		N/A					
LSRAM MBU	0		N/A					
uSRAM WRD	16		N/A					
uSRAM BIT	16		N/A					
uSRAM MBU	0		N/A					
FF1'	0	0	N/A					
FF2'	0	0	N/A					
FF3'	0	0	N/A					
FF4'	0	0	N/A					
FF5'		0	N/A					
FF6'		0	N/A					
FF7'		0	N/A					
FF8'			N/A					
FF9'			N/A					
Cluster1	0	0	N/A					
Cluster2	0	0	N/A					
Cluster3	0	0	N/A					
Cluster4	0	0	N/A					
Cluster5		0	N/A					
Cluster6		0	N/A					
Cluster7		0	N/A					
Cluster8			N/A					
Cluster9			N/A					

Table 19: Test Results – Run 9

DUT#	M2S050-896_406	M2S090-484_139	M2S150-1152_47	M2S090-484_144	M2S090-484_145	M2S050-896_414	M2S050-896_398	M2S150-1152_38
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	2.25E+10	2.24E+10	2.22E+10	2.17E+10	2.15E+10	2.14E+10	2.13E+10	2.11E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0						
LSRAM WRD	703		583					
LSRAM BIT	0		583					
LSRAM MBU	0		0					
uSRAM WRD	22		21					
uSRAM BIT	22		21					
uSRAM MBU	0		0					
FF1'	2	0	0					
FF2'	0	0	0					
FF3'	0	0	1					
FF4'	0	0	2	SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
FF5'		0	0					
FF6'		0	0					
FF7'		0	1					
FF8'			0					
FF9'			2					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 20: Test Results – Run 8

DUT#	M2S050-896_406	M2S090-484_139	M2S150-1152_47	M2S090-484_144	M2S090-484_145	M2S050-896_414	M2S050-896_398	M2S150-1152_38
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	1.13E+10	1.13E+10	1.12E+10	1.09E+10	1.08E+10	1.08E+10	1.07E+10	1.06E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	338		249					
LSRAM BIT	338		249					
LSRAM MBU	0		0					
uSRAM WRD	10		6					
uSRAM BIT	10		6					
uSRAM MBU	0		0					
FF1'	0	0	1					
FF2'	1	0	0					
FF3'	0	0	1					
FF4'	0	0	0					
FF5'		0	1					
FF6'		0	1					
FF7'		0	0					
FF8'			0					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	1					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 21: Test Results – Run 9

DUT#	M2S050-896_427	M2S090-484_159	M2S150-1152_48	M2S090-484_146	M2S090-484_147	M2S050-896_425	M2S050-896_426	M2S150-1152_51
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	1.36E+10	1.35E+10	1.34E+10	1.31E+10	1.30E+10	1.29E+10	1.28E+10	1.27E+10
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0						
LSRAM WRD	433		319					
LSRAM BIT	433		319					
LSRAM MBU	0		0					
uSRAM WRD	13		14					
uSRAM BIT	13		14					
uSRAM MBU	0		0					
FF1'	0	0	0					
FF2'	0	0	2					
FF3'	1	0	0					
FF4'	1	0	0	SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
FF5'		0	0					
FF6'		0	0					
FF7'		0	0					
FF8'			0					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			1					
Cluster9			0					

Table 22: Test Results – Run 8

DUT#	M2S050-896_430	M2S090-484_151	M2S150-1152_49	M2S090-484_150	M2S090-484_149	M2S050-896_428	M2S050-896_49	M2S150-1152_51
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	5.45E+09	5.41E+09	5.37E+09	5.25E+09	5.21E+09	5.18E+09	5.15E+09	5.11E+09
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	163		119					
LSRAM BIT	163		119					
LSRAM MBU	0		0					
uSRAM WRD	3		3					
uSRAM BIT	3		3					
uSRAM MBU	0		0					
FF1'	0	0	0					
FF2'	0	0	0					
FF3'	0	0	0					
FF4'	0	0	1					
FF5'		1	0					
FF6'		0	0					
FF7'		0	1					
FF8'			0					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

Table 23: Test Results – Run 9

DUT#	M2S050-896_430	M2S090-484_151	M2S150-1152_49	M2S090-484_150	M2S090-484_149	M2S050-896_428	M2S050-896_49	M2S150-1152_51
Design	200FFx4_uLRAM_TTag	FF_PLL_HS	2000FFx9_uLRAM_TTag	BufChain	BufChain	BufChain	BufChain	BufChain
Fluence	8.98E+09	8.92E+09	8.86E+09	8.65E+09	8.59E+09	8.53E+09	8.48E+09	8.42E+09
SEL	0	0	0	0	0	0	0	0
PLL LOCK		0		SEL Only	SEL Only	SEL Only	SEL Only	SEL Only
LSRAM WRD	268		221					
LSRAM BIT	268		221					
LSRAM MBU	0		0					
uSRAM WRD	9		5					
uSRAM BIT	9		5					
uSRAM MBU	0		0					
FF1'	0	0	0					
FF2'	0	0	0					
FF3'	1	0	0					
FF4'	0	0	0					
FF5'		0	0					
FF6'		0	1					
FF7'		0	1					
FF8'			1					
FF9'			0					
Cluster1	0	0	0					
Cluster2	0	0	0					
Cluster3	0	0	0					
Cluster4	0	0	0					
Cluster5		0	0					
Cluster6		0	0					
Cluster7		0	0					
Cluster8			0					
Cluster9			0					

V. Test Results Summary

A SEL Cross Section and FIT

There are no SEL occurrences for all fluences as shown in Table 17. The DUTs were biased at the maximum specification voltages and heated to a temperature of approximately 85° to 95° C.

Table 16: SEL Summary

Device	Sum of SEL	Sum of Fluence	Cross Section (σ)	FIT
M2S050	0	4.41E+11	None Detected	None Detected
M2S090	0	4.44E+11	None Detected	None Detected
M2S150	0	2.74E+11	None Detected	None Detected

Table 17: SEL Occurrences by DUT

Device	DUT#	Sum of Fluence	Number of SELs Observed
	M2S050-896_398	4.35E+10	0
	M2S050-896_402	2.97E+10	0
	M2S050-896_403	2.29E+10	0
	M2S050-896_404	2.41E+10	0
	M2S050-896_405	3.23E+10	0
	M2S050-896_406	2.35E+10	0
	M2S050-896_409	2.81E+10	0
	M2S050-896_410	2.80E+10	0
	M2S050-896_411	2.28E+10	0
	M2S050-896_412	3.07E+10	0
	M2S050-896_413	3.05E+10	0
	M2S050-896_414	4.37E+10	0
	M2S050-896_425	1.29E+10	0
	M2S050-896_426	1.28E+10	0
	M2S050-896_427	1.36E+10	0
	M2S050-896_428	1.37E+10	0
	M2S050-896_430	1.44E+10	0
M2S050	M2S050-896_49	1.36E+10	0
M2S050 Total			
	M2S090-484_133	2.85E+10	0
	M2S090-484_134	2.83E+10	0
	M2S090-484_135	2.32E+10	0
	M2S090-484_136	2.95E+10	0
	M2S090-484_137	2.39E+10	0
	M2S090-484_138	3.21E+10	0
	M2S090-484_139	2.34E+10	0
	M2S090-484_141	2.31E+10	0
M2S090	M2S090-484_142	3.11E+10	0

Device	DUT#	Sum of Fluence	Number of SELs Observed
	M2S090-484_143	3.09E+10	0
	M2S090-484_144	4.43E+10	0
	M2S090-484_145	4.40E+10	0
	M2S090-484_146	1.31E+10	0
	M2S090-484_147	1.30E+10	0
	M2S090-484_149	1.38E+10	0
	M2S090-484_150	1.39E+10	0
	M2S090-484_151	1.43E+10	0
	M2S090-484_159	1.35E+10	0
M2S090 Total			
	M2S150-1152_38	4.32E+10	0
	M2S150-1152_41	2.78E+10	0
	M2S150-1152_42	2.26E+10	0
	M2S150-1152_43	2.92E+10	0
	M2S150-1152_44	2.38E+10	0
	M2S150-1152_45	3.19E+10	0
	M2S150-1152_46	3.03E+10	0
	M2S150-1152_47	1.12E+10	0
	M2S150-1152_48	1.34E+10	0
	M2S150-1152_49	1.42E+10	0
M2S150	M2S150-1152_51	2.63E+10	0
M2S150 Total			
Grand Total		**1.16E+12**	**0**

B SEU Errors, Cross Section, FIT

Table 18: SEU FIT Rate

Formulas	*σ (PerBit) = (∑ RunUpsets(i)/NumBits (i)) / ∑ Fluence(i) ; where i is the run number.* *σ(Mb) = σ(PerBit) * 2 [20] bits* *FIT = σ(Mb) * f(NYC) * 10^9 (errors / 10^9 hour) ; where f(NYC) = 13 n /cm^2 / hour*

	Device	Errors	Number of Elements	Fluence	o Per Element	σ/Million Elements	FIT [NYC]
Flip-Flop	M2S050	20	2000×4 Chains	1.38×10^{11}	1.82×10^{-14}	1.91×10^{-8}	248 Mb
	M2S090	5	200×7 Chains	1.37×10^{11}	2.61×10^{-14}	2.74×10^{-8}	356 Mb
	M2S150	49	2000×9 Chains	1.24×10^{11}	2.20×10^{-14}	2.31×10^{-8}	300 Mb
Logic Cluster	M2S050	1	166	1.38×10^{11}	1.09×10^{-14}	1.15×10^{-8}	149 Mb
	M2S090	0	16	1.37×10^{11}	-	-	-
	M2S150	3	166	1.24×10^{11}	1.62×10^{-14}	1.70×10^{-8}	221 Mb
LSRAM Bit	M2S050	4421	1271808	1.38×10^{11}	2.53×10^{-14}	2.65×10^{-8}	344 Mb
	M2S090	-	-	-	-	-	-
	M2S150	2212	1271808	9.44×10^{10}	1.84×10^{-14}	1.93×10^{-8}	251 Mb
uSRAM Bit	M2S050	150	82944	$1.38E\times10^{11}$	1.31×10^{-14}	1.38×10^{-8}	179 Mb
	M2S090	-	-	-	-	-	-
	M2S150	95	82944	9.44×10^{10}	1.21×10^{-14}	1.27×10^{-8}	165 Mb
PLL Lock	M2S090	1	1	1.37×10^{11}	7.32×10^{-12}	N/A*	0.1 PLL
PLL Output	M2S090	0	1	1.37×10^{11}	$<7.32\times10^{-12}$	N/A*	<0.1 PLL

Note: All devices were tested in avionics mode (system controller was disabled)

*Per PLL

C Discussion

SEL

There are no SEL occurrences. The power supplies used included the HP6624/HP6629/Agillent N6700 (with high precision modules) all capable of detecting current jumps smaller than the mA range.

SEU

1. Flip-flop
   - The flip-flop FIT rate is between 248-356 per million flip-flops at NYC, which is consistent with experiment.
2. Globals (GB, RGB, and Logic Cluster)
   - The logic cluster upset rate is between 149-221 FIT per million (2^{20}) clusters at NYC Sea Level.
   - No upsets are detected on RGB or GB.
3. uSRAM/LSRAM
   - LSRAM fit rate is between 251-344 FIT and uSRAM FIT rate is between 165-179 FIT per million (2^{20}) bits at NYC Sea level.
   - No multi bit upsets were detected in the same word, which implies EDAC error correction will be a suitable error mitigation methodology.
4. PLL
   - Observed one PLL loss of lock. However, no phase shift was detected on the flip-flop chains on the DUT and it matched the golden model on the master chip cycle for cycle. It means, the PLL output was not affected even though the PLL lost lock. This corresponds to an upper bound of 0.1 FIT per PLL.

VI. Appendix

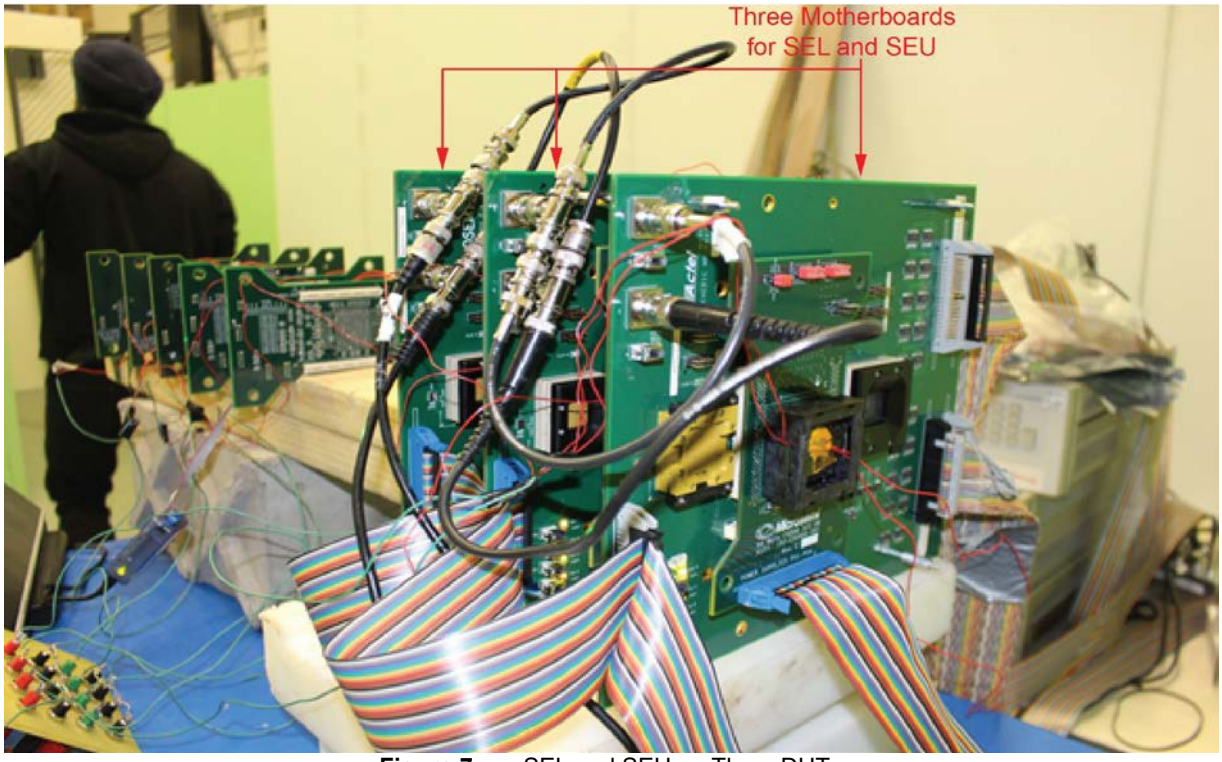

Figure 7: SEL and SEU on Three DUTs

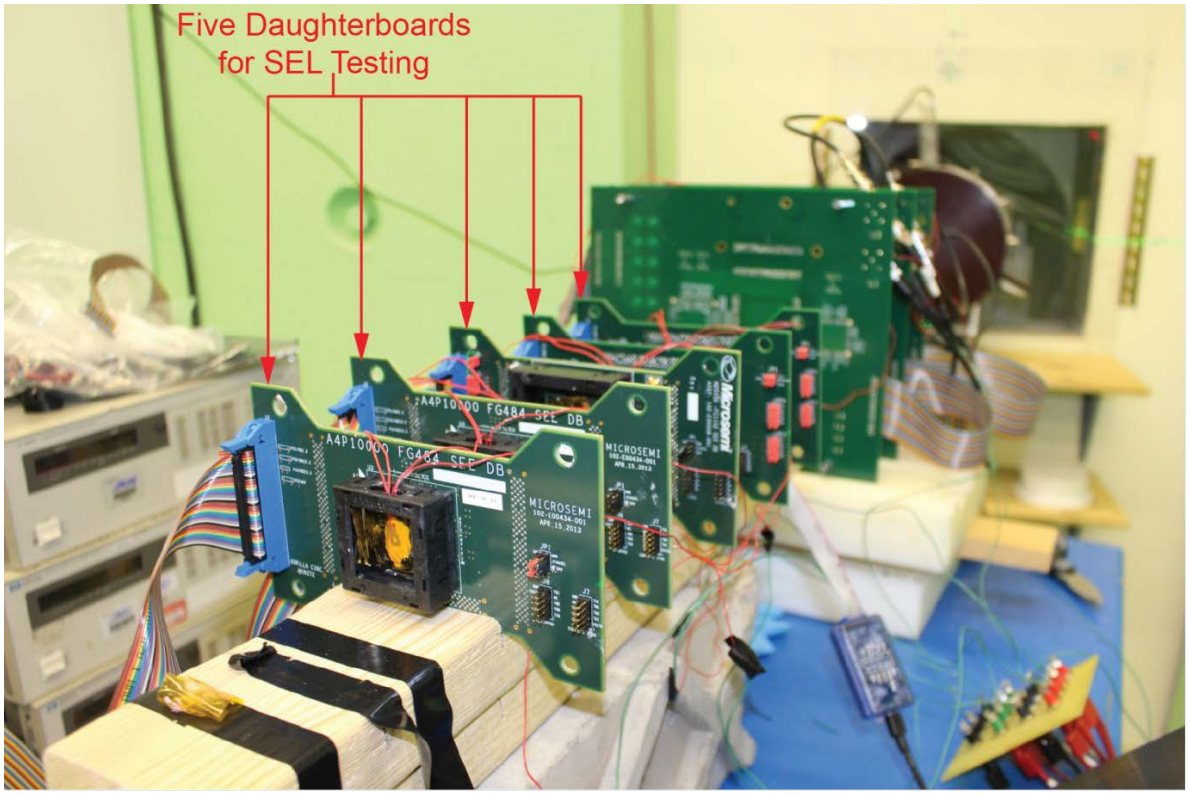

Figure 8: SEL on Five DUTs

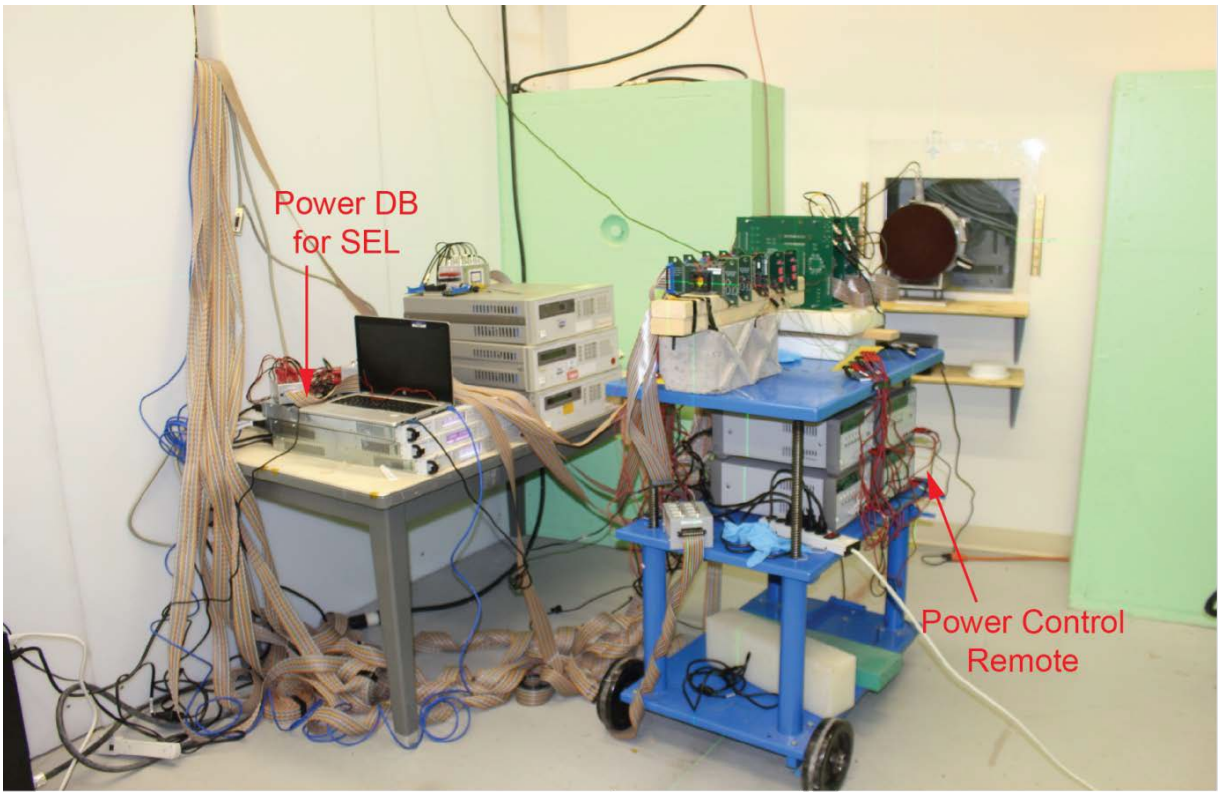

Figure 9: Cave Setup

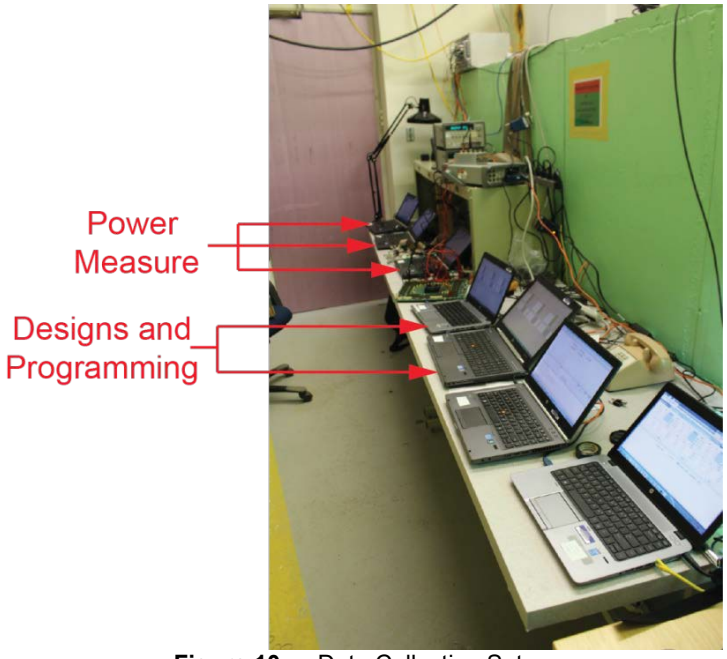

Figure 10: Data Collection Setup

VII. List of Changes

Revision	Changes	Page
Revision 3 (April 2020)	Updated Table 18 to indicate all devices were tested in avionics mode (system controller was disabled).	26
Revision 2 (August 2015)	Updated Table 18 (SAR 69489).	26
Revision 1 (July 2015)	Initial revision	NA

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