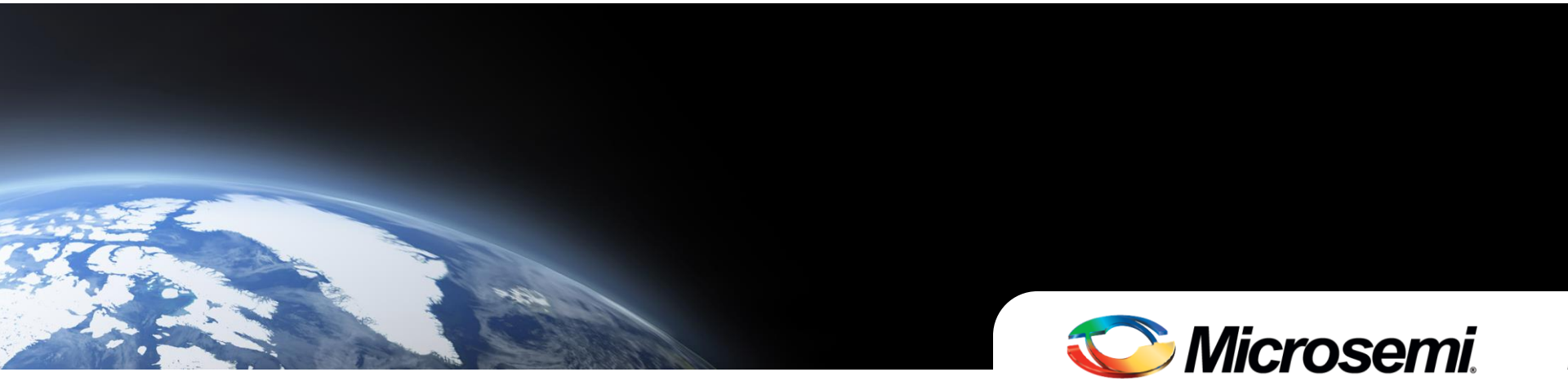
Power Matters.™



Fault Tolerant LEON3 Processor and SpaceWire Router Standard Products

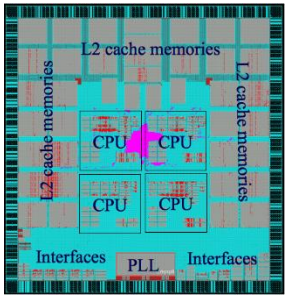
Microsemi Space Forum 2015

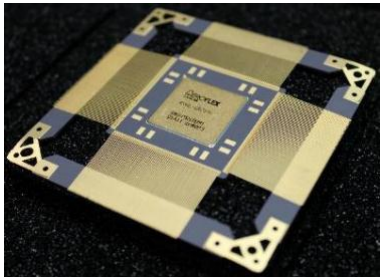
Sandi Habinc
Managing Director, Cobham Gaisler AB

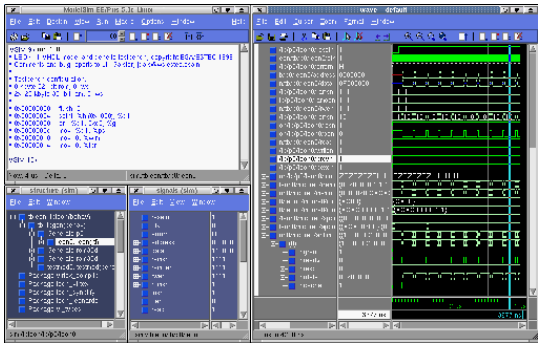
Microsemi SPACE FORUM

Cobham Gaisler Product Portfolio

- LEON3/LEON4 processors
  - Standard version
  - Fault Tolerant version
- LEON compatible IP cores
  - Floating Point Unit
  - Memory Management Unit
  - Memory controllers
  - Serial and parallel interfaces







- TSIM and GRSIM: LEON simulators
- GRMON: LEON debug monitor
- RTOS: VxWorks, ThreadX, Linux, RTEMS, etc.

- LEON development boards
- Test equipment
- Software development environment based on open source tools
- Technical support and adaptations

LEON3 SPARC V8 Processor

- Features
  - IEEE-1754 SPARC V8 compliant, 32-bit processor
  - 7-stage pipeline, multi-processor support
  - Separate multi-set caches with LRU/LRR/RND
  - On-chip debug support unit with trace buffer
  - Highly configurable:
    - Cache size 1-256 KiB, 1-4 sets, LRU/LRR/RND
    - Hardware Multiply/Divide/MAC options
    - MMU, FPU high-performance or small-size
    - Pipeline optimization for specific target technologies
    - Fault tolerance optimization for specific target technologies
    - 20-30 MHz on Microsemi RTAX-S/SL FPGA
    - 25-35 MHz on Microsemi RT ProASIC3 FPGA
    - 80-100 MHz on Microsemi RTG4 FPGA (preliminary)
  - Certified SPARC V8 by SPARC International
  - Suitable for space and military applications
  - Baseline processor for space projects in US, Europe and Asia

SpaceWire Protocol and Interface

- The SpaceWire standard is a self-clocking serial protocol that provides a high speed, low power serial interface while offering a flexible simple user interface
- Protocol is derived from IEEE 1355-1995
- Current standard document is ECSS-E-ST-50-12C
- Physical layer is LVDS ANSI/TIA/EIA-644
  - On-chip or external LVDS drivers
  - Cobham SpaceWire Physical Layer Transceiver (UT200SpWPHY01)
- Industry standard protocol
  - Accepted by all major space organizations: NASA, ESA, JAXA, ISRO, KARI, IAI, ROSCOSMOS, etc.
  - 5th International SpaceWire Conference held in Sweden in June 2013
- Simple user interface
  - 9 or 10 bit transmit & receive on-chip FIFO memories are typical
  - Supports variable packet size and data rates
  - DMA interface, with support for RMAP or RMAP CRC acceleration

LEON3FT RTAX-S/SL & RT3PE

- Processor features
  - 32-bit SPARC V8 processor implemented on pre-programmed RTAX2000S/SL and RT ProASIC3
  - LEON3FT processor core:
    - Harvard architecture with separate caches:
      - 8 KiB Instruction Cache
      - 4 KiB Data Cache
    - Hardware multiply and divide
    - Power-down mode
    - On-chip debug support unit with 4 KiB trace buffer
    - IEEE-754 single/double precision Floating Point Unit (FPU)
    - SPARC Reference Memory Management Unit (MMU)

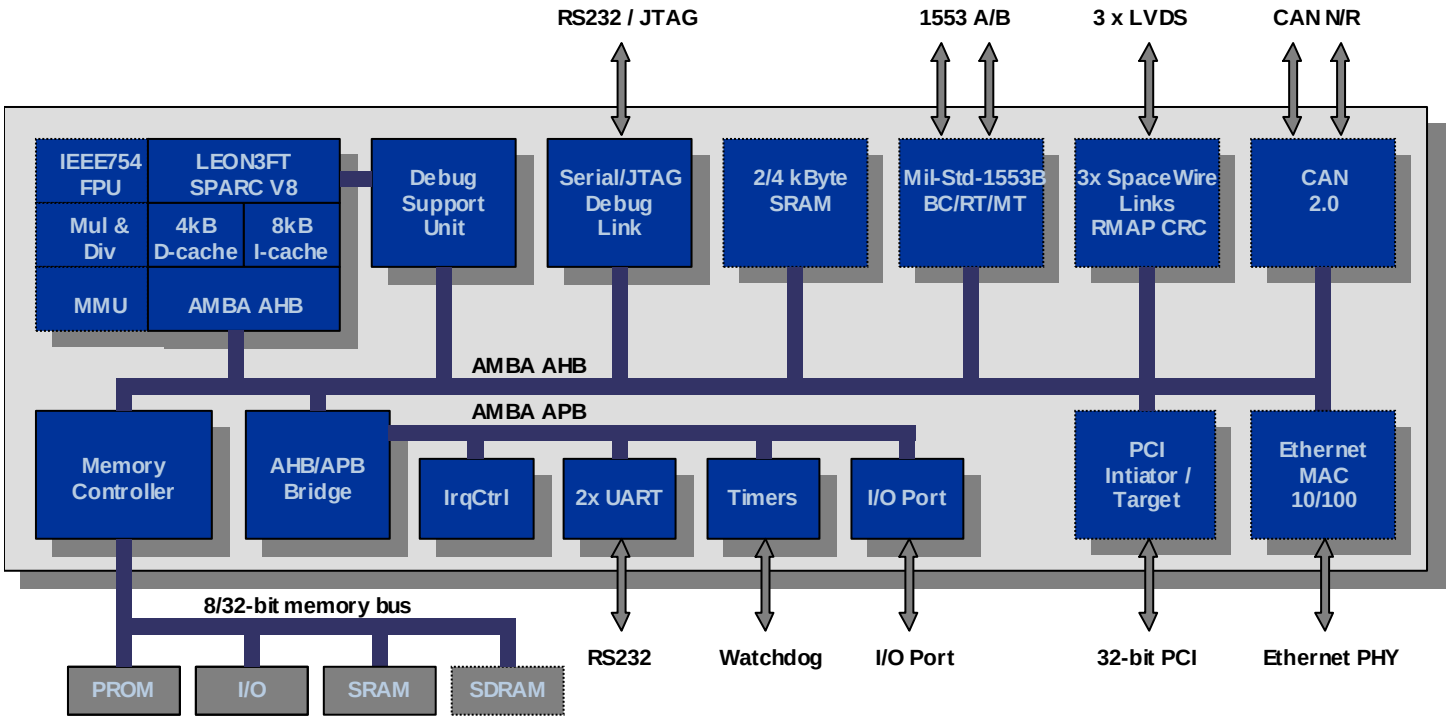
  - Fault tolerant design detects & corrects errors (SEU) in on-chip memory without any performance penalty or software interruption
  - SEU testing performed successfully (reported in 2005)
  - 20 MIPS and 4 MFLOPS @ 25 MHz
  - 25 MHz, 500 mW at 100% load, 380 mW in power-down

LEON3FT Peripherals

- Peripheral features
  - Triple SpaceWire links with RMAP CRC and DMA
  - Redundant MIL-STD-1553 BRM with DMA (based on Microsemi IP core)
  - PCI Initiator / Target / Arbiter with DMA (based on Microsemi IP core)
  - Dual 10/100 Mbit/s Ethernet MAC with DMA
  - Redundant CAN-2.0 interface with SJA1000 software interface
  - 8/32-bit memory controller for PROM, EEPROM, SRAM and SDRAM with ECC (BCH and Reed-Solomon)
  - 32-bit Timer unit, UARTs with FIFO, 16/32-bit I/O port
  - All IP cores SEU proof

LEON3FT Architecture

- The LEON3FT RTAX-S/SL and RT3PE architectures is based on a common design for all the different configurations, featuring a 32-bit AMBA AHB bus for high-speed communication and a 32-bit AMBA APB bus for peripherals and registers. Several cores are standard, such as the LEON3FT processor, but some are optional, such as the number of SpaceWire links.



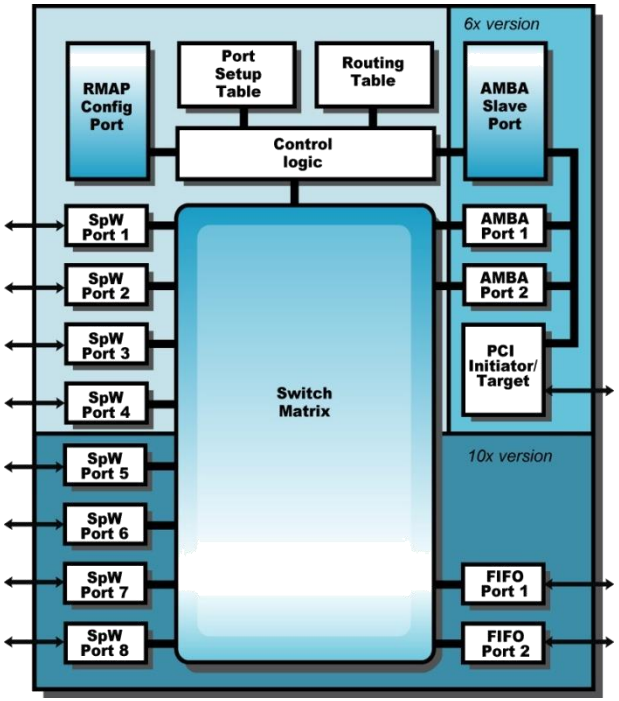
LEON3FT Pre-programmed Configurations

- Standard configurations:
  Instrument Controller, Spacecraft Controller and Payload Controller

Configuration / Feature	IC-1 CID-1	IC-2 CID-2	SC-1 CID-3	SC-2 CID-4	SC-3 CID-5	SC-4 CID-6	PC-1 CID-7	PC-2 CID-8
LEON3FT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FPU	Yes	Yes	Yes				Yes	Yes
MMU					Yes	Yes		
Hardware Mul/Div					Yes	Yes		
Debug Support Unit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
UART Debug Link	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
JTAG Debug Link								
On-chip Memory	4 kB		4 kB					
SpaceWire Links		2		3	2		2	
Mil-1553 RT	1							
Mil-1553 BC/RT/MT			1					
CAN	1				1			
PCI Initiator / Target						Yes		
Ethernet MAC						1		2
Memory Controller	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDRAM support				Yes	Yes	Yes	Yes	Yes
Standard peripherals	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package	CQ352	CQ352	CQ352	CG624	CG624	CG624	CQ352	CQ352
Speed	24 MHz	25 MHz	24 MHz	25 MHz	25 MHz	25 MHz	25 MHz	25 MHz

Radiation Tolerant SpaceWire Router

- Compliant with ECSS-E-ST-50-12C
- Configuration port using RMAP ECSS-E-ST-50-52C
- Wormhole Routing
  - Non-blocking switch-matrix connecting any input to any output
  - Path, Logical and Regional Logical addressing
  - Group Adaptive Routing
  - Packet Distribution
  - Priority levels for output port arbitration
- SpaceWire ports, up to 8 external
  - Up to 200 Mbit/s in both directions per link
  - Support for on-chip or off-chip LVDS
- FIFO ports, 2 external, 9-bit wide, cascadable
- AMBA ports, 2 internal with DMA and RMAP
- PCI initiator and target with DMA, 32-bit, 33 MHz
- System-time distribution via all ports
- Timers on all ports to prevent deadlock

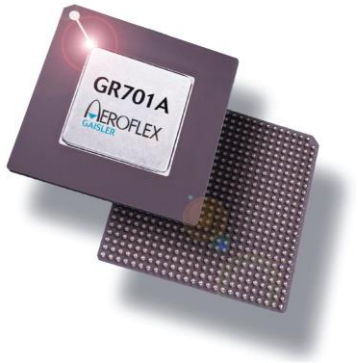


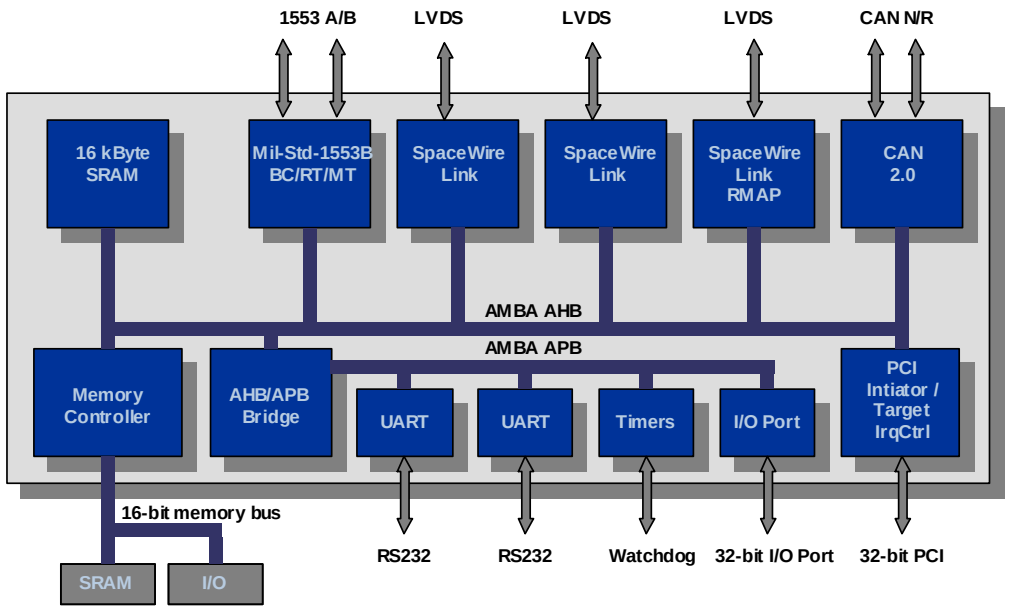
SpaceWire Router Configurations

	RT-SPW-ROUTER-10X	RT-SPW-ROUTER-6X
SpaceWire ports	8	4
FIFO ports	2	
AMBA ports with RMAP		2
Configuration port with RMAP	Yes	Yes
Configuration port with AMBA		Yes
PCI Initiator/Target		Yes
AMBA status		Yes
UART/JTAG Debug Link		Yes
FPGA	Microsemi RTAX2000S(L) CQFP352,CCGA624	Microsemi RTAX2000S(L) CQFP352,CCGA624
	Microsemi RT3PE3000L CCGA484	
SpaceWire physical interface	LVTTL	LVTTL
	LVDS	LVDS

GR701A PCI to SpW, 1553B and CAN

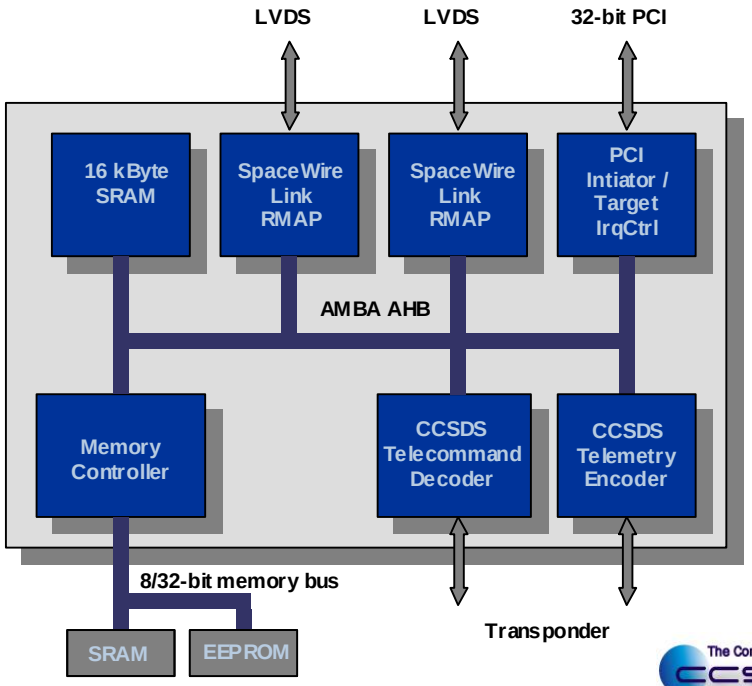
- GR701A companion chip for processors and PCI systems implemented on RTAX2000S/SL FPGA
- PCI bus Initiator and Target, 32-bit, 33 MHz
- 3 SpaceWire links with RMAP, 80 Mbit/s
- Redundant MIL-STD-1553 BRM
- 16 KiB EDAC protected on-chip SRAM
- 8-bit EDAC protected bus to external memory
- 2 UART/RS232
- 16-bit I/O port
- Timers and watchdog
- CQFP352 package



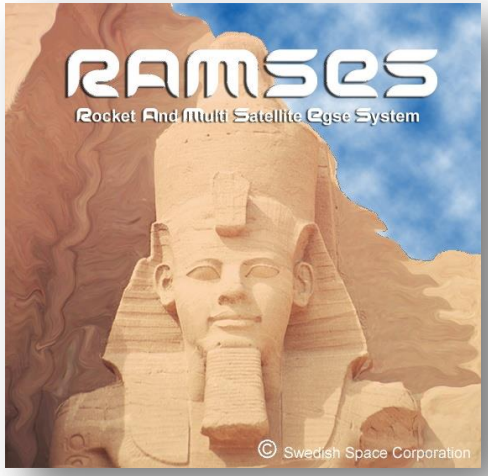


GR703 Telemetry & Telecommand

- GR703 companion chip provides PCI based processors with SpaceWire interfaces and CCSDS telemetry encoding and telecommand decoding capabilities, such as protocol sub-layer handling, Reed-Solomon and con-volutional encoding, BCH decoding, pseudo-randomization



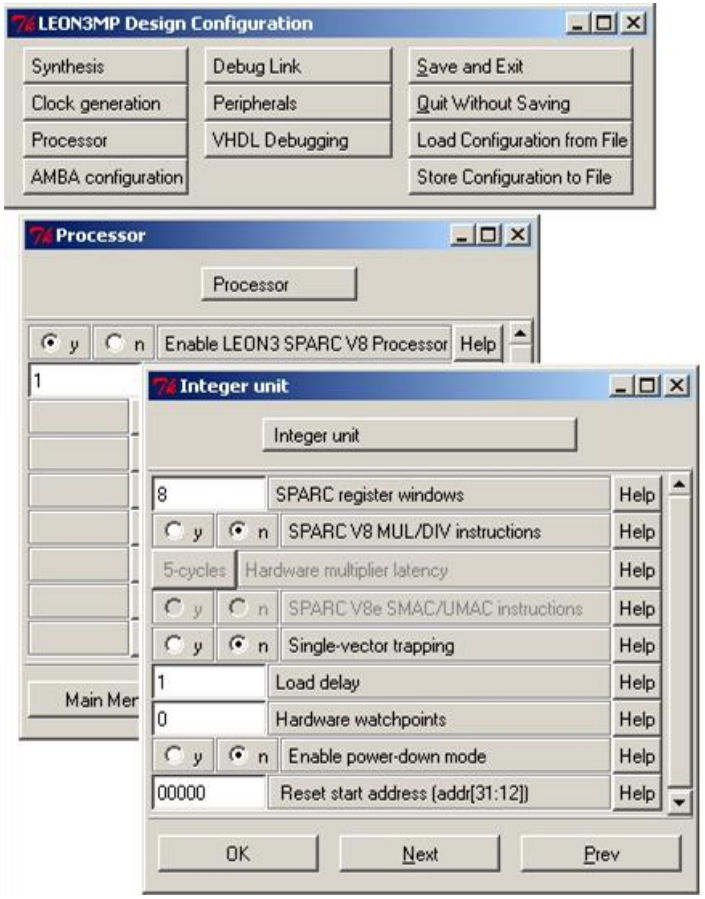
- CCSDS TM/TC ground station / EGSE available for development and testing



The Consultative Committee CCSDS.ORG for Space Data Systems

Custom Configurations

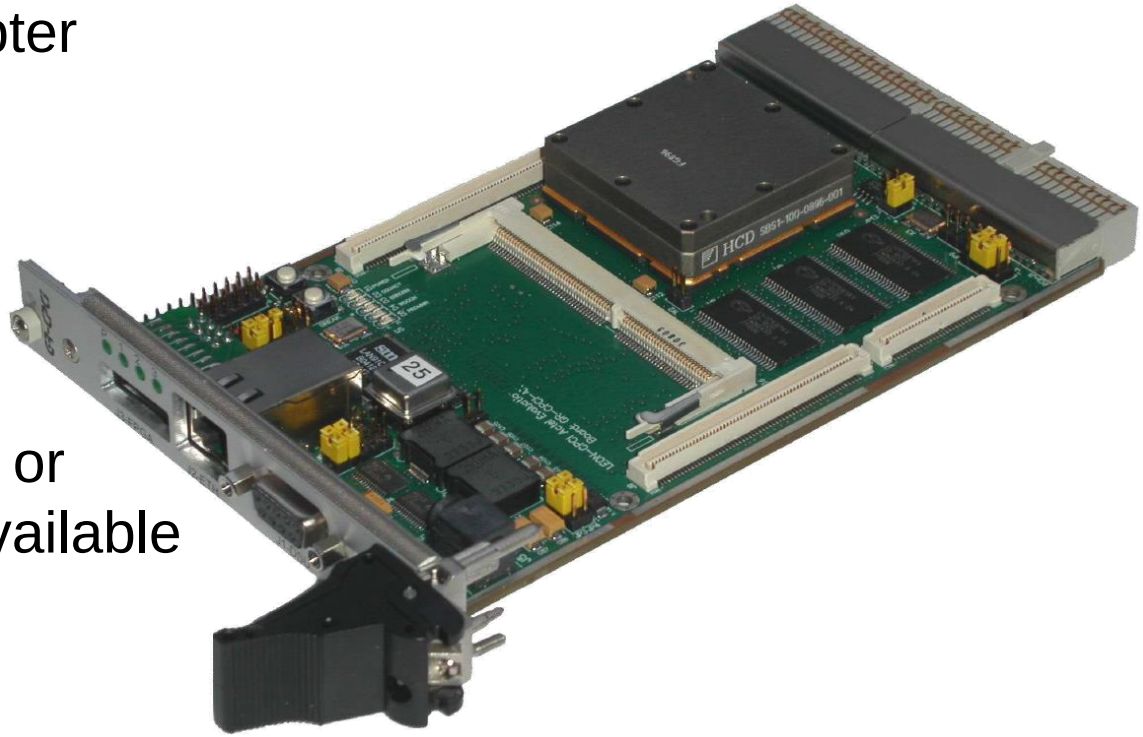
- All our LEON3FT and SpaceWire products are based on GRLIB VHDL IP core library, which is a complete System-on-Chip design environment available for end-user development:
  - Processors
  - Peripherals
  - Memory controllers
  - Serial and parallel high speed interfaces
  - AMBA on-chip bus with Plug & Play support
  - Fault tolerant and standard version
  - Support for many tools & prototyping boards
  - Support for portability between technologies
- Custom LEON3FT configurations based on the current architecture are possible (additional NRE)
- Cobham Gaisler can also integrate customer-furnished IP cores
- Flexible licensing (per FPGA or project)



Supported RTAX-S/SL Devices

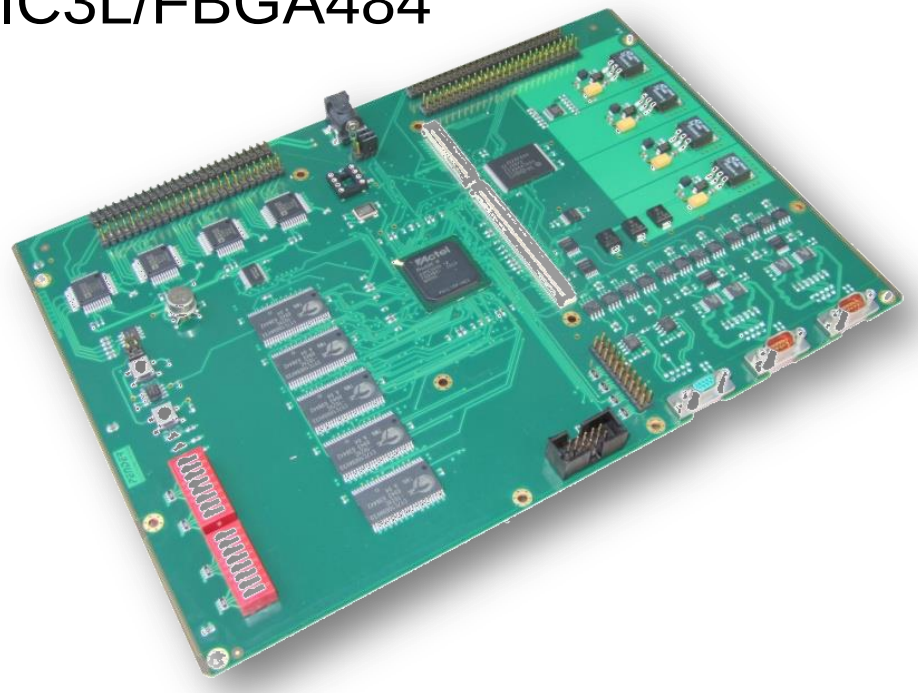
- LEON3FT-RTAX-S/SL, RT-SPW-ROUTER, GR701A & GR703 delivered in all quality levels as pre-programmed components
- All LEON3FT-RTAX-S/SL standard configurations available now
- RT-SPW-ROUTER 10x and 6x configurations available now
- Hi-rel parts available in CQFP352 and CCGA624 packages
- Low-cost prototypes on AX2000/FBGA896 are available using an adapter

- Prototyping board for RTAX2000S/CCGA624 or AX2000/FBGA896 is available from Cobham Gaisler



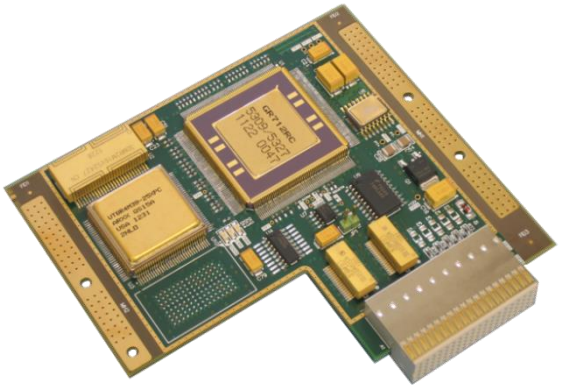
Supported RT ProASIC3 Devices

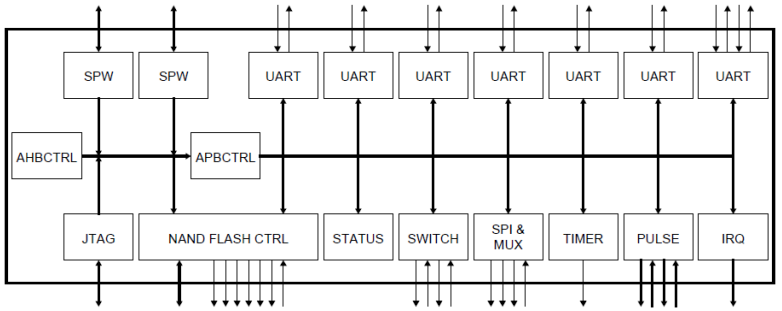
- LEON3FT-RT3PE and RT-SPW-ROUTER delivered in all quality levels as pre-programmed off-the-shelf components
- All LEON3FT-RT3PE standard configurations available now
- RT-SPW-ROUTER 10x configuration available now
- Hi-rel parts available in CCGA484 packages
- Low-cost prototypes on ProASIC3L/FBGA484
- Prototyping board is available from Cobham Gaisler
- Support for FlashPro4 cable for programming and software debugging with GRMON



Example of custom design - MASCOT

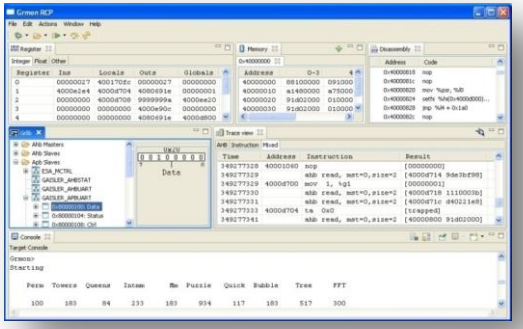
- MASCOT asteroid lander on-board computer developed by Cobham Gaisler for DLR, launched in December 2014 with the Hayabusa-II probe
- Fully redundant computer based on GR712RC Dual-Core LEON3FT processor device and RT ProASIC3 FPGA for I/O functions
- RT ProASIC3 FPGA design fully based on GRLIB IP cores, including the SpaceWire router

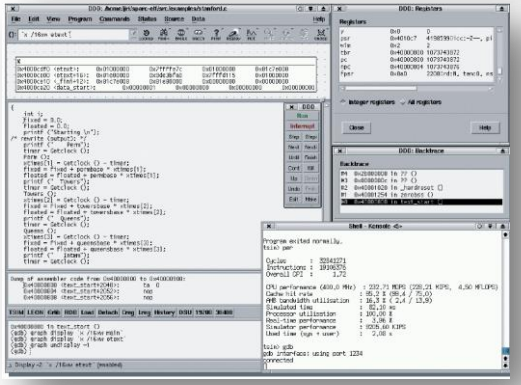




Development Tools and Operating Systems

- GRMON hardware debug monitor:
  - Supporting all kernels/compilers
  - Command line or Tcl/Tk
  - GDB remote debug support
- TSIM behavioral simulator:
  - Single-core LEON2/LEON3/LEON4
  - Code coverage, profiling, back trace
  - High-performance (> 30 MIPS)
  - Command line or Eclipse IDE
  - GDB remote debug support
- Support for several open-source software:
  - RTEMS, Linux 3.10, eCOS
  - GNU GCC compiler and associated tools
- LEON3 port and BSP available for VxWorks 6.7 and ThreadX
- Software drivers available for SpaceWire, MIL-STD-1553, CAN, PCI, etc.





Designing with RTG4 and LEON3FT/GRLIB

- Current state of RTG4 support in LEON3FT/GRLIB
  - LEON3FT and basic peripherals fully mapped to RTG4
  - GRLIB technology map (e.g. memories, pads) in place
  - Script generation adapted to support IGLOO2/SF2 and RTG4
  - Template designs ready
    - IGLOO2 Stater Kit
    - SmartFusion2 Security Evaluation Kit
    - SmartFusion2 Advanced Development Kit
    - RTG4 Development Kit
- Bridges to interface hard system are in place
- Basic software support for initialization of hard system
- Wrappers to support more complex macros are in place (e.g. SerDes) or in development (e.g. PCIe controller)
- LEON3FT/GRLIB IP offering for RTG4 in place

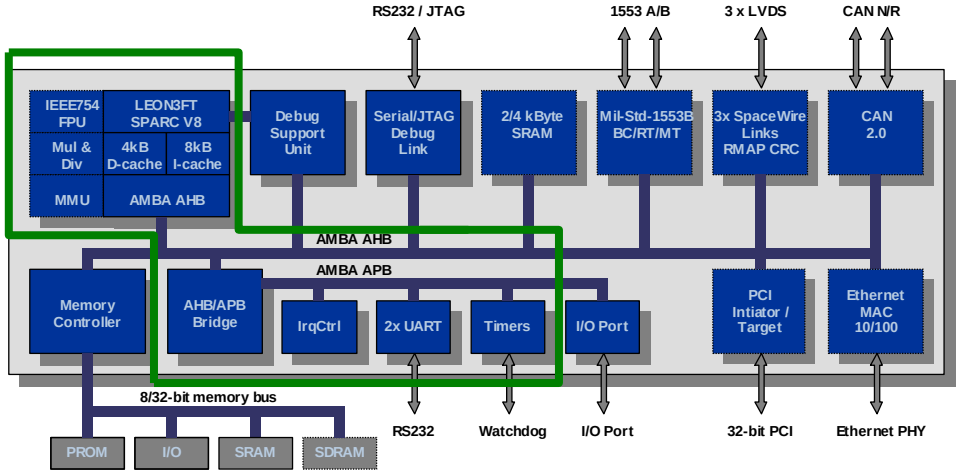
Migrating existing GRLIB designs to RTG4

- Option 1: Move existing design, do not use hard system
  - Straightforward provided that existing designs have proper separation between technology agnostic parts and target technology elements
  - Reset and clocking strategy may need an update
- Option 2: Adapt design to use hard system & complex macros
  - Use Libero build system, or use a pre-generated system
  - Existing memory controller needs to be replaced with bridge that connects to hard system
  - Software will need updating to handle hard system

LEON3FT RTG4 example implementations

- RTG4 post-layout resource usage for a processor core design (i.e. processor, timer unit, UART, interrupt controller)
- RT4G150, Temp=Voltage=MIL, Standard speed

Design	4LUT	DFF	Logic Element
LEON3FT TINY system	2521 (1.7%)	1196 (0.8%)	2557 (1.7%)
LEON3FT MIN system	4967 (3.3%)	1686 (1.1%)	5029 (3.3%)
LEON3FT GP system	13021 (8.6%)	5026 (3.31%)	13371 (8.8%)
LEON3FT HP system	31041 (20.5%)	10084 (6.6 %)	32002 (21%)



Conclusions

- LEON3FT-RTAX-S/SL and LEON3FT-RT3PE: a flexible pre-programmed solution for platform, payload and instruments
- RT-SPW-ROUTER 10x and 6x SpaceWire router:
  - 200 Mbit/s in both directions
  - 16x router through bridging without any extra glue logic

- Quick turn-around time for custom configurations
- Lower-cost prototype solutions available

- LEON3FT/GRLIB now supports RTG4!
- RTG4 brings significant performance improvement to LEON3FT compared to previous FPGA generations

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Thank You

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