Power Matters.™

ESIstream© Protocol Presentation

Microsemi

More Useful data

Less overhead

Open protocol

Simpler Hardware implementation

e2v’s data converters are microwave capable, they are used in Space primarily for :

- Telecommunication Payloads
- SAR Radar remote sensing payloads
- LiDAR.
- Altimeters using GNSS Reflectrometry.
- TWTA signal processing feedback loops.
- GNSS Software defined navigation signals.

Agenda

ESIstream
The Efficient Serial Interface

Main benefits and introduction

I / Encoding

II / Scrambling

III / Disparity

IV / Synchronization

V / Multiple lanes configuration

Conclusion

Main benefits

ESIstream
The Efficient Serial Interface

More Useful data

Less overhead

Open protocol

Simpler Hardware implementation

High efficiency data rate:	87.5% of useful data
Simple hardware implementation:	Sub-10 pages specifications
Guaranteed DC balance transmission:	±16 running disparity
Sufficient number of transitions:	Max run length of 32bits
Synchronisation monitoring:	Using Clk bit
Deterministic latency & Multiple lanes configuration	Yes.

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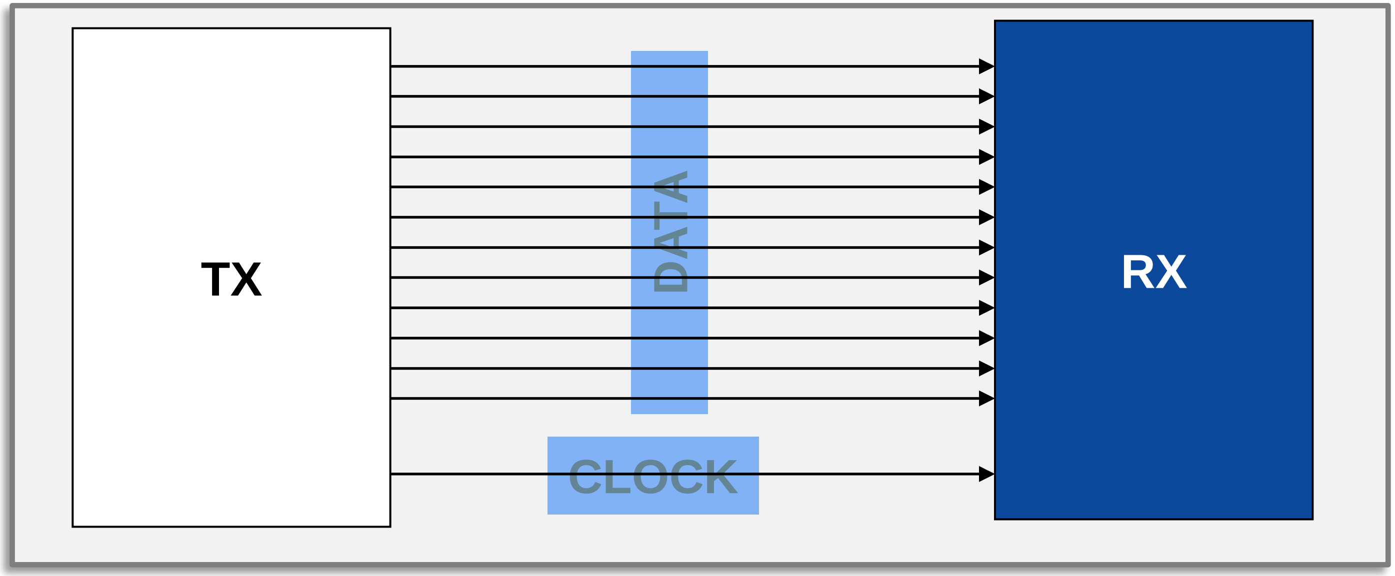
Introduction 1/3
Using a parallel interface

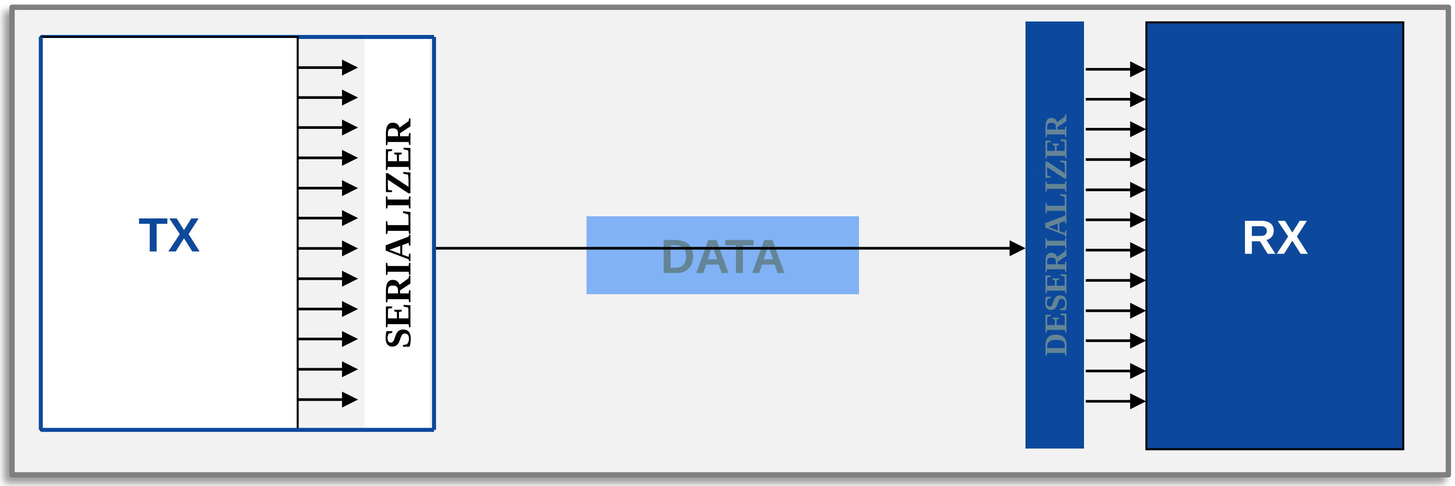


Cons
- Many traces
- Requires trace lengths control

Pros
- Minimum Latency
- No additional data processing

Introduction 2/3

Using a serial interface



Cons

- Processing required to implement the transmission protocol.
  - ESIstream simplifies serial data processing.
- Increased latency due to protocol implementation
  - ESIstream improves latency with reduced data overheads.

Pros

- Less PCB traces
- Clock is recovered from data stream
- Relaxed PCB trace lengths requirements

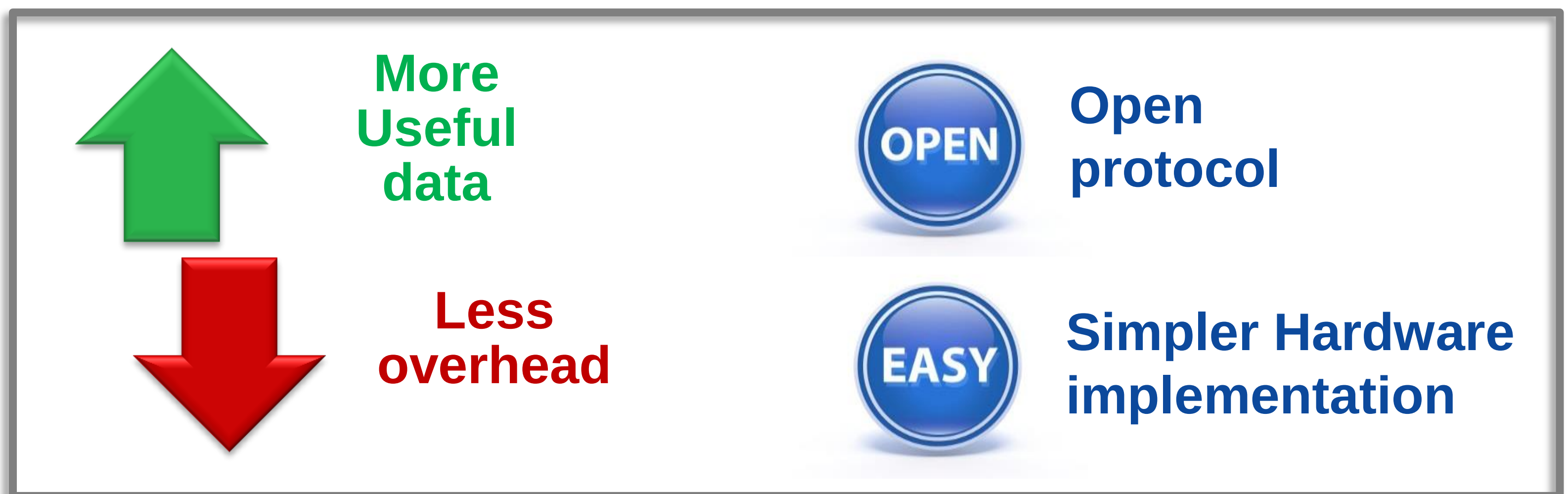
Introduction 3/3
Why ESIstream?

ESIstream
The Efficient Serial Interface

The ESIstream protocol is born from a severe need of the following combination:

- Reduced overhead on serial links, as low as possible.
- Increased rate of useful data when linking ADCs & DACs operating at GSPS speeds with FPGAs on a serial interface.
- Simplified hardware implementation; simple enough to be built on RF SiGe technologies.

An early form of ESIstream has been implemented in EV5AS210, a 5bit 20GSPS demonstrator ADC from e2v.
The protocol has now matured and is being implemented in other devices.
It works on standard FPGA high-speed transceiver/serdes I/Os.



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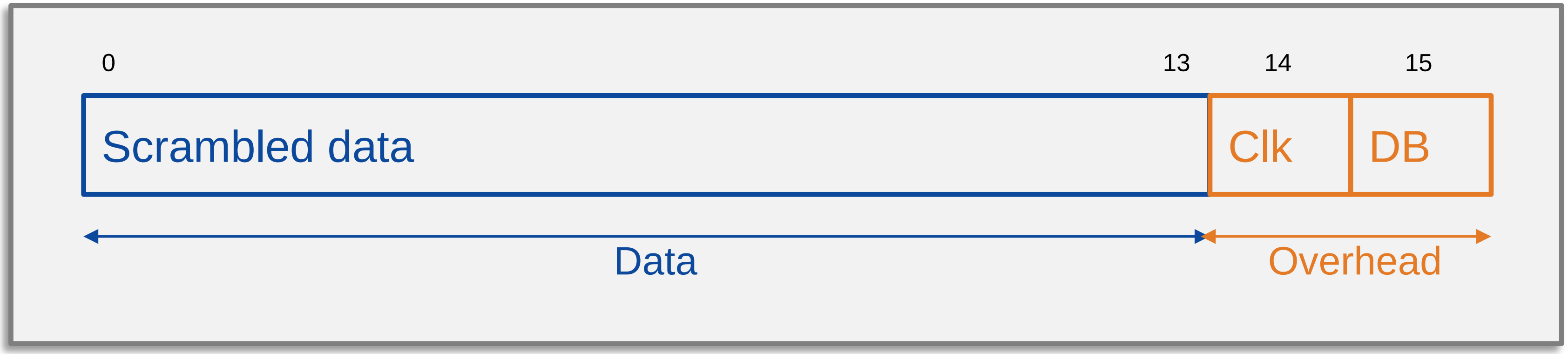
Encoding
14bits/16bits

The ESIstream protocol is based on a 14b/16b encoding which gives a data rate efficiency of 87.5%.

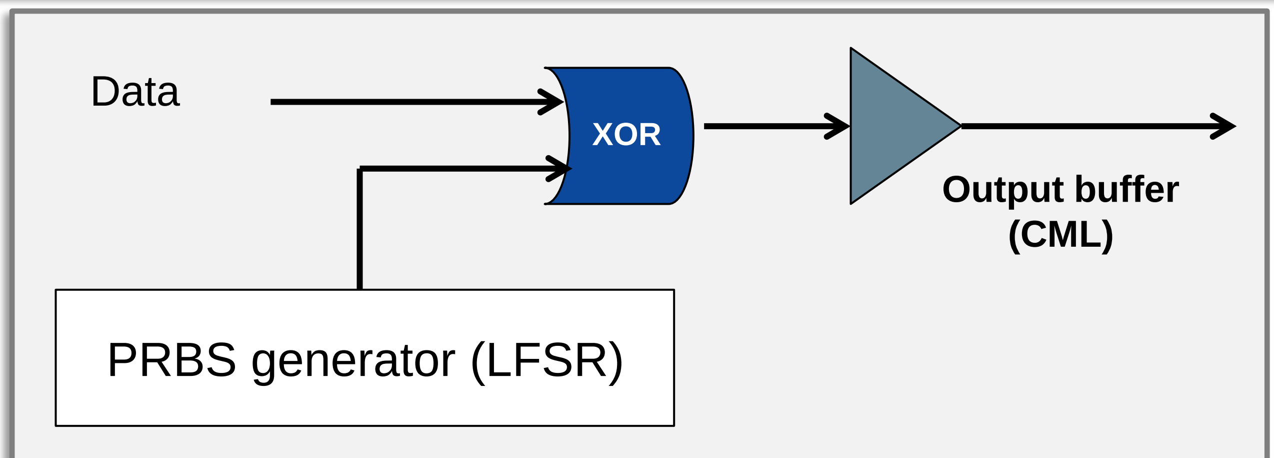
A frame contains 14 bits of data and 2 bits of overhead.
The 14 bits of data are scrambled.
The overhead includes a Clk bit which alternates between ‘0’ and ‘1’ and which is used to monitor the synchronization of the transmision.
The overhead also includes a disparity bit to ensure a DC balanced transmission.



The scrambling process

The scrambling process is needed for 3 reasons:

- It ensures that there are transitions in the transmission (needed for the CDR), in addition to the Clk bit in the overhead.
- It ensures a statistical overall DC balanced transmission (for AC coupling system).
- It spreads the spectral content.



Disparity
Principle

In some highly unlikely cases, despite the scrambling process, the transmission might not be DC balanced overall. This will cause a problem to the reception after some time.

To prevent these cases from occuring, a disparity bit is added.

Running disparity (RD) :

The running disparity is the difference between the number of '0' and '1' sent overall.

0	1	1	0	1	0	0	1	0	1	0	0	0	0	0	RD = -5

Disparity bit (DB) :

If the frame increases the running disparity above a certain threshold (+/-16), all the bits of the frame except the disparity bit are inverted. The disparity bit is put to '1' in that case, so the RX recognizes that the data were inverted.
This ensures that the protocol has a max run length of 48bits. Taking into account the Clk bit, the maximum run length of the protocol is 32 bits.

Disparity

Example of disparity bit

At some time t_i during the transmission $RD(t_i) = -5$.
The following 15 bits of data need to be sent.

t_i	0	1	0	0	0	0	1	0	0	1	1	0	0	0	0	$D_w = -7$

This 15 bits word adds a -7 to the running disparity, the updated RD does not exceed -16, thus the disparity bit is at '0' and the data are not inverted. The frame sent at t_i is then:

t_i	0	1	0	0	0	0	1	0	0	1	1	0	0	0	0	0	← DB

When DB=0 data is not inverted

Thus $RD(t_{i+1}) = RD(t_i) + D_w – 1(\text{for DB}) = -13$

The next data to send is:

t_{i+1}	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	$D_w = -5$

This 15 bits word adds a -5 to the running disparity, the updated RD exceeds -16, thus the disparity bit is at '1' and the data are inverted. The frame sent at t_{i+1} is then:

t_{i+1}	1	1	1	1	1	0	0	0	1	0	1	1	1	1	0	1	← DB

When DB=1 data is inverted

Thus $RD(t_{i+2}) = RD(t_{i+1}) – D_w +1(\text{for DB}) = -7$

Synchronization

TX/RX Frame alignement

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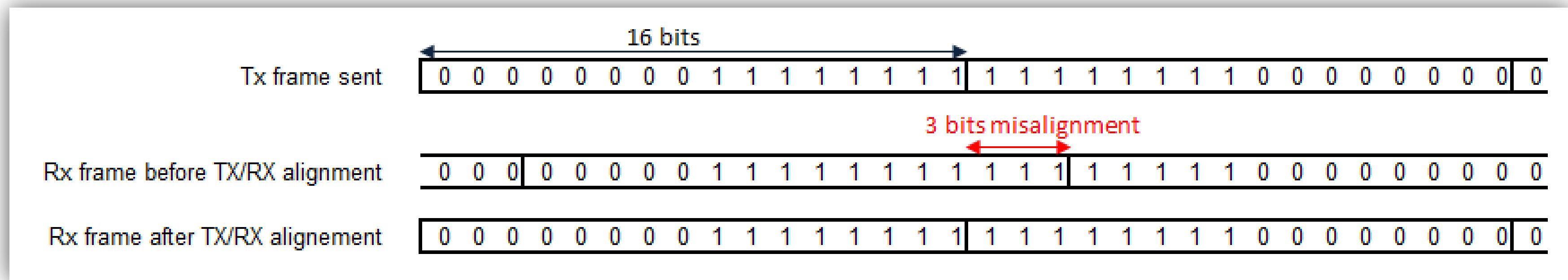
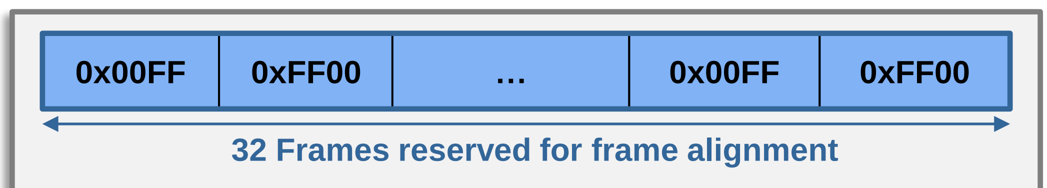
The Efficient Serial Interface

The first step of the TX/RX alignment procedure consists in aligning the frames sent by TX with the 16 bits word obtained at the output of the RX deserializer.



To correct frame misalignment, TX sends a known sequence for 32 frames used by RX to align its 16bits word to the TX frames.



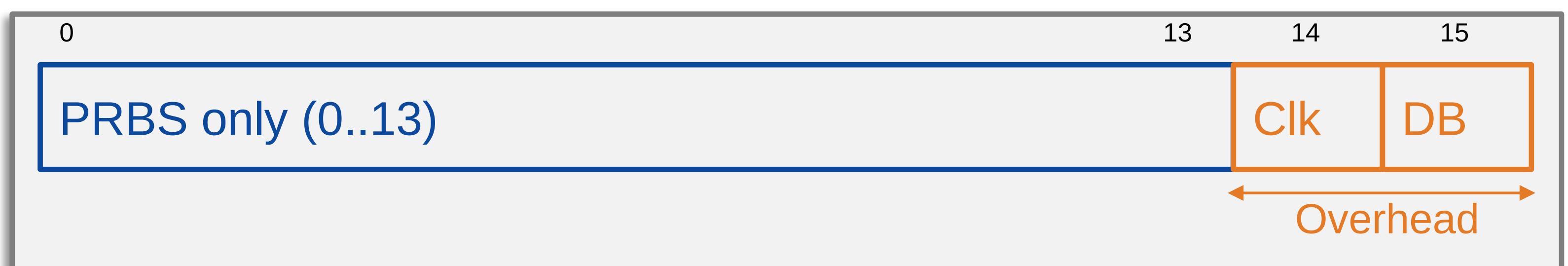
After system start-up, the RX sends a SYNC pulse to the TX which starts the synchronization process of the serial interface.
The RX then seeks the comma 0x00FFFF00 or 0xFF0000FF to align its frames with the TX's.

Synchronization
TX/RX PRBS alignement

The next step is to align the RX PRBS with TX PRBS.
To achieve that, the TX sends the PRBS value for 32 frames after the alignment sequence:

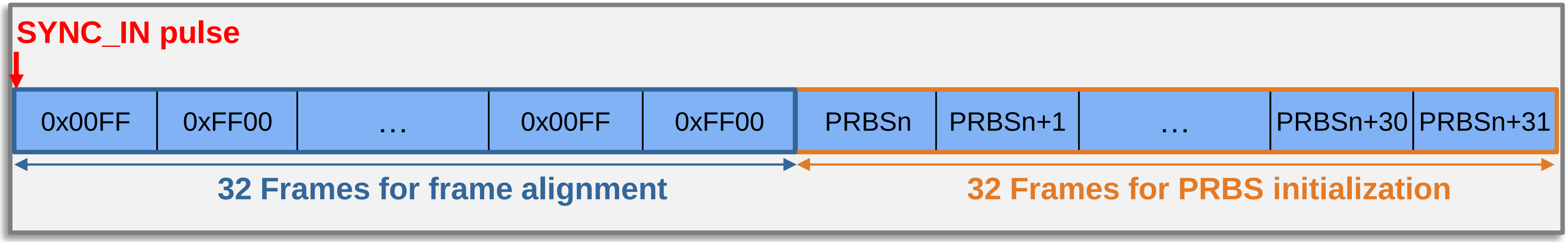
The RX initialises its PRBS using the values it receives from the TX.

The frame during this sequence contains the Clk bit and the disparity bit as the PRBS sequence may impact the running disparity of the transmission:



Synchronization
Process overview

The complete synchronization sequence contains 2 parts of 32 frames to realize TX/RX frames alignement and TX/RX PRBS alignement:



After this sequence, TX and RX are synchronized.

Lengths of 32 frames are sufficient to allow the RX to process the synchronisation successfully and to be ready to process the useful data at the end of a synchronisation sequence without additional buffer to the data path.

Deterministic latency

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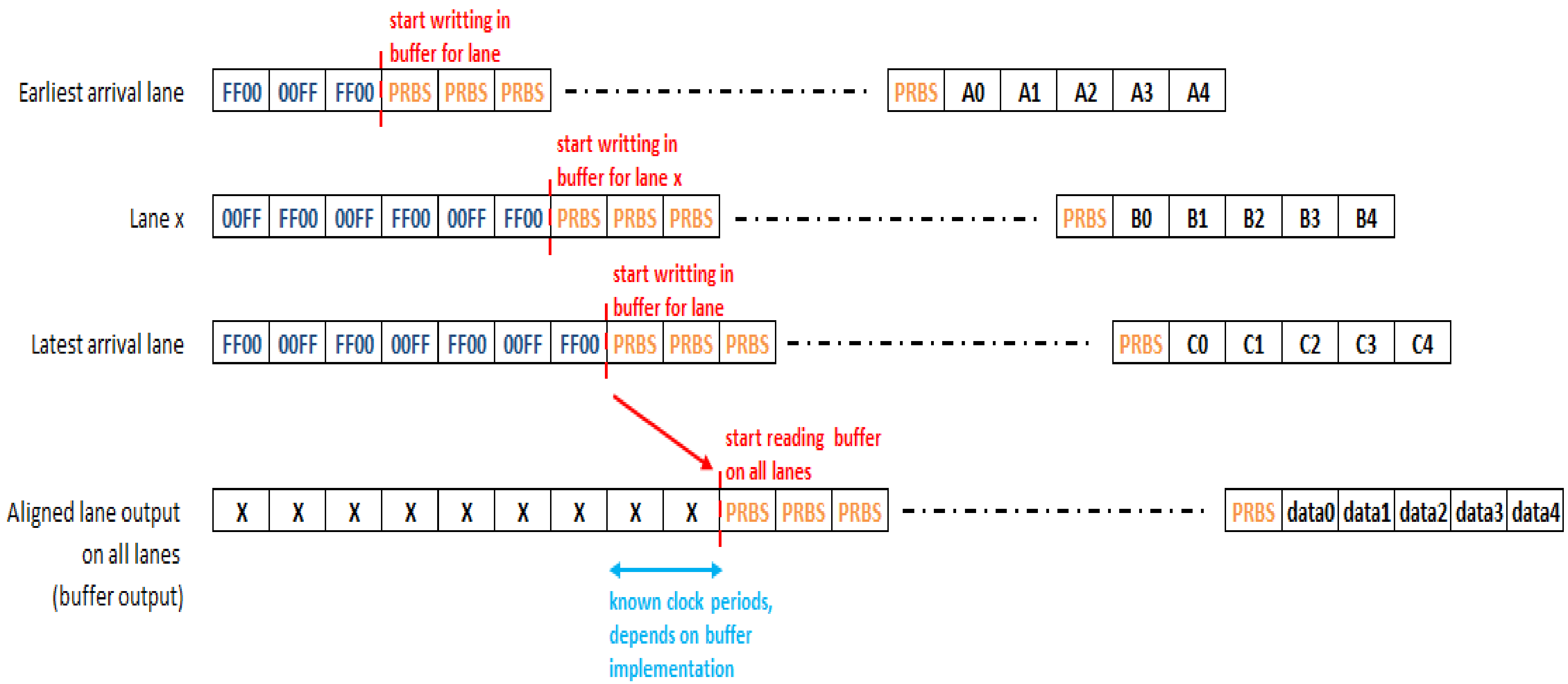
Using the synchronization sequence, deterministic latency systems can be implemented, using buffer at the reception stage.



Multiple Lanes configuration
Implementation example.

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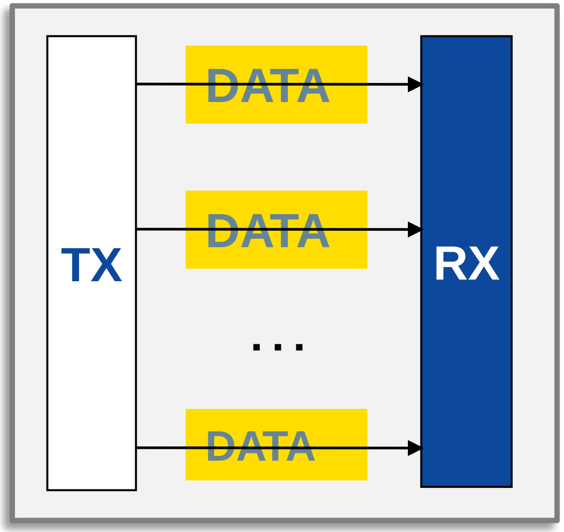

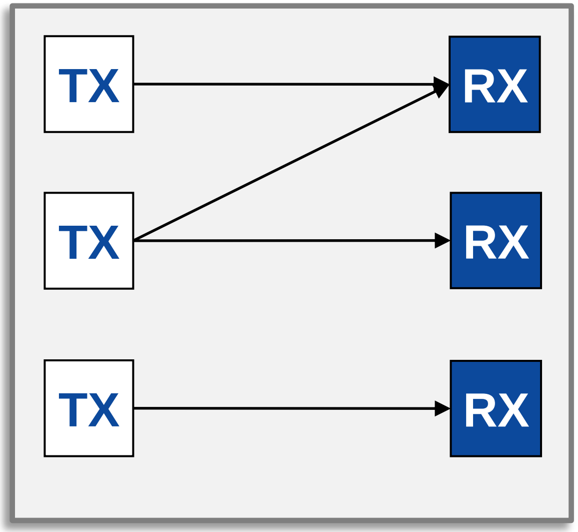

In case of multiple lanes configuration, in order to avoid cross-lane correlation issues the PRBS sequences between lanes should not be aligned.

To align multiple lanes at RX level, the synchronization sequence can be used.
The first frame of the PRBS synchronization sequence can be used as a stamp to realign all lanes together.

If multiple TX units using single or multiple lanes configuration need to be synchronous, the TX units need to start sending the synchronization sequence with a known relation between them so that the RX units can realign them.
If multiple RX units are used, then they need to be synchronized in order to synchronize all lanes together.

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Example with Microsemi FPGA

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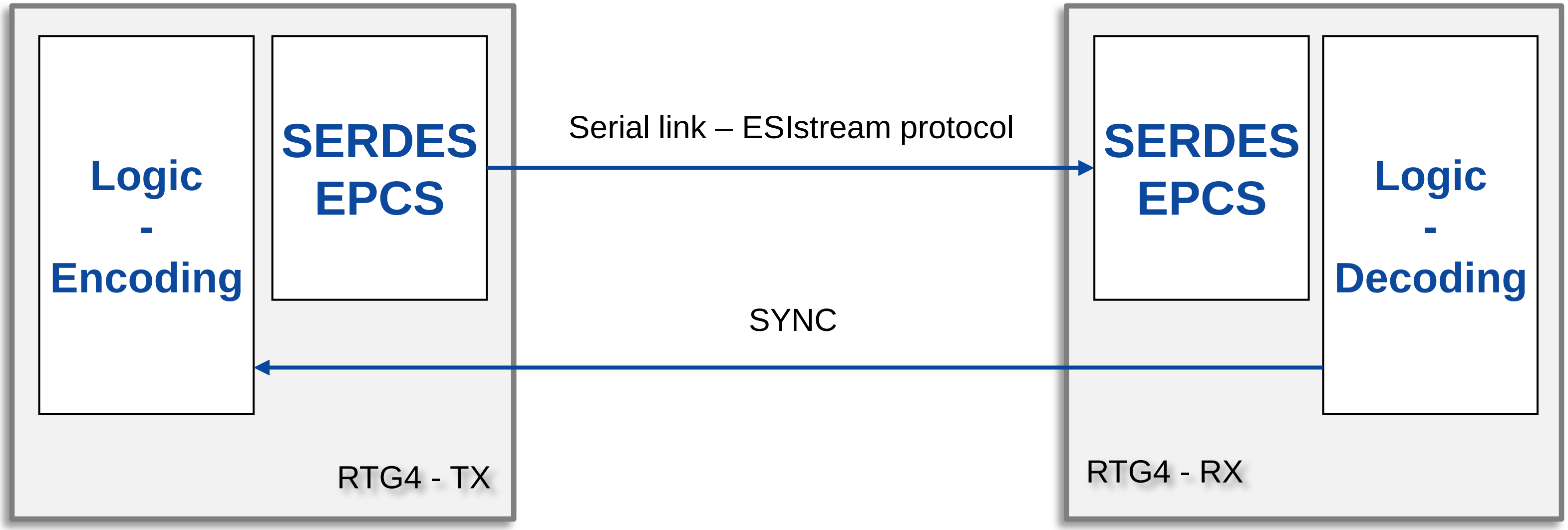

The ESIstream protocol can be used with Microsemi FPGAs to increase the efficiency of a serial interface.

The example above shows the architecture when using a unique serial link. However, the RTG4 allows 24 serial lanes so the system could use up to 24 lanes with one SYNC signal to transmit efficiently high quantity of data between devices that support high-speed serial transmission.

Summary of benefits

More Useful data

Less overhead

OPEN **Open protocol**

EASY **Simpler Hardware implementation**

High efficiency data rate:	87.5% of useful data
Simple hardware implementation:	Sub-10 pages specifications
Guaranteed DC balance transmission:	±16 running disparity
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Deterministic latency & Multiple lanes configuration	Yes.

Document download

ESIstream
The Efficient Serial Interface

Download the latest ESIstream documents on:

http://www.esistream.com/download-area/

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Thank You

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