SmartFusion2, IGLOO2, and RTG4

Hard Multiplier AddSub Configuration

Microsemi

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Introduction

The Hard Multiplier AddSub for SmartFusion2, IGLOO2, and RTG4 supports normal (Figure 1) and dot product (Figure 2) multiplication. Blue registers indicate control signals; brown registers are for data.

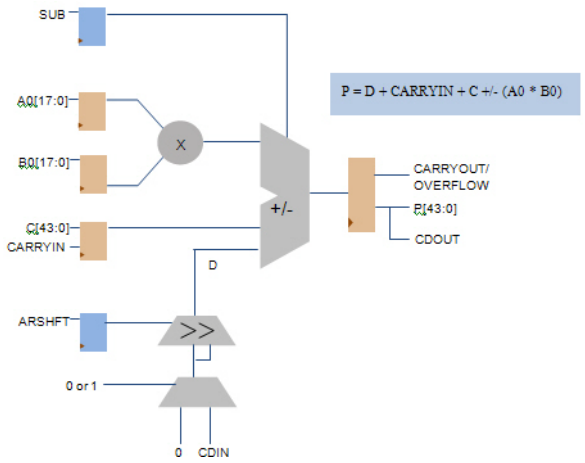

***Figure 1* • Normal Multiplier AddSub**

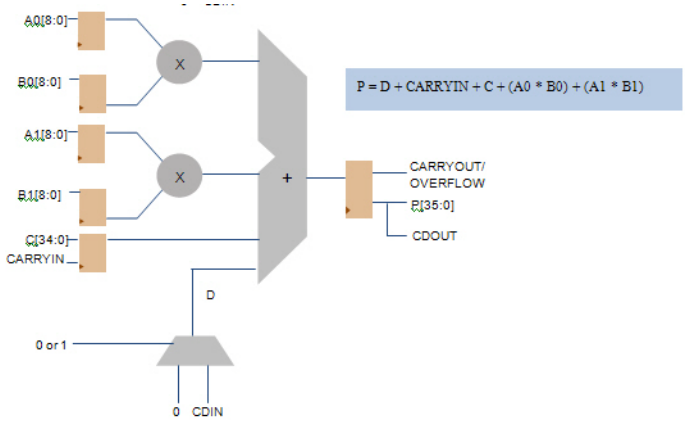

***Figure 2* • Dot Product Multiplier Add**

Key Features

The Hard Multiplier AddSub supports two operating modes: Normal and Dot Product.

- A structural netlist is generated in either Verilog or VHDL.
- Individual inputs and outputs can be optionally registered with:
  - A common rising edge clock
  - Independent active-low asynchronous and synchronous clear controls
  - Independent active-high enable controls

- An additional cascade output CDOUT can be enabled. This is the sign-extended 44 bit copy of output P.
- An additional cascade input CDIN from previous math block can be enabled.
- An additional Carry In input can be enabled.
- An additional Carry Out or Overflow output can be enabled.
- Normal Mode Features:
  - Configurable operand widths for A0 and B0 between 2 and 18
  - Configurable operand width for C between 2 and 44
  - Optional assignment of operand A0 to an 18 bit two's complement constant
  - Optional assignment of operand C to a 44 bit two’s complement constant
  - Option to select between Multiplier followed by Adder, Subtractor or dynamic AddSub
  - Optional Arithmetic Right Shift by 17 bits of the Cascade input
- Dot Product Mode Features:
  - Configurable operand widths for A0, B0, A1, B1 between 2 and 9
  - Configurable operand width for C between 2 and 35
  - Optional assignment of operand A0 and A1 to a 9 bit two's complement constant
  - Optional assignment of operand C to a 35 bit two’s complement constant

1 – SmartDesign

The Hard Multiplier AddSub for SmartFusion2, IGLOO2, and RTG4 is available for download from the Libero® SoC IP Catalog via the web repository. Once listed in the Catalog you can double-click the macro to configure it in SmartDesign. For information on using SmartDesign to configure, connect, and generate cores, see the Libero SoC online help.

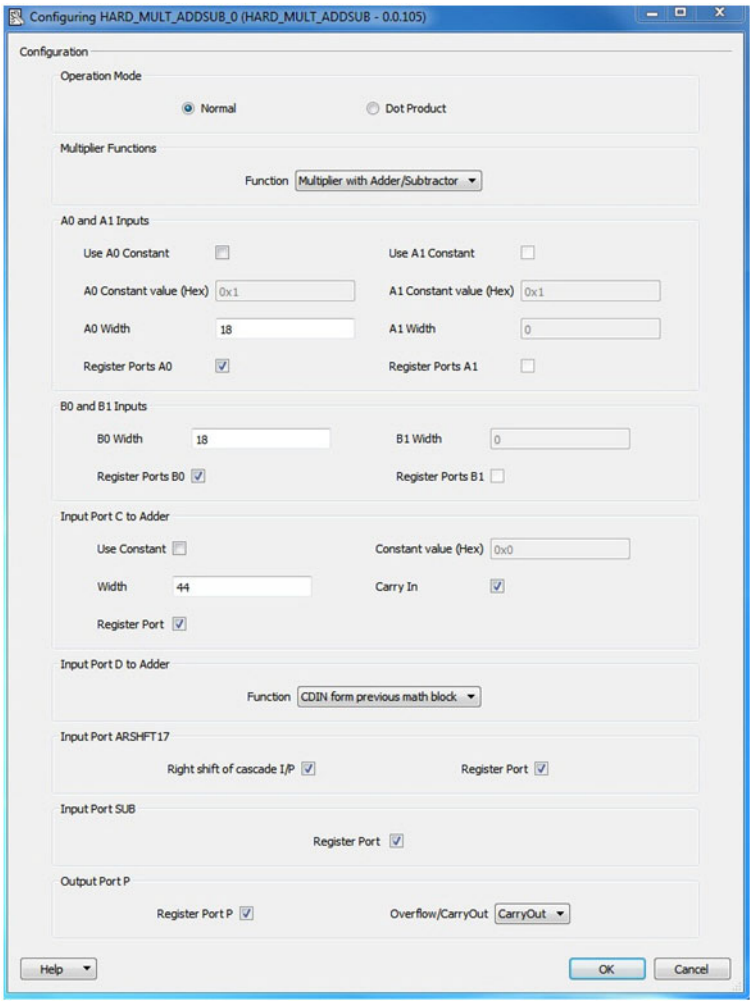

Figure 1-1 **• Hard Multiplier AddSub Configuration Options - Normal Mode**

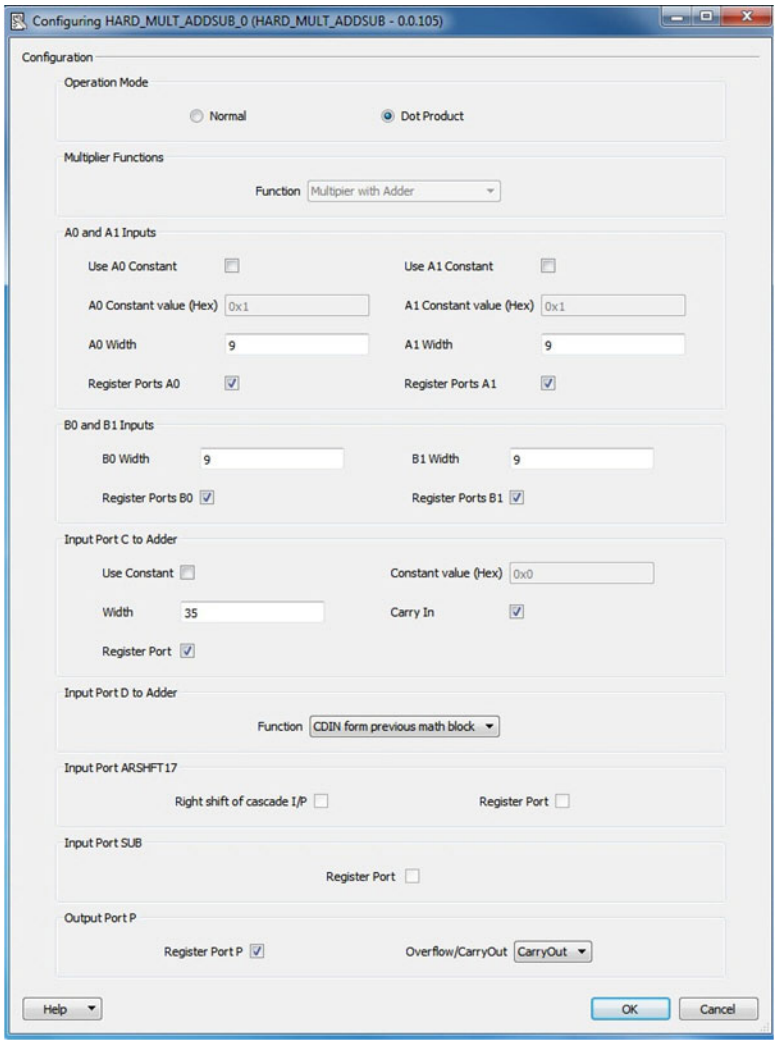

***Figure 1-2* • Hard Multiplier Add Configuration Options - Dot Product Mode**

After configuring and generating the macro instance, you can simulate basic functionality. The macro can then be instantiated as a component of a larger design.

2 – Core Parameters

Table 2-1 lists the Normal mode Hard Multiplier AddSub settings; Table 2-2 lists the Dot Product mode settings.

***Table 2-1* • Hard Multiplier AddSub Normal Mode Configuration Description**

Name	Valid Range	Description
Multiplier Functions		
Function	Multiplier with Adder Multiplier with Subtractor Multiplier with Adder/Subtractor	The Multiplier with Adder/Subtractor exposes the SUB control signal, which enables you to dynamically toggle between an add or subtract operation.
Input Port A0		
Use Constant		Sets input port A0 to constant
Constant Value (Hex)	-2^{17} to (2^{17} - 1)	Two's complement value of A0, if A0 is constant. Values shorter than 18 bits are padded with zeros. Negative values must be a full 18 bits wide. For example, 0x1FFFF means +131071 (2^{17} - 1), while 0x3FFFF means -1
Width	2 to 18	Width of input port A0; if shorter than 18 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1
Register Port		Registers input port A0 (if A0 is not set to constant)
Input Port B0		
Width	2 to 18	Width of input port B0; if shorter than 18 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1.
Register Port		Registers input port B0
Input Port C		
Use Constant		Sets input port C to constant
Constant Value (Hex)	-2^{43} to (2^{43} - 1)	Two's complement value of C, if C is constant. Values shorter than 44 bits are padded with zeros. Negative values must be a full 44 bits wide.
Width	2 to 44	Width of input port C; if shorter than 44 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1.
Carry In		Carry in for C (if C is not set to constant)
Register Port		Registers input port C and Carry In (if C is not set to constant)
Input Port D to Adder		

***Table 2-1* • Hard Multiplier AddSub Normal Mode Configuration Description (continued)**

Name	Valid Range	Description
Function		Select CDIN from previous math block
Input Port ARSHFT17		
Right Shift of Cascade input		Cascade input is arithmetic right-shifted by 17 if selected.
Register Port		Registers ARSHFT17 control signal
Input Port SUB		
Register Port		Registers SUB control signal when multiplier with Adder/Subtractor option is selected
Output Port P		
Register Port		Registers output port P, CDOUT and Overflow/CarryOut
Overflow/CarryOut	None, Overflow, CarryOut	Select the output port function to include in the module interface

***Table 2-2* • Hard Multiplier Add Dot Product Mode Configuration Description**

Name	Valid Range	Description
Input Port A0		
Use Constant		Sets input port A0 to constant
Constant Value (Hex)	-2^8 to (2^8 - 1)	Two's complement value of A0, if A0 is constant. Values shorter than 9 bits are padded with zeros. Negative values must be a full 9 bits wide. For example, 0xFF means +255 (2^8 - 1), while 0x1FF means -1
Width	2 to 9	Width of input port A0; if shorter than 9 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1.
Register Port		Registers input port A0 (if A0 is not set to constant)
Input Port A1		
Use Constant		Sets input port A1 to constant
Constant Value (Hex)	-2^8 to (2^8 - 1)	Two's complement value of A1, if A1 is constant. Values shorter than 9 bits are padded with zeros. Negative values must be a full 9 bits wide. For example, 0xFF means +255 (2^8 - 1), while 0x1FF means -1
Width	2 to 9	Width of input port A1; if shorter than 9 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1.
Register Port		Registers input port A1 (if A1 is not set to constant).
Input Port B0		

***Table 2-2* • Hard Multiplier Add Dot Product Mode Configuration Description**

Name	Valid Range	Description
Width	2 to 9	Width of input port B0; if shorter than 9 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1.
Register Port		Registers input port B0
Input Port B1		
Width	2 to 9	Width of input port B1; if shorter than 9 bits it is sign-extended. For example, if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1.
Register Port		Registers input port B1
Input Port C		
Use Constant		Sets input port C to constant
Constant Value (Hex)	-2^{35} to (2^{35} - 1)	Two's complement value of C, if C is constant. Values shorter than 35 bits are padded with zeros. Negative values must be a full 35 bits wide.
Width	2 to 35	Width of input port C; if shorter than 35 bits it is sign-extended
Carry In		Carry in for C (if C is not set to constant)
Register Port		Registers input port C and Carry In (if C is not set to constant)
Input Port D to Adder		
Function		Select CDIN from previous math block
Output Port P		
Register Port		Registers output port P, CDOUT, and Overflow/CarryOut
Overflow/CarryOut	None, Overflow, CarryOut	Select the output port function to include in the module interface

3 – Port Description

The figures below display the Hard Multiplier AddSub input and output ports for Normal mode (Figure 3-1) and Dot Product mode (Figure 3-2). The ports shown are a superset of all possible ports. Only a subset of the ports is used in any given Hard Multiplier AddSub configuration.

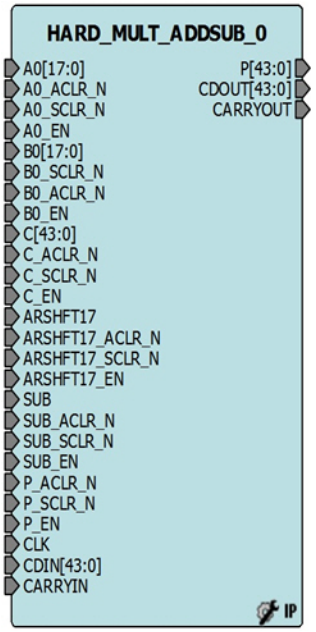

Figure 3-1 **• Hard Multiplier AddSub Ports, Normal Mode**

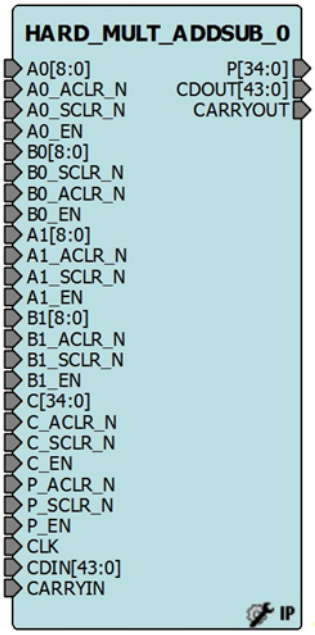

***Figure 3-2* • Hard Multiplier Add Ports, Dot Product Mode**

Table 3-1 lists the Hard Multiplier AddSub port signals for Normal mode.

***Table 3-1* • Hard Multiplier AddSub Ports - Normal Mode**

Signal	Direction	Description
A0	Input	Input data A0, 2- 18 bits wide
B0	Input	Input data B0, 2- 18 bits wide
C	Input	Input data C, 2- 44 bits wide
CLK	Input	Input clock for all registers
A0_ACLR_N	Input	Asynchronous reset for data A0 registers
A0_SCLR_N	Input	Synchronous reset for data A0 registers
A0_EN	Input	Enable for data A0 registers
B0_ACLR_N	Input	Asynchronous reset for data B0 registers
B0_SCLR_N	Input	Synchronous reset for data B0 registers
B0_EN	Input	Enable for data B0 registers
C_ACLR_N	Input	Asynchronous reset for data C, Carry In registers
C_SCLR_N	Input	Synchronous reset for data C, Carry In registers
C_EN	Input	Enable for data C, Carry In registers
ARSHFT17_ACLR_N	Input	Asynchronous reset for ARSHF T17 register

***Table 3-1* • Hard Multiplier AddSub Ports - Normal Mode (continued)**

Signal	Direction	Description
ARSHFT17_SCLR_N	Input	Synchronous reset for ARSHF T17 register
ARSHFT17_EN	Input	Enable for ARSHFT17 register
SUB_ACLR_N	Input	Asynchronous reset for input control SUB registers
SUB_SCLR_N	Input	Synchronous reset for input control SUB registers
SUB_EN	Input	Enable for input control SUB registers
SUB	Input	Input control signal to select between add or subtract operation
P_ACLR_N	Input	Asynchronous reset for result P, CDOUT, Overflow/Carryout registers
P_SCLR_N	Input	Synchronous reset for result P, CDOUT, Overflow/Carryout registers
P_EN	Input	Enable for result P, CDOUT, Overflow/Carryout registers
CDIN	Input	Input cascade data from previous math block, 44 bits wide
CARRYIN	Input	Carry In for operand C
P	Output	P = D + CARRYIN + C + (A0 * B0) when SUB = 0 P = D + CARRYIN + C - (A0 * B0) when SUB = 1
OVERFLOW	Output	When high, indicates that the result exceeded the width of output P. OVERFLOW = (P[45] ^ P[44]) | (P[44] ^ P[43])
CARRYOUT	Output	This bit can be used to extend the adder in the fabric. CARRYOUT = C[43] ^ D[43] ^ P[44]
CDOUT	Output Cascade	Cascade output of result P. CDOUT is a copy of P, sign-extended to 44 bits. The entire bus must either be dangling or drive an entire CDIN of another MATH block in Normal mode.

Table 3-2 lists the Hard Multiplier Add port signals for Dot Product mode.

***Table 3-2* • Hard Multiplier Add Ports - Dot Product Mode**

Signal	Direction	Description
A0	Input	Input data A0, 2- 9 bits wide
B0	Input	Input data B0, 2- 9 bits wide
A1	Input	Input data A1, 2- 9 bits wide
B1	Input	Input data B1, 2- 9 bits wide
C	Input	Input data C, 2- 35 bits wide
CLK	Input	Input clock for all registers
A0_ACLR_N	Input	Asynchronous reset for data A0 registers
A0_SCLR_N	Input	Synchronous reset for data A0 registers
A0_EN	Input	Enable for data A0 registers
B0_ACLR_N	Input	Asynchronous reset for data B0 registers
B0_SCLR_N	Input	Synchronous reset for data B0 registers
B0_EN	Input	Enable for data B0 registers
A1_ACLR_N	Input	Asynchronous reset for data A1 registers
A1_SCLR_N	Input	Synchronous reset for data A1 registers
A1_EN	Input	Enable for data A1 registers
B1_ACLR_N	Input	Asynchronous reset for data B1 registers
B1_SCLR_N	Input	Synchronous reset for data B1 registers
B1_EN	Input	Enable for data B1 registers
C_ACLR_N	Input	Asynchronous reset for data C, Carry In registers
C_SCLR_N	Input	Synchronous reset for data C, Carry In registers
C_EN	Input	Enable for data C, Carry In registers
CARRYIN	Input	Carry In for operand C
CDIN	Input	Input cascade data from previous math block
P_ACLR_N	Input	Asynchronous for result P, CDOUT, Overflow/Carryout registers
P_SCLR_N	Input	Synchronous reset for result P, CDOUT, Overflow/Carryout registers
P_EN	Input	Enable for result P, CDOUT, Overflow/Carryout registers
P	Output	P = D + CARRYIN + C + (A0 * B0) + (A1 * B1)
OVERFLOW	Output	When high, indicates that the result exceeded the width of output P. OVERFLOW = (P[36] ^ P[35]) | (P[35] ^ P[34])

***Table 3-2* • Hard Multiplier Add Ports - Dot Product Mode**

Signal	Direction	Description
CARRYOUT	Output	This bit can be used to extend the adder in the fabric. CARRYOUT = C[34] ^ D[34] ^ P[35]
CDOUT	Output Cascade	Cascade output of result P. CDOUT is a sign-extended copy of P. The entire bus must either be dangling or drive an entire CDIN of another MATH block in Dot Product mode.

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Fax, from anywhere in the world, 408.643.6913

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Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

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The technical support email address is soc_tech@microsemi.com.

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