UG0602
User Guide
RTG4 FPGA Programming

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 9.0

The following is a summary of changes made in revision 9.0 of this document:

- Updated Table 1, page 3 to add DirectC and ChipPro Solution.
- Added In-Flight Reprogramming, page 16.

1.2 Revision 8.0

The following is a summary of changes made in revision 8.0 of this document:

- Updated Note below Table 1, page 3.
- Updated section Programming File Size, page 5.
- Updated section JTAG Power Supply Requirements, page 8.
- Updated section State of RTG4 Components During Programming, page 10.

1.3 Revision 7.0

The following is a summary of changes made in revision 7.0 of this document:

- Updated the information about FlashPro Express. For more information, see Digest, page 11.
- Update the information about power interruption during programming. For more information see, Programming Flow, page 5.

1.4 Revision 6.0

Information about Digest check was updated. See Digest, page 11.

1.5 Revision 5.0

The following is a summary of changes made in revision 5.0 of this document:

- Information about the silicon sculptor was removed. Silicon sculptor programming is not supported for RTG4 devices.
- Information about JTAG_TCK was updated. See JTAG Programming, page 6.

1.6 Revision 4.0

The following is a summary of changes made in revision 4.0 of this document:

- Added a note about standalone erase in the introduction chapter. For more information, see RTG4 FPGA Programming, page 3.
- Deleted the SPI Slave Programming section and all the related information about SPI slave programming in this document.
- Added the Digest Checks section. For more information, see Digest, page 11.
- Replaced the pin name VDDJ with VDDI3 in the RTG4 FPGA Programming chapter. For more information, see RTG4 FPGA Programming, page 3.

1.7 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Information about RTG4 programming modes was updated. For more information, see Table 1, page 3.
- The RTG4 programming flow was updated. For more information, see Programming Flow, page 5.
- The Programming Using an External Microprocessor section was removed.
- Information about the SPI master was updated.

- The document was changed to the new template.

1.8 Revision 2.0

Removed references of security throughout the document (SAR 66946).

1.9 Revision 1.0

Revision 1.0 was the first publication of this document.

2 RTG4 FPGA Programming

RTG4™ FPGAs offer a variety of programming options to cater to diverse end-user applications. The device supports programming of the following components:

- FPGA fabric
- µPROM

RTG4 devices can be programmed by JTAG. In JTAG programming, the device is programmed using an external master such as Microchip FlashPro4/5/6 programmer, an external microprocessor or ChipPro solution. The following table lists different programming modes and interfaces. In the following sections, these programming methods are discussed in detail.

Table 1 • **RTG4 Programming Modes**

Mode	Interface	Master	Software	Bitstream Format
JTAG Programming	System Controller dedicated JTAG port	External FlashPro4/5/6 Programmer	Libero® SoC/FlashPro	Libero SoC default file/STAPL
		External Microprocessor	DirectC	DAT
		ChipPro solution using FlashPro6	ChipPro Solution	STAPL

Note:

- Erase has no adverse effects and no reliability concerns when performed as part of a full programming cycle or as a standalone operation. Retention and endurance qualification of non-volatile cells were performed using full programming cycles.
- Each programming operation will increment the cycle count by one. Each standalone erase operation will increment the cycle count by two. Ensure that the cycle count never exceeds the maximum number of programming or erase cycles specified in the datasheet (200 cycles).
- Microchip documentation discourages customers from performing standalone erase operations on flight units so that the cycle count always reports the exact number of programming cycles performed on these units. For example, if ten programming operations and two standalone erase operations are performed on a unit, its cycle count will report 14. It could be interpreted as 14 programming operations or seven standalone erase operations or any combinations leading to a cycle count of 14. There is no dedicated hardware to count standalone erase operations and Programming operations separately.

2.1 Bitstream Generation

Libero SoC generates the programming bitstream required to support the different programming modes.

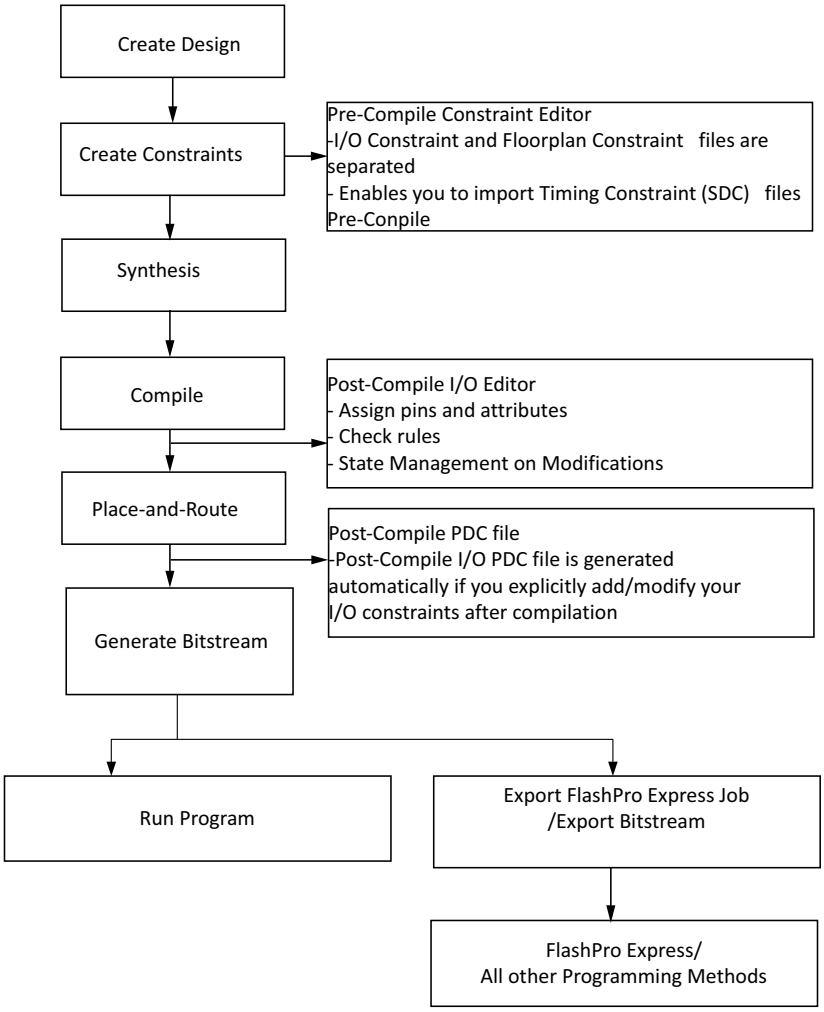
2.1.1 Libero SoC Programming Bitstream Generation Flow

Libero SoC is used to generate the programming bitstream formats needed for different programming modes. The following figure shows the Libero SoC programming bitstream generation flow.

After implementation of the design, the programming bitstream is generated by clicking the **Generate Bitstream** option in Libero. As programming is integrated into the Libero SoC software design flow, you can program the device directly by clicking **Program Design > Run PROGRAM Action**.

You can also program the device using standalone programming tool FlashPro Express. Export *.job file from Libero SoC (Export FlashPro Express Job menu). For more information, see *FlashPro Express User Guide*.

Figure 1 • **Libero SoC Programming Bitstream Generation Flow**



2.1.2 Programming File Size

The µPROM is part of the fabric. When the fabric is programmed, the µPROM will also be programmed if bitstream contains the µPROM (partial or full content) data. The following table lists the typical bitstream size and format for RTG4 devices.

Table 2 • **Programming Bitstream Size**

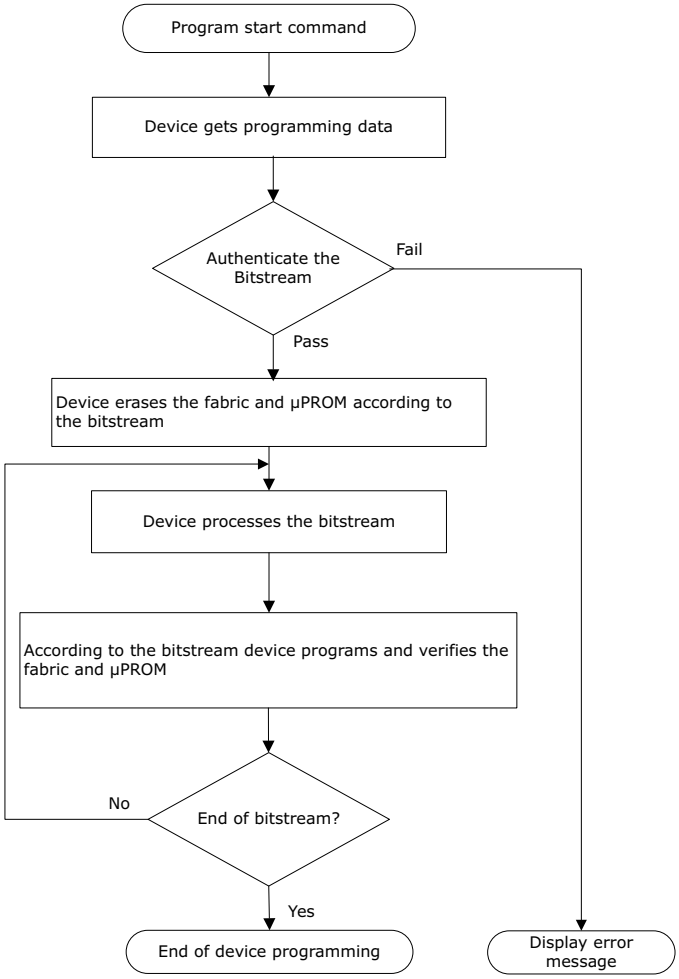
Device	File Type	Fabric + µPROM Full
RT4G150	STAPL	8 MB

2.2 Programming Flow

The programming flow starts when the system controller initiates the device programming start command, and ends when the bitstream data is fully transferred and verified. Verification of the programmed contents are part of the programming flow. It is recommended not to interrupt the programming flow. If the programming flow is interrupted or fails before completion, the device will not be enabled. The FPGA is enabled only after the entire bitstream is successfully programmed. Interrupt during programming may damage the device. The following figure summarizes the RTG4 programming flow.

Note: Power interruption is not supported during programming.

Figure 2 • **Programming Flow**



2.3 JTAG Programming

RTG4 devices have a built-in JTAG controller that is compliant with IEEE 1149.1 and compatible with IEEE 1532. An external programmer, such as FlashPro4/5/6, is used to program the device. The devices can be programmed in both single and chain modes.

The RTG4 devices have JTAG pins in a dedicated bank, which varies depending on the package. For more information about banks and their locations, see *RTG4 FPGA Pin Descriptions*.

JTAG banks can be operated at 1.8 V, 2.5 V, or 3.3 V.

The logic level of the JTAG signals depends on the JTAG bank voltage. The following table lists the JTAG pin names and descriptions.

The JTAG interface is used for device programming and testing or for debugging instantiated soft processor firmware, as listed in the following table. JTAG I/Os are powered by the VDDI3 supply associated with the bank where the I/O reside.

Table 3 • **JTAG Pins**

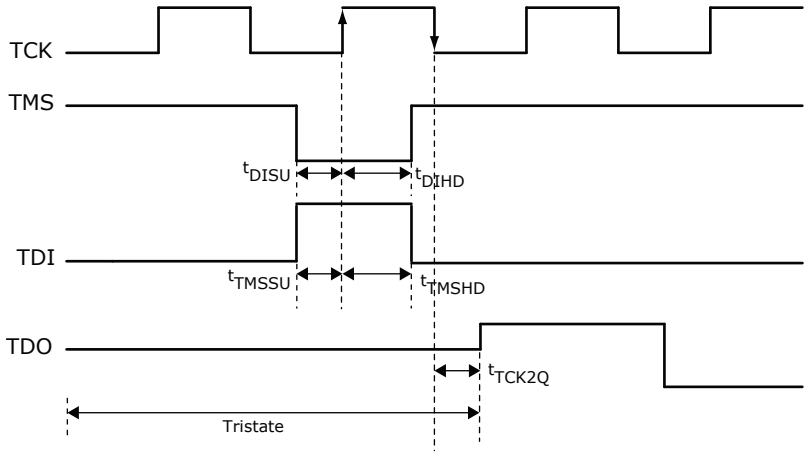
Pin Name	Direction	Weak Pull-up	Description
JTAG_TMS	Input	Yes	JTAG test mode select. Do not connect (DNC) in unused condition.
JTAG_TRSTB	Input	Yes	JTAG test reset. Must be held low during device operation. In unused condition, pull down to VSS through 1 kΩ resistor for upset immunity.
JTAG_TDI	Input	Yes	JTAG test data in. DNC in unused condition.
JTAG_TCK	Input	No	JTAG test clock. When unused, TCK be tied to VSS or VDDI3 through 200 to 1 kΩ resistor on the board as per IEEE 1532 requirements. This prevents totem pole current on the input buffer.
JTAG_TDO	Output	No	JTAG test data out. DNC in unused condition.

For more information about JTAG, see *AC439: Board Design Guidelines for RTG4 FPGA Application Note*.

2.3.1 JTAG Timing

Proper operation of JTAG programming depends on the timing relationship between JTAG pins as shown in the following figure. For the recommended timing values, see the 1532 timing characteristics table of the *DS0131: RTG4 FPGA Datasheet*.

Figure 3 • **JTAG Signals Timing Diagram**



2.3.2 JTAG Programming Architecture

The system controller implements the functionality of a JTAG slave and complies to IEEE 1532 and IEEE 1149.1 standards. The JTAG port communicates with the system controller using:

- a command register that sends the JTAG instruction to be executed.
- a 128-bit data buffer that transfers any associated data.

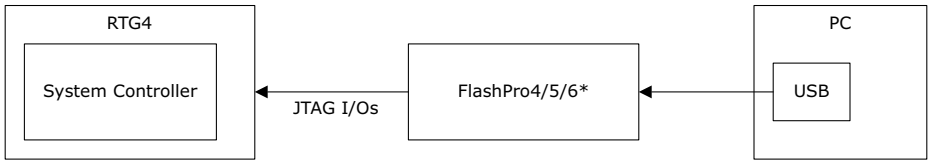
2.3.3 Design Implementation

The FPGA fabric and the µPROM can be programmed using JTAG programming mode.

- An USB-based FlashPro4/5/6 programmer can be used to program the RTG4 device using the dedicated JTAG interface. Libero SoC (or standalone FlashPro Express) executes the programming from a PC connected to the programmer.

The following figure shows the FlashPro4/5/6 programmer connected to the JTAG ports of a RTG4 device. Only this programming mode is supported by the current version of the Libero SoC software.

Figure 4 • **JTAG Programming Mode**



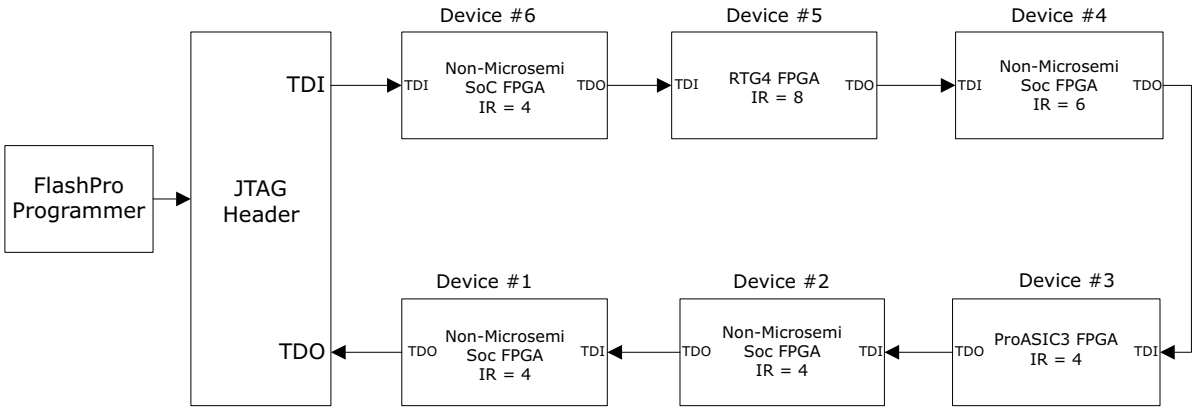
* The FlashPro3 programmer can be used in JTAG programming mode but it has been discontinued.

A single FlashPro4/5/6 programmer can also program multiple Microchip FPGAs from the same family or from different families in a single JTAG chain.The TDO pin of the JTAG header represents the beginning of the chain. The TDI pin of the last device is connected back to the JTAG header, thus completing the chain.

A non-Microchip FPGA can also be included in the chain as shown in the Figure 5, page 7. When a Microchip FPGA within a chain is programmed, all non-Microchip FPGAs in the chain are placed in bypass mode. When a device is in bypass mode, the device's data register length is automatically set to 1 and the device stops responding to any programming instructions.

For more information about JTAG chain programming, see the *FlashPro Express User Guide*.

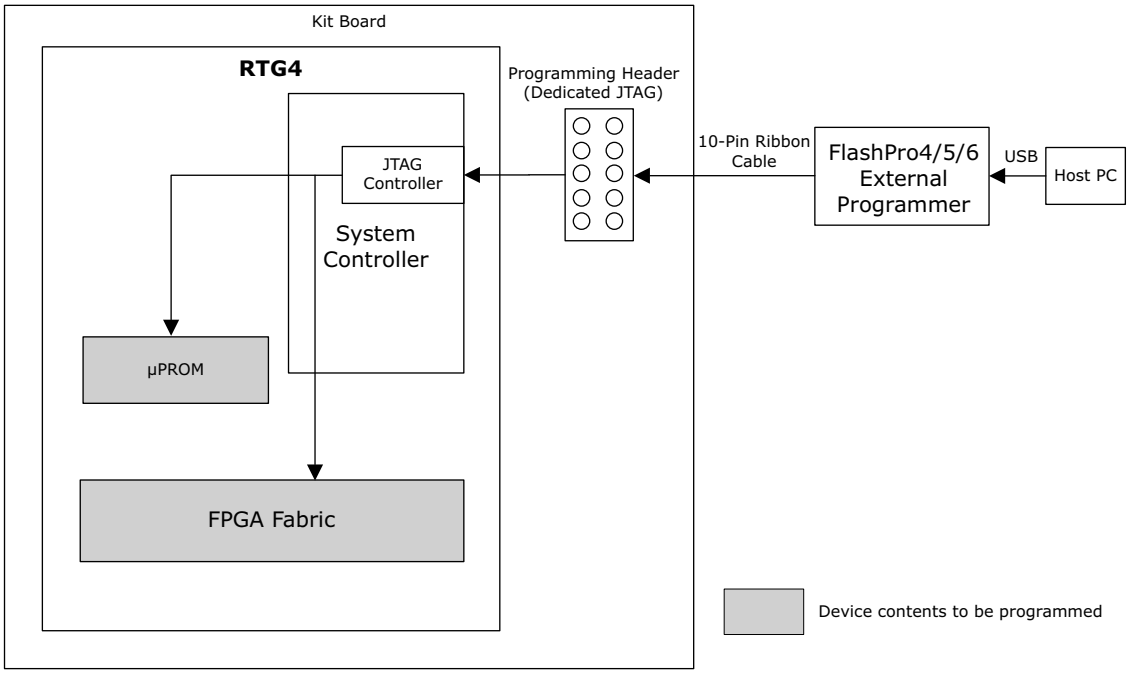
Figure 5 • **Device Programming in JTAG Chain**



2.3.4 Programming Using an External Programmer

RTG4 devices can be programmed using an external programmer through the dedicated JTAG port. When programming with the Libero SoC or standalone FlashPro Express software, FlashPro4/5/6 cable must be connected to the JTAG pins of the device through a 10-pin programming header, as shown in the following figure. The target board must provide power to the VPP, VDD, and VDDI3 pins.

Figure 6 • **JTAG Programming using External Programmer**



2.3.4.1 JTAG Power Supply Requirements

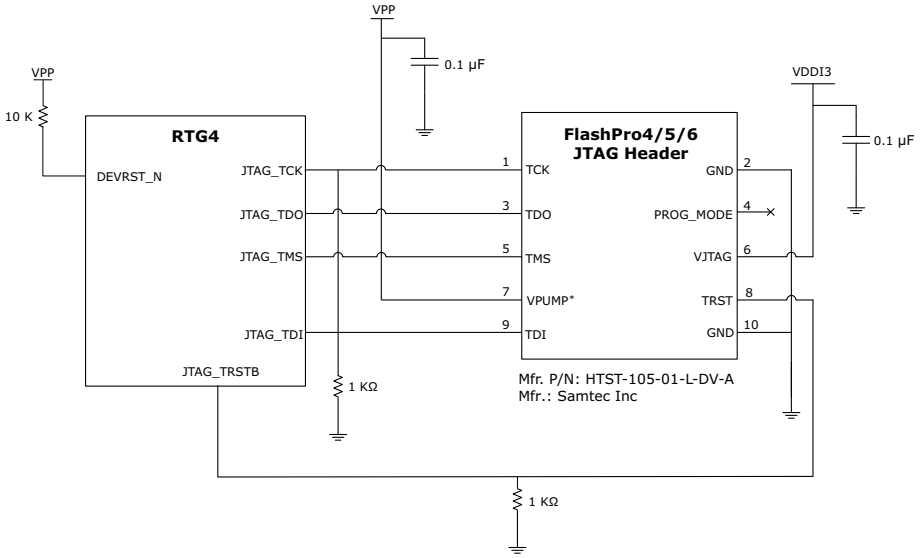
The power supplies must conform to the specification as defined in the *DS0131: RTG4 FPGA Datasheet*. Measures must be taken to ensure signal integrity, so that power supplies and JTAG signals are free from noise.

Before programming, the FPGA needs to be powered up. The power supply to the JTAG bank must be turned on.

RTG4 FPGAs require a single programming voltage to be applied at the VPP pin during programming. This voltage must be supplied from the board. When the device is not programmed under normal operating conditions, VPP must be connected to its supply range. The board must supply power to the VPP, VDD, VDDI3 pins of the device, and the VJTAG pin of the programmer header. VDDI3 provides power to the JTAG circuitry. For more information about voltage range, see the *DS0131: RTG4 FPGA Datasheet*.

Microchip recommends that VPP and JTAG power supply lines (VDDI3) are kept separate with independent filtering capacitors. See the following figure for capacitor requirements. The bypass capacitor must be placed within 2.5 cm of the device pins. The following figure shows the connections between the programming header and the device.

Figure 7 • **JTAG Programming of a Single RTG4 Device**



Note: From Libero SoC v11.8 SP3 and later, FlashPro does not detect or drive VPUMP for SmartFusion2, IGLOO2, and RTG4 devices. FlashPro detects and drives VPUMP only when ProASIC3/IGLOO/Fusion/SmartFusion device is detected in the chain.

- FlashPro does not detect VPP on SmartFusion2, IGLOO2, and RTG4 devices. VPUMP pin on this board can be left floating.
- If the board contains ProASIC3/IGLOO/Fusion/SmartFusion along with SmartFusion2/IGLOO2/RTG4 in the JTAG chain, then connect VPUMP of the ProASIC3/IGLOO/Fusion/SmartFusion to the JTAG header of the VPUMP pin.

2.3.5 JTAG Programming Using External Microprocessor

An external microprocessor can be used to program the device through the dedicated JTAG interface. This type of programming requires that the external microprocessor run DirectC, a Microchip programming solution for FPGAs, and the microprocessor's GPIO ports drive the JTAG interface.

Note: The DirectC solution supports programming of the FPGA fabric and uPROM. DirectC is used by adding the necessary APIs and compiling the source code to create a binary executable. The binary executable is downloaded to the external microprocessor along with the programming data file. For more information about DirectC, see *Embedded Programming*.

2.3.6 JTAG Programming Using ChipPro Solution

The ChipPro programmer baseboard with FlashPro6 can be used to program the device through the dedicated JTAG interface. This can be done either using the Libero SoC or a standalone FlashPro Express. For information about ChipPro, see *CP-PROG-BASE*.

2.4 State of RTG4 Components During Programming

The following table lists the state of each ASIC block and I/O type during the programming mode described in this user guide. You can configure the I/O state during JTAG programming in Libero SoC, as shown in the following figure. For more information about device I/O states during programming, see the *Libero SoC User Guide*.

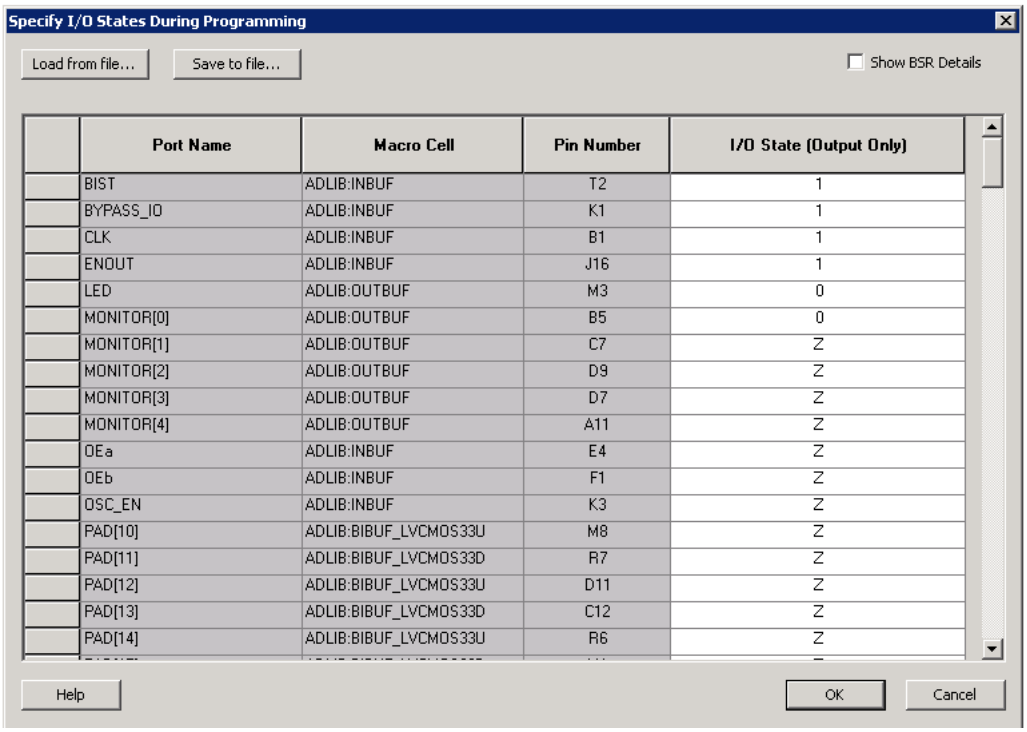
Note: I/Os are tristated in the blank devices, that is, factory shipped unprogrammed devices.

Table 4 • **ASIC Block and I/O State During Programming**

	Programming Methodology
Components	**JTAG**
Shared I/O (fabric/FDDR)	Tristated by system controller
Dedicated Fabric I/O	Tristated by system controller
SerDes I/O	Unaffected by programming
FDDR Block	Fabric interfaces gated off by a flash bit (so no transactions can occur at config APB, AHB/AXI interfaces to fabric)
SerDes Block	Fabric interfaces gated off by a flash bit (so no transactions can occur at config APB, AHB/AXI interfaces to fabric)

The following figure shows the various I/O states of RTG4 components during programming.

Figure 8 • **I/O States During Programming**



If the RTG4 is the only driver on the line, and there are no external contentions or shorts, then there is no reliability concern for RTG4. If this RTG4 output pair drives another RTG4 LVDS receiver, there is no issue because the RTG4 input pins can tolerate the full voltage swing from GND to the VDDI for the corresponding bank.

To prevent damage to the external LVDS receiver, it must be able to tolerate the full voltage swing from 0 V to VDDI on its inputs without reliability impact. If not, then the external LVDS receiver must have failsafe support for either open or shorted inputs. If the receiver supports failsafe for open (floating) differential inputs, then the user can configure both FPGA output pads to be the default tristate output during programming. If the receiver supports failsafe for shorted and terminated inputs, then the user can configure both FPGA output pads to be LOW during programming. Since the device is erased during programming, the I/O standard does not matter.

2.5 Digest

Digest is a 32-bit Multiple Input Shift Register (MISR) CRC code generated by a hardware circuit in the System controller. It is generated for Fabric/µPROM of the FPGA. Digest is used for protecting the data integrity.

The digest is printed during bitstream generation and bitstream programming. When a user creates a design in Libero and then exports the FlashPro Express job, the fabric digest is printed in the Libero log window and saved in a digest file under the export folder. The digest file is a text file containing the 32-bit digest value. The name of the digest file will match the name of the FlashPro Express job exported, and will be appended with a ".digest" extension.

The digest is also printed at the end of programming operation in the Libero and FlashPro Express log. The user can compare this printed digest with the same in the exported digest file to ensure the intended programming of the FPGA.

2.5.1 Digest Check – VERIFY_DIGEST

During programming operation, the digest is calculated simultaneously and stored in the fabric user segment. When VERIFY_DIGEST is performed, the digest is recalculated and compared against the stored value in the fabric user segment. This compare ensures the image programmed in the device has not changed since the last time the device was programmed.

There is no digest check on power-up, and a digest check (that is, VERIFY_DIGEST) has to be initiated through Libero or FlashPro Express.

Note: It is recommended to keep the track of how many times VERIFY_DIGEST and/or verify are performed as Libero SoC does not keep a track of the count (impacts the data retention limit). For more information about maximum number of counts, see *DS0131: RTG4 FPGA Datasheet*.

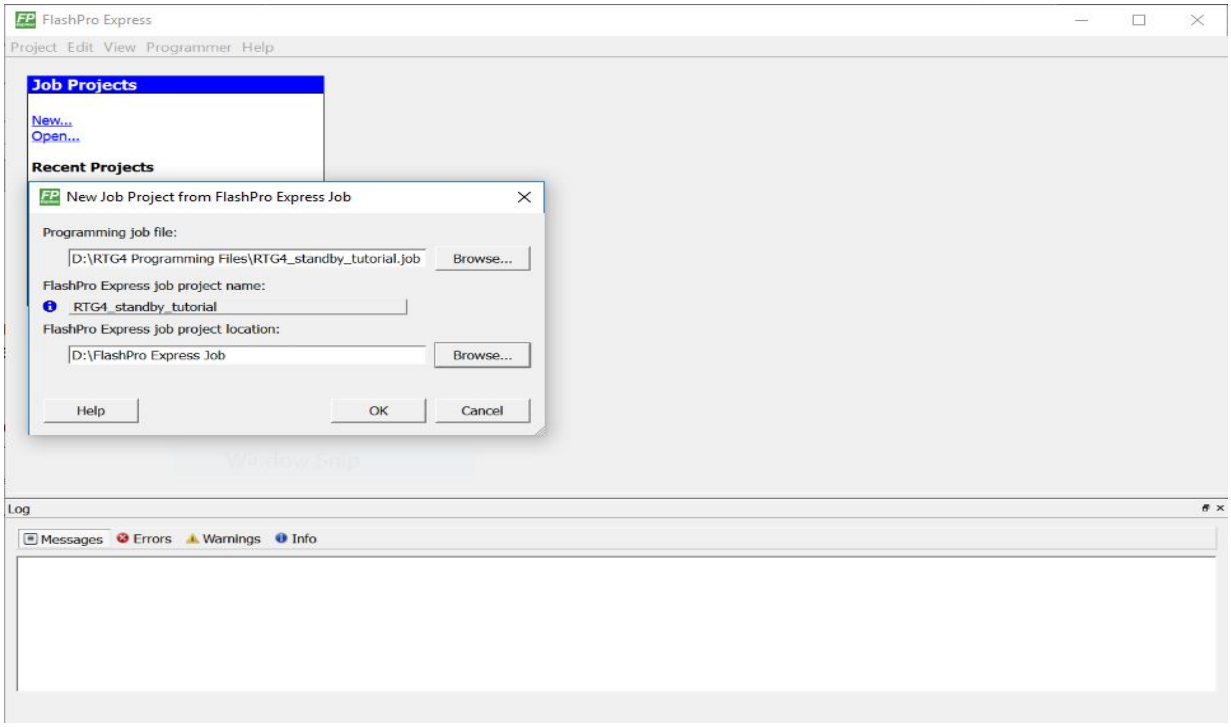
2.5.1.1 Use Model

Use the VERIFY_DIGEST setting if there is any concern about bitstream modification. User may consider disabling this function for security concerns. See Figure 13, page 14 on how to disable this action in Libero.

To perform a VERIFY_DIGEST,

1. Launch **FPExpress**.
2. Click **New** or select **New Job Project** from FlashPro Express Job from Project menu to create a new job project.
3. Enter the following in the New Job Project from FlashPro Express Job dialog box:
   - Programming job file: Click **Browse**, and navigate to the location where the .job file is located and select the file.
   - FlashPro Express job project location: Click **Browse** and navigate to the location where you want to save the project.
4. Click **OK**.

Figure 9 • **Configuring the Digest Check**

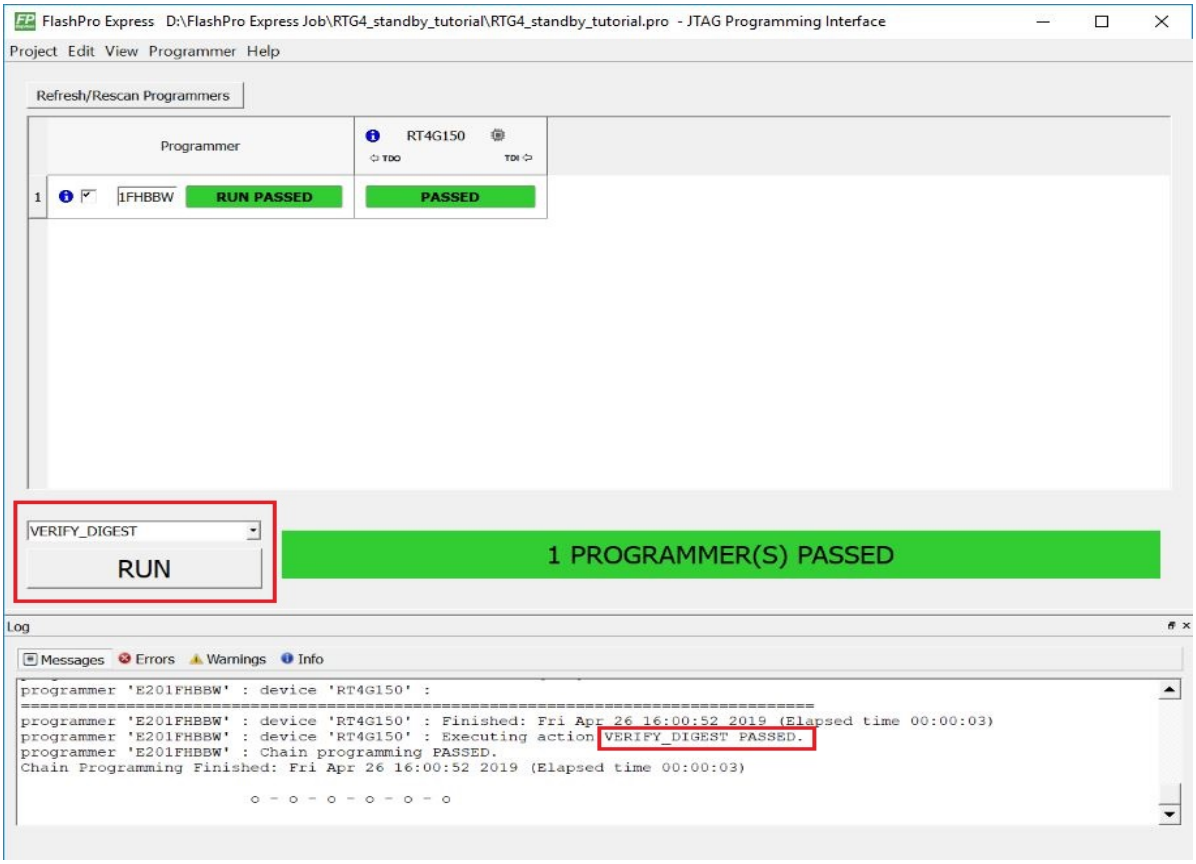


5. From the Drop Down select **VERIFY_DIGEST** from the list.

Figure 10 • **Verifying Digest**

6. Click **VERIFY_DIGEST**. The log window displays the digest check status.

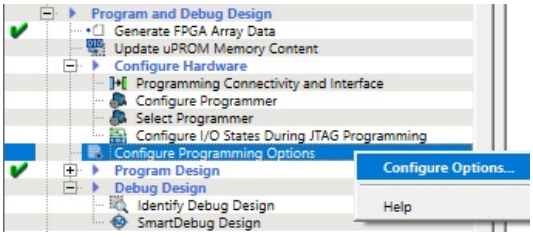
Figure 11 • **Verifying Digest – Log Details**



To disable a digest check:

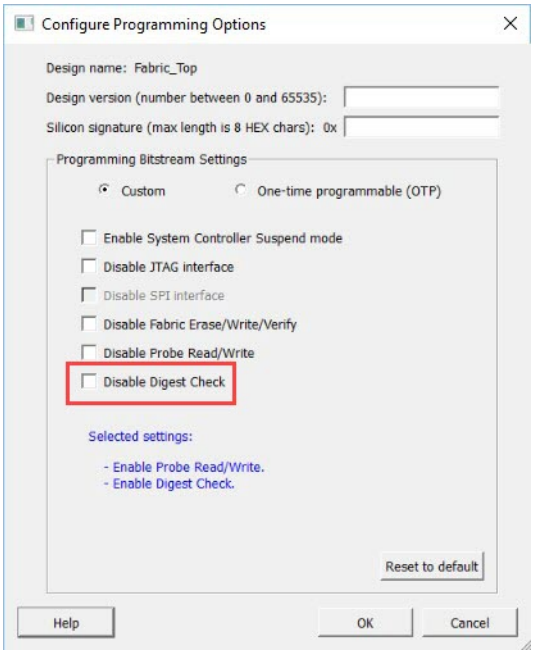
1. In the Libero project **Design Flow** window, double-click **Configure Programming Options** or right-click and click **Configure Options**.

Figure 12 • **Configuring Programming Options**



2. Select the **Disable Digest Check** check box under **Programming Bitstream Settings**.

Figure 13 • **Disabling Digest Check**



Note: To disable the digest check, you need to first program the device with **Disable Digest Check** option enabled and power cycle the device with TRSTB pin tied to LOW.

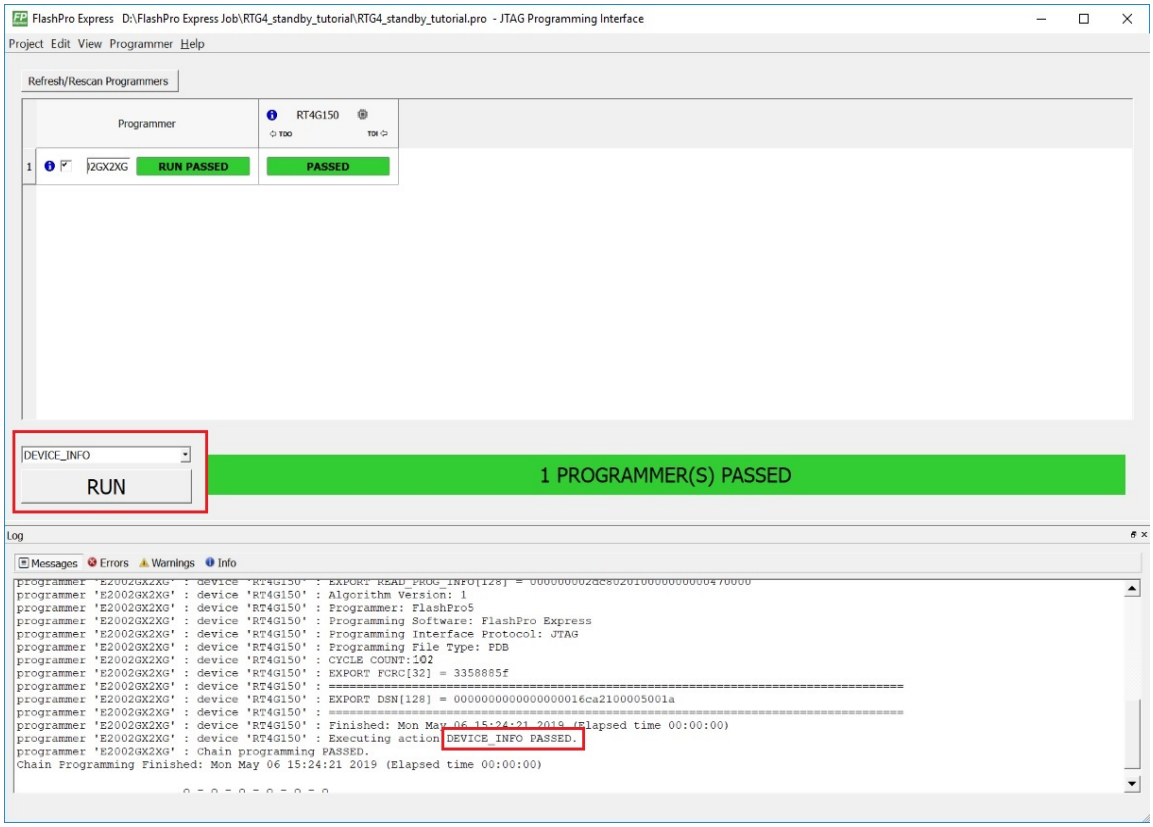
2.5.2 Digest Check – DEVICE_INFO

DEVICE_INFO action is available in both Libero and FlashPro Express software. Design name, Design checksum and Fabric digest are printed in the DEVICE_INFO log. These can be manually compared to the checksum in the STAPL file and digest in the .digest file to ensure the device is programmed with the intended design. There is no restriction on number of times DEVICE_INFO is performed (that is, no impact on retention limit).

2.5.2.1 Use Model

DEVICE_INFO is a quick way to check the status of a programmed device and to ensure that the intended design has been programmed into the device. DEVICE_INFO also prints Cycle Count in the log file, which can be used to track the retention limit as shown in the following figure.

Figure 14 • **DEVICE_INFO – Log Details**



2.6 In-Flight Reprogramming

Reprogramming on orbit is increasingly becoming a hard requirement for space payload electronics. Satellite payload electronics' complexity have evolved so much that it is impossible to identify hardware bugs until the satellite is launched. The ability to reprogram an FPGA in space can be used to fix critical bugs. Furthermore, re-programmability in the FPGAs enables tuning of data processing algorithms to give the optimum results for new science missions. When the primary mission of the satellite is accomplished, the satellite hardware can be re-purposed to accomplish additional objectives if the FPGAs can be reprogrammed.

2.6.1 In-Flight Reprogramming Guidance

Microchip has performed several sets of radiation tests on RTG4 FPGAs and determined that the FPGAs can be programmed in space, with a greater-than-99% probability of success on orbit.

RTG4 reprogramming in space is supported with the following guidance:

- Single Event Effects (SEE) Impact
  - Probability of first-time success for programming in GEO-synchronous orbit with Solar-Min conditions is calculated to be greater than 99%. If radiation disrupts programming, it is highly likely that the next programming attempt will succeed. Heavy ion test results can be found in *RTG4 PLL, POR and Inflight-Programming Heavy Ion SEE Report*.
  - Probability of programming success in LEO is very high. No programming or verify failure was observed in accelerated ground testing. See *RTG4 Proton Testing Report*.
  - In-beam reprogramming and verify is non-destructive as seen in accelerated ground testing.
  - It is unlikely that an ion will disrupt programming, since the flux in space is many orders of magnitude lower than the flux used during accelerated ground testing.
- Total Ionizing Dose (TID) Impact
  - Reprogramming can be accomplished at TID levels up to 50 Krad, which is sufficient for 10 years of GEO and more than 20 years of LEO.

2.6.2 In-Flight Reprogramming Sequence

In the DirectC v2021.2 release, a new “Reprogram_InFlight” action will be introduced to take care of the entire required sequence for RTG4 in-flight reprogramming. See *DirectC v2021.2 User Guide* for information about "Reprogram_InFlight" action.

For information about timing requirements and interface to the RTG4 JTAG pins, see JTAG Programming, page 6.

2.6.3 In-Flight Reprogramming Solutions

A programming controller is required to retrieve the new programming code from an external memory and to upload the new code into the target RTG4 FPGA, which is to be programmed. Some of the viable options for a programming controller includes (but not limited to):

- Standalone radiation-tolerant microcontroller such as Microchip's SAMRH71F20. A reference design is available in *GitHub*. A demonstration video can be found *here*.
- Other possible solutions which include implementing a JTAG player in RTL or using a soft processor in an FPGA. These solutions have not been tested by Microchip.